实验九 计数器的设计 实验报告

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1 实验目的

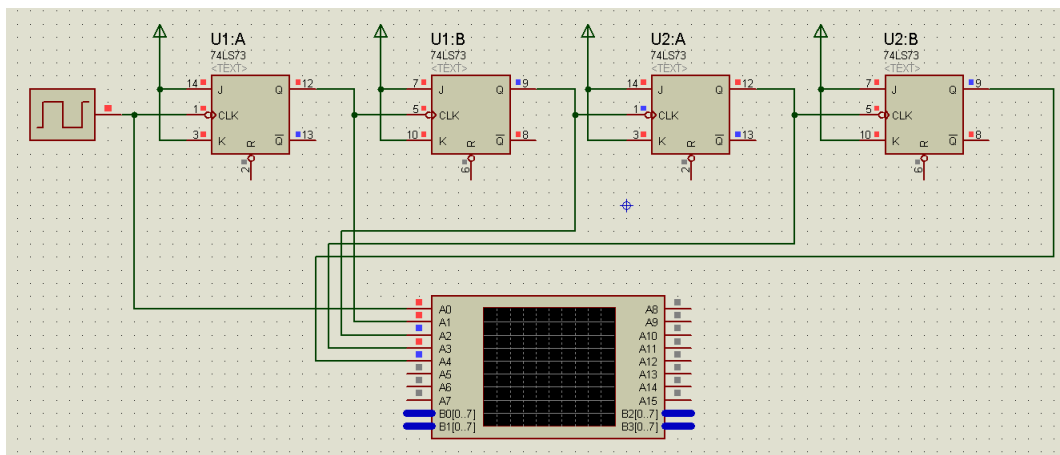熟悉 JK 触发器的逻辑功能，掌握 JK 触发器构成异步计数器和同步计数器。

2 实验仪器

1. 实验箱、万用表、示波器
2. 74LS73、74LS00、74LS08、74LS20
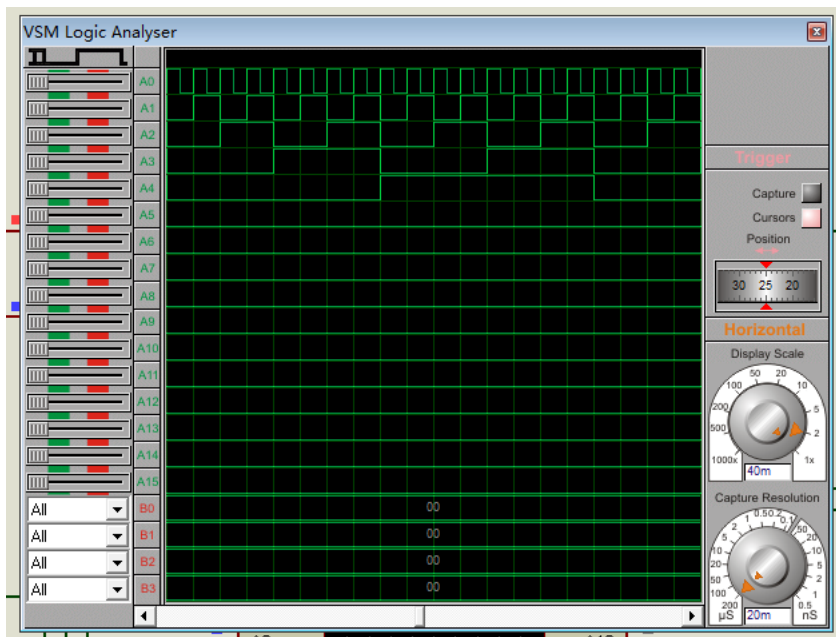
3 实验内容

3.1 用 JK 触发器设计一个 16 进制异步计数器

将前一个 JK 触发器的输出接到后一个 JK 触发器的 J 端和 K 端，则当前一个 JK 触发器输出的下降沿到达时，后一个 JK 触发器的输出反转。
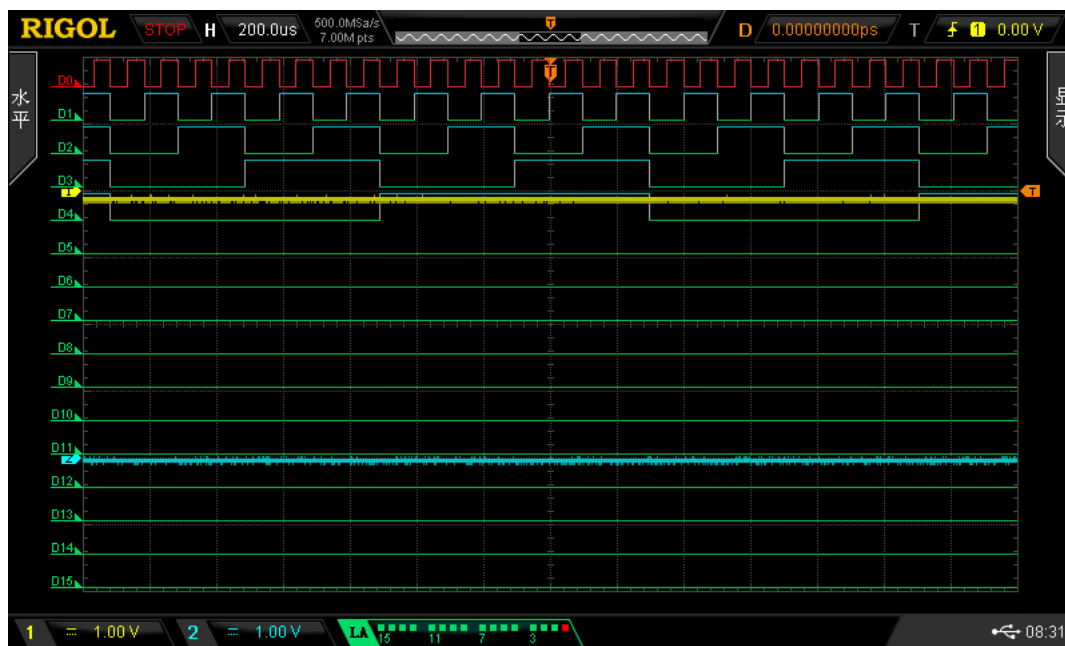
3.1.1 Proteus 实验设计

3.1.2 Proteus 逻辑分析仪

3.1.3 实验板实现——逻辑分析仪

3.2 用 JK 触发器设计一个 16 进制同步计数器

3.2.1 次态表

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

3.2.2 触发器转换表

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

3.2.3　卡诺图化简

J_0 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

K_0 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

J_1 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	1	X	X
10	0	1	X	X

K_1 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	1	0
10	X	X	1	0

J$_2$ map

Q$_3$Q$_2$ \ Q$_1$Q$_0$	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

K$_2$ map

Q$_3$Q$_2$ \ Q$_1$Q$_0$	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	0	0	1	0
10	X	X	X	X

J$_3$ map

Q$_3$Q$_2$ \ Q$_1$Q$_0$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

K$_3$ map

Q$_3$Q$_2$ \ Q$_1$Q$_0$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	0

3.2.4 驱动方程

$J_0 = 1$

$K_0 = 1$

$J_1 = Q_0$

$K_1 = Q_0$
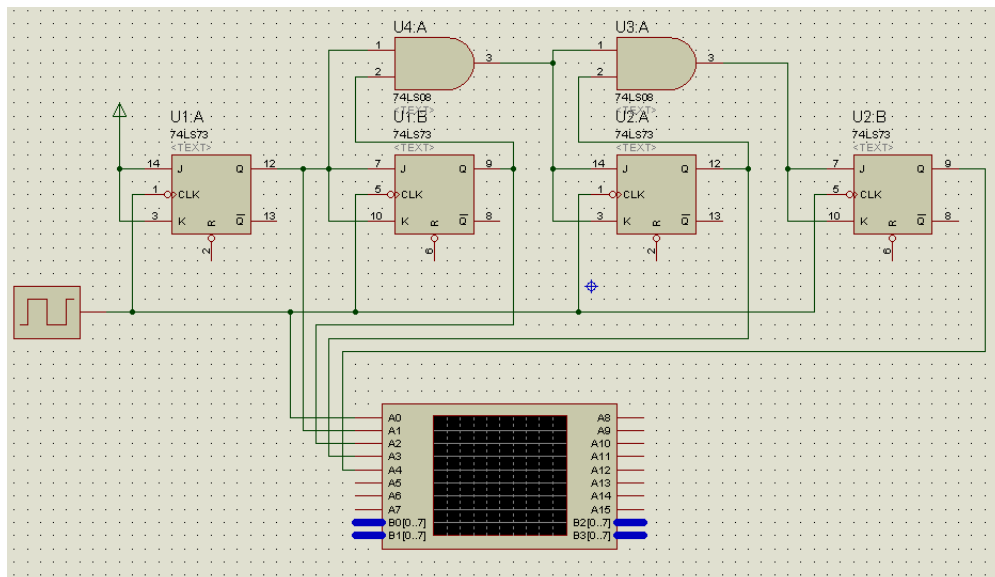
$J_2 = Q_1 \cdot Q_0$
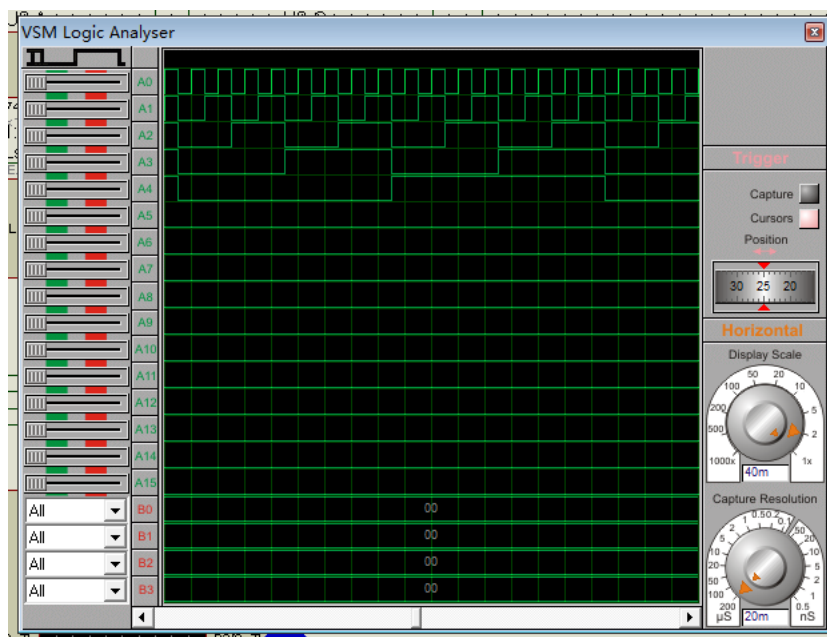
$K_2 = Q_1 \cdot Q_0$

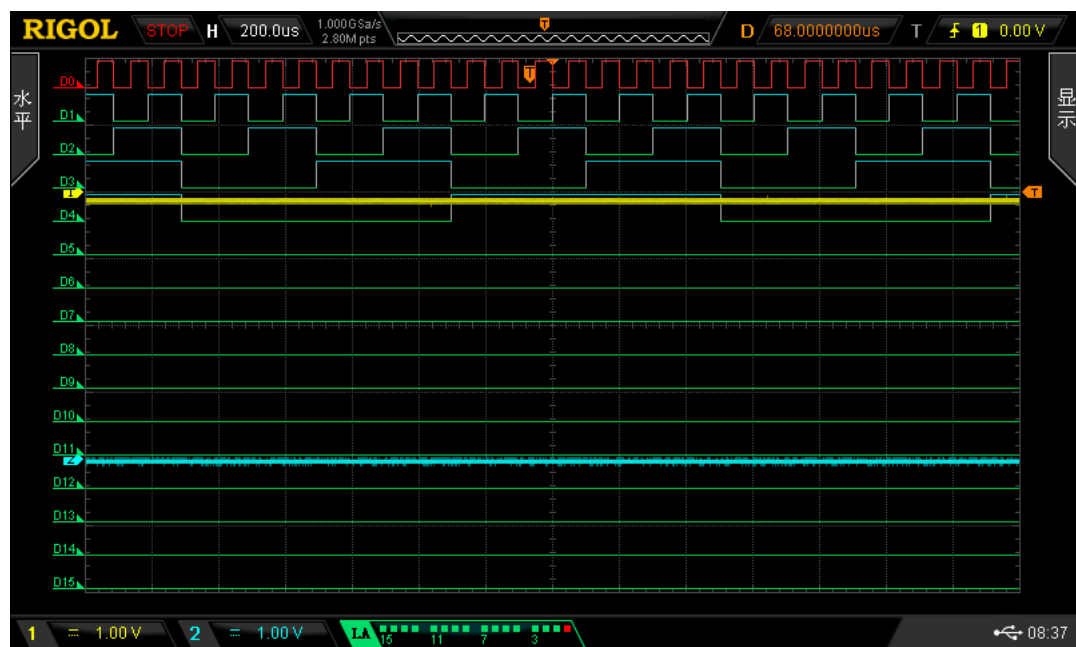$J_3 = Q_2 \cdot Q_1 \cdot Q_0$

$K_3 = Q_2 \cdot Q_1 \cdot Q_0$

3.2.5 电路图

3.2.6 Proteus 逻辑分析仪

3.2.7 实验板实现——逻辑分析仪

3.3 用 JK 触发器设计一个具有右移功能的计数器

3.3.1 次态表

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	D_{SR}	0	0	0
0	0	0	1	D_{SR}	0	0	0
0	0	1	0	D_{SR}	0	0	1
0	0	1	1	D_{SR}	0	0	1
0	1	0	0	D_{SR}	0	1	0
0	1	0	1	D_{SR}	0	1	0
0	1	1	0	D_{SR}	0	1	1
0	1	1	1	D_{SR}	0	1	1
1	0	0	0	D_{SR}	1	0	0
1	0	0	1	D_{SR}	1	0	0
1	0	1	0	D_{SR}	1	0	1
1	0	1	1	D_{SR}	1	0	1
1	1	0	0	D_{SR}	1	1	0
1	1	0	1	D_{SR}	1	1	0
1	1	1	0	D_{SR}	1	1	1
1	1	1	1	D_{SR}	1	1	1

3.3.2 触发器转换表

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

3.3.3 卡诺图化简

J_0 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	X	X	1
01	0	X	X	1
11	0	X	X	1
10	0	X	X	1

K_0 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	1	0	X
01	X	1	0	X
11	X	1	0	X
10	X	1	0	X

J_1 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	X	X
01	1	1	X	X
11	1	1	X	X
10	0	0	X	X

K_1 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	1	1
01	X	X	0	0
11	X	X	0	0
10	X	X	1	1

J_2 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	X	X	X	X
11	X	X	X	X
10	1	1	1	1

K_2 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01	1	1	1	1
11	0	0	0	0
10	X	X	X	X

J_3 map ($D_{SR} = 0$)

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

K_3 map ($D_{SR} = 0$)

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	1	1	1
10	1	1	1	1

J₃ map (D_SR = 1)

J$_3$ map (D$_{SR}$ = 1)

Q$_3$Q$_2$ \ Q$_1$Q$_0$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	X	X	X	X
10	X	X	X	X

K$_3$ map (D$_{SR}$ = 1)

Q$_3$Q$_2$ \ Q$_1$Q$_0$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	0	0
10	0	0	0	0

3.3.4 驱动方程

$J_0 = Q_1$
$K_0 = \overline{Q_1}$
$J_1 = Q_2$
$K_1 = \overline{Q_2}$
$J_2 = Q_3$
$K_2 = \overline{Q_3}$
$J_3 = D_{SR}$
$K_3 = \overline{D_{SR}}$

3.3.5 电路图
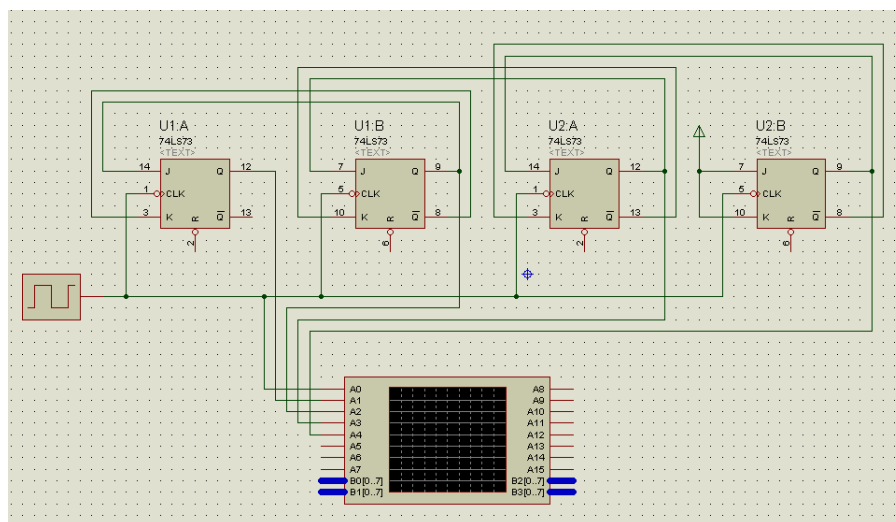
3.4 用 JK 触发器设计一个特殊的 12 进制同步计数器

3.4.1 状态转换图

$01 \rightarrow 02 \rightarrow 03 \rightarrow 04 \rightarrow 05 \rightarrow 06 \rightarrow 07 \rightarrow 08 \rightarrow 09 \rightarrow 10 \rightarrow 11 \rightarrow 12 \rightarrow 01 \rightarrow \cdots$

3.4.2 次态表

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	0	0	0	1

3.4.3 触发器转换表

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

3.4.4 卡诺图化简

J_0 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	X
10	1	X	X	1

K_0 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	X	X	X
10	X	1	1	X

J_1 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	X	X	X
10	0	1	X	X

K_1 map

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	X	X
10	X	X	1	0

J₂ map

Q₃Q₂ \ Q₁Q₀	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

K₂ map

Q₃Q₂ \ Q₁Q₀	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	1	0	1	0
10	X	X	X	X

J₃ map

Q₃Q₂ \ Q₁Q₀	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

K₃ map

Q₃Q₂ \ Q₁Q₀	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	X	X	X
10	0	0	0	0

3.4.5 驱动方程

$J_0 = 1$

$K_0 = 1$

$J_1 = Q_0$

$K_1 = Q_0$
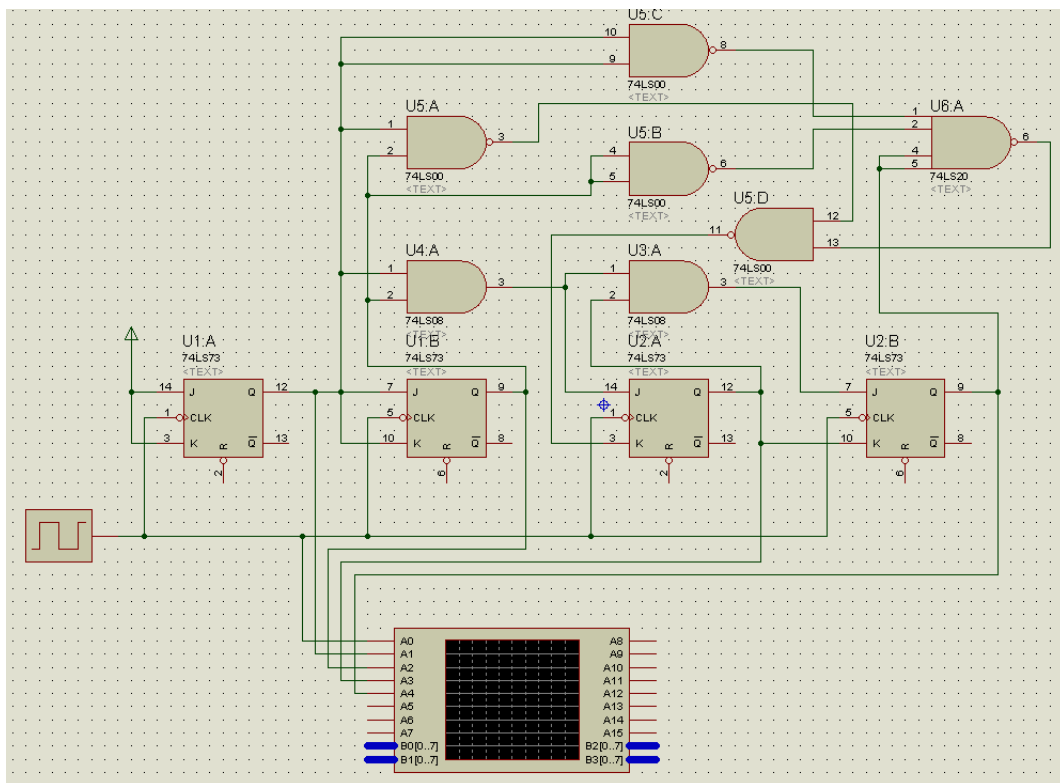
$J_2 = Q_1 \cdot Q_0$

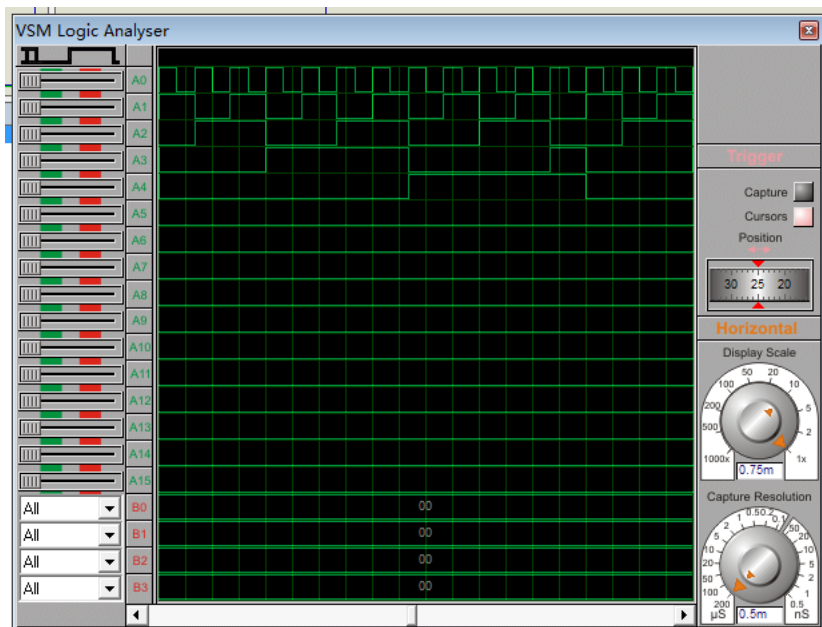$K_2 = Q_1 \cdot Q_0 + Q_3 \cdot \overline{Q_1} \cdot \overline{Q_0}$

$J_3 = Q_2 \cdot Q_1 \cdot Q_0$

$K_3 = Q_2$

3.4.6 电路图

3.4.7 Proteus 逻辑分析仪

3.4.8 实验板实现——逻辑分析仪