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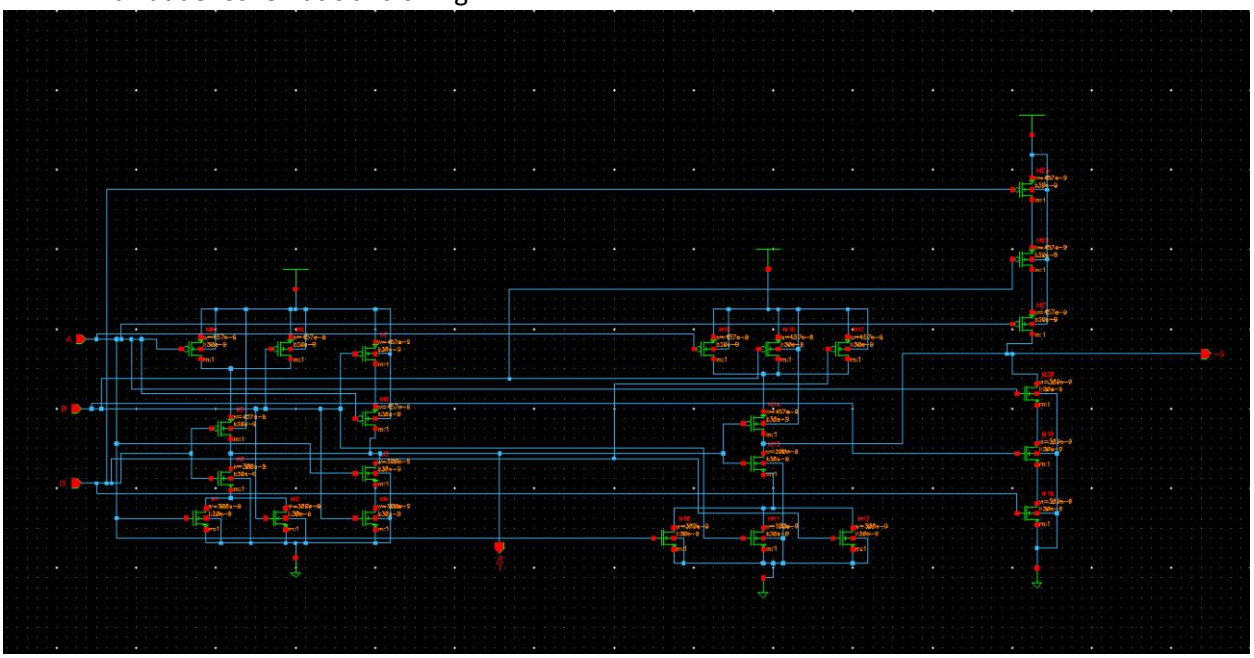
EEE 591

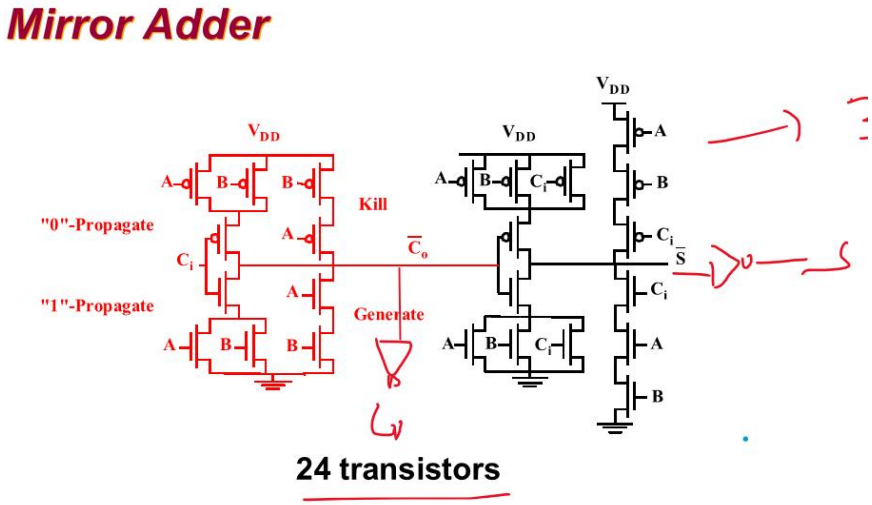
LAB #04

1. Full adder schematic and sizing



Nmos:300nm
Pmos:457nm

a. Explain the sizing criteria used



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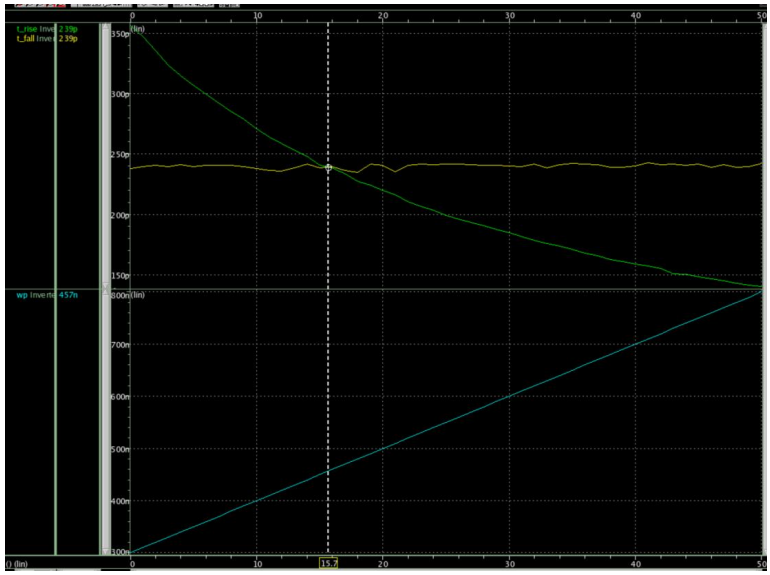
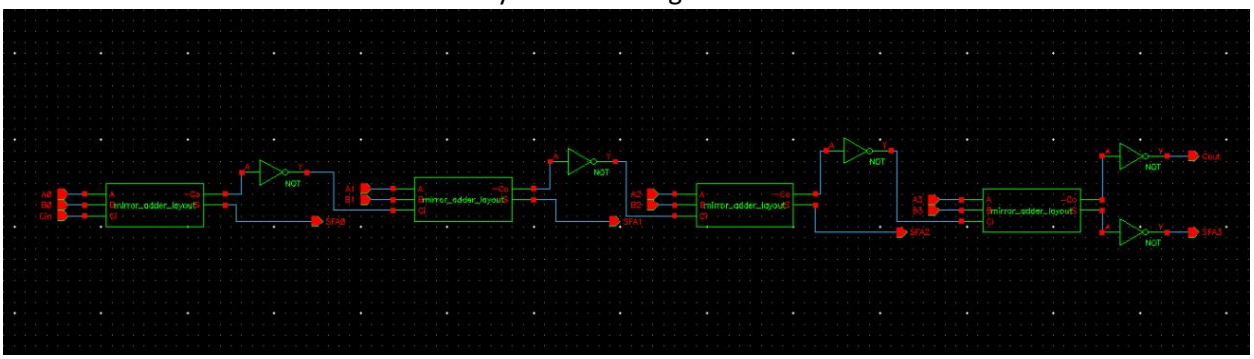


The minimum sized NMOS transistor you can use has WN = 300nm;I choose the mirror adder because it is easier to size the pmos transistor;all the pull-up network and pull-down network are symmetric;so I can sweep the pmos transistors sizes and get the suitable sizes to let Wp to match the LH and HL delay.

b. Provide the sizes (W/L) of all your transistors

All the nmos transistors:300nm; All the pmos transistors:457nm

c. Provide the schematic of your 4-bit design



d. Provide any scaling you choose to do for the 4-bit design and justification for the choice

I put the inverter outside the 1-bit adder design,and I just add the inverter to the Cout;I only have 5 inverters in my design.And it is easy to design and layout for the mirror_adder.

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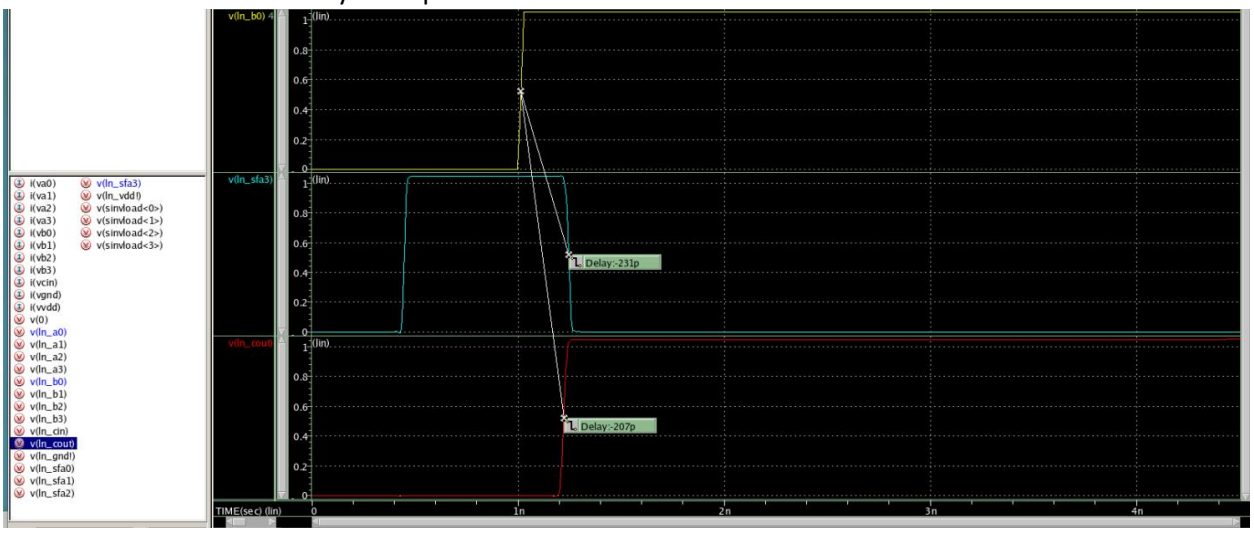
•**Simplicity**: The ripple-carry adder is easy to design and implement. It simply consists of a series of full adders (FA), each responsible for adding a bit from each operand along with a carry bit from the previous stage.

•**Low Hardware Cost**: Due to its simple design, the ripple-carry adder requires fewer components compared to other types of adders like carry-lookahead adders. It is cost-effective in terms of area and power consumption.

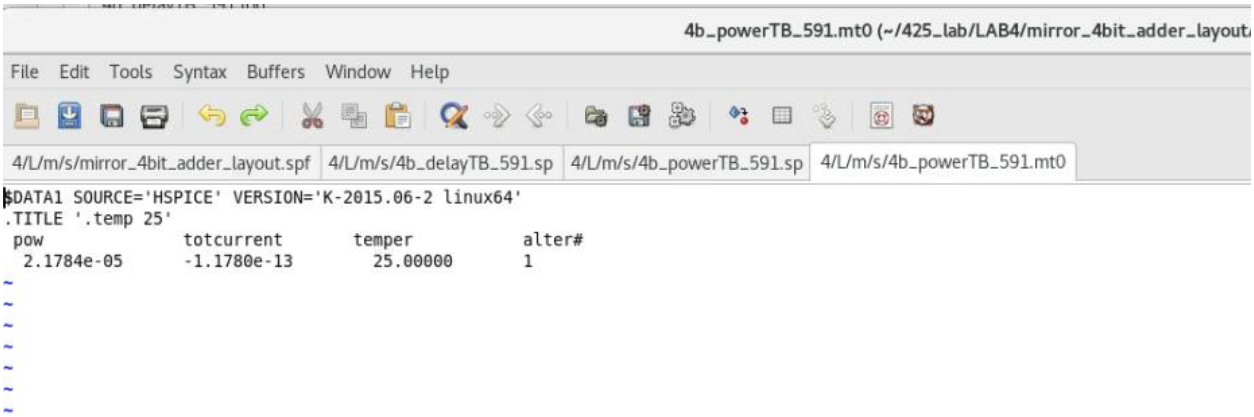
2. Simulation results
    a. Include the worst case delay plots

    Worst case delay = 231ps



    b. Include the power consumption analysis results

    Power=21.784uw



3. Include confirmation of
    a. Layout & DRC Pass

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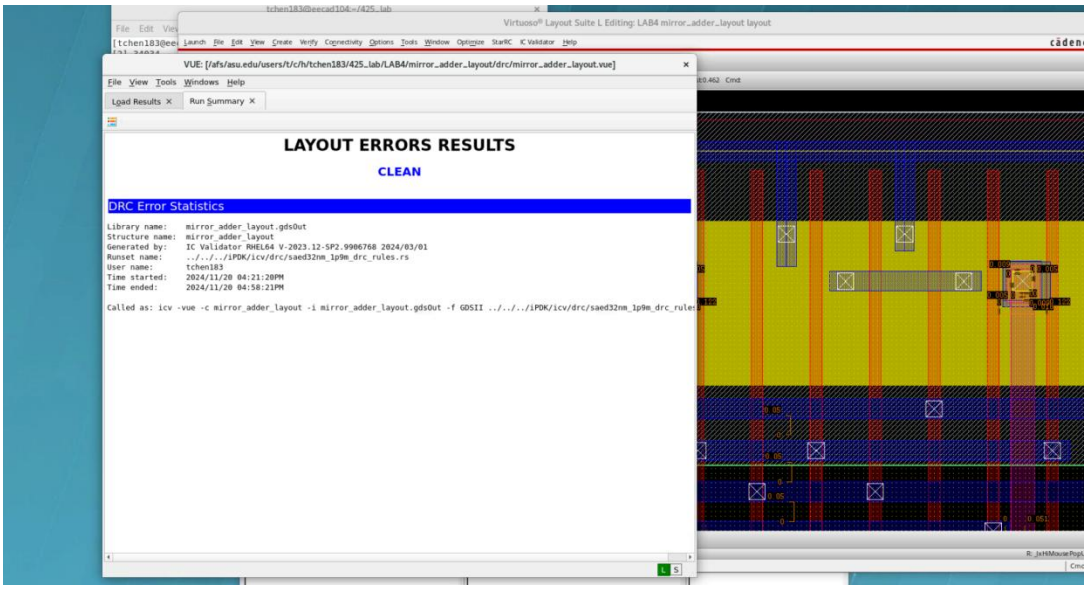

b. Layout & LVS Pass

4. Report the total area of your layout

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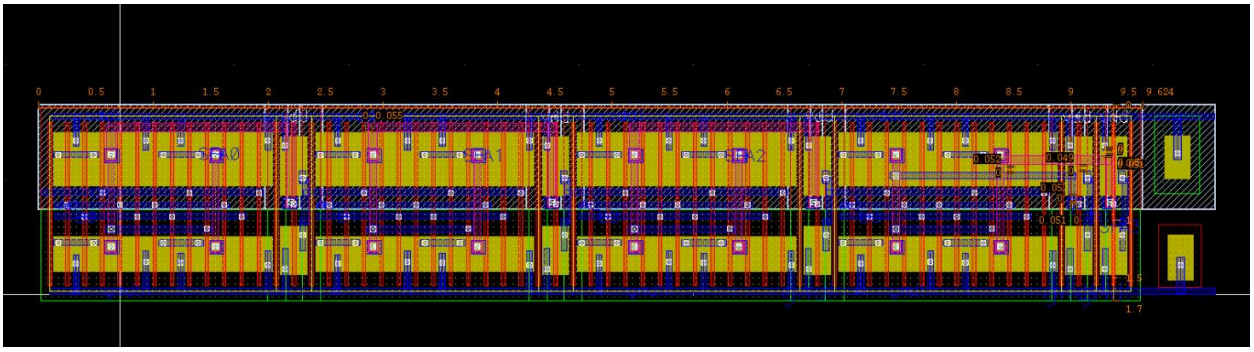


Width = 9.624um
Height =1.7um
Area = width * height = 16.3608um^2

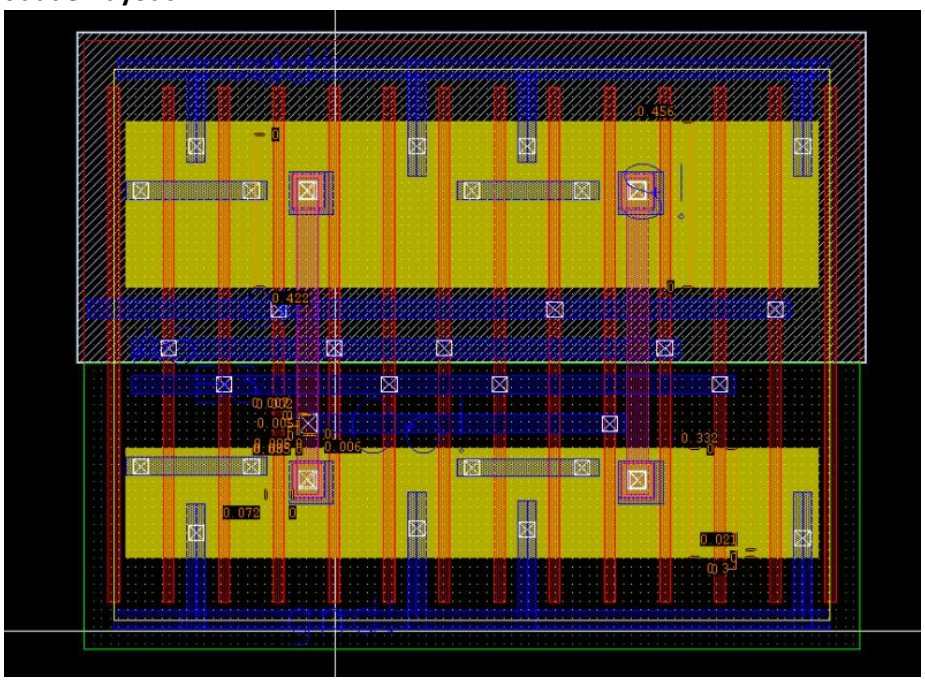
5. Report your overall score as outlined in the lab document

Score: The overall score for your design is calculated based on the following formula:

$$Score = \frac{400ps}{Delay} + \frac{100\mu W}{Power} + \frac{150\mu m^2}{Area}$$

Delay	231ps
Power	21.784uw
Area	16.3608um^2
Score	15.5

1-bit adder layout



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4-bit adder layout