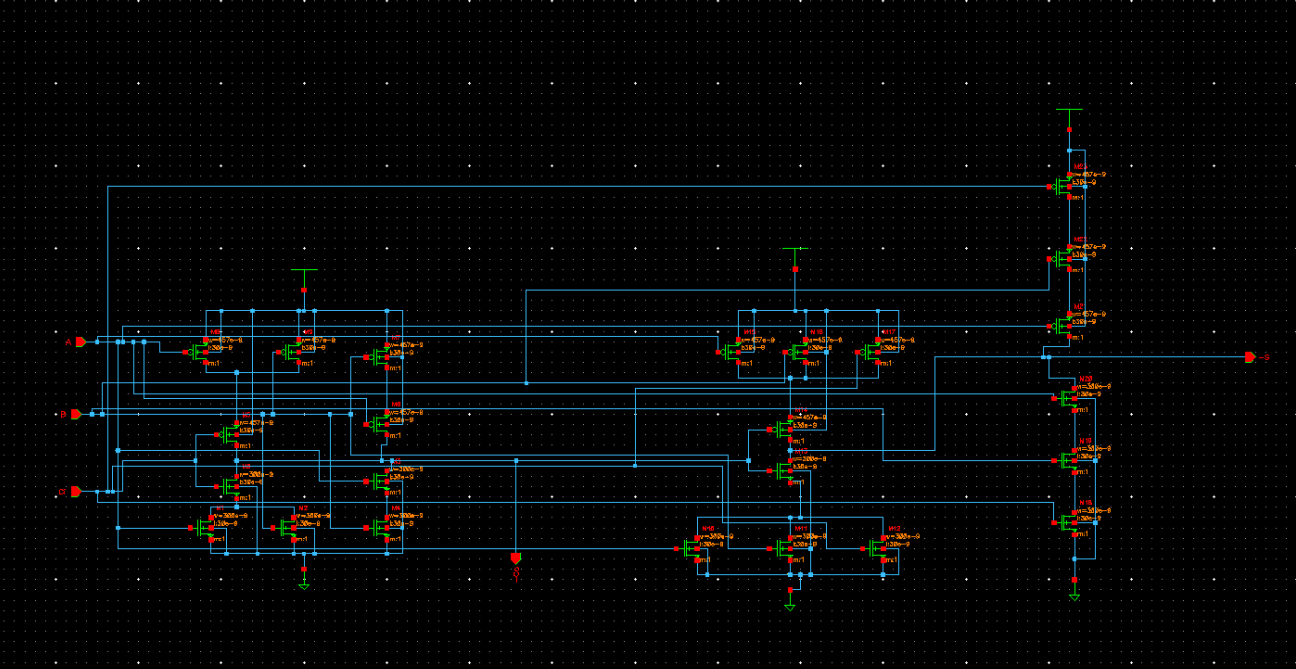
EEE 591

**LAB #04**

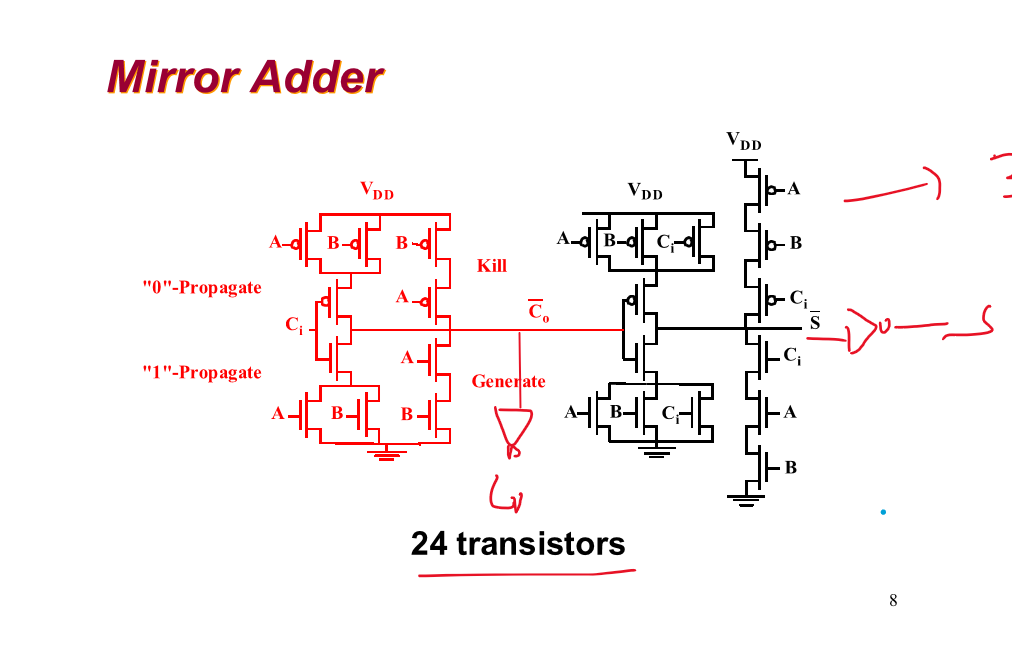
1. **Full adder schematic and sizing**

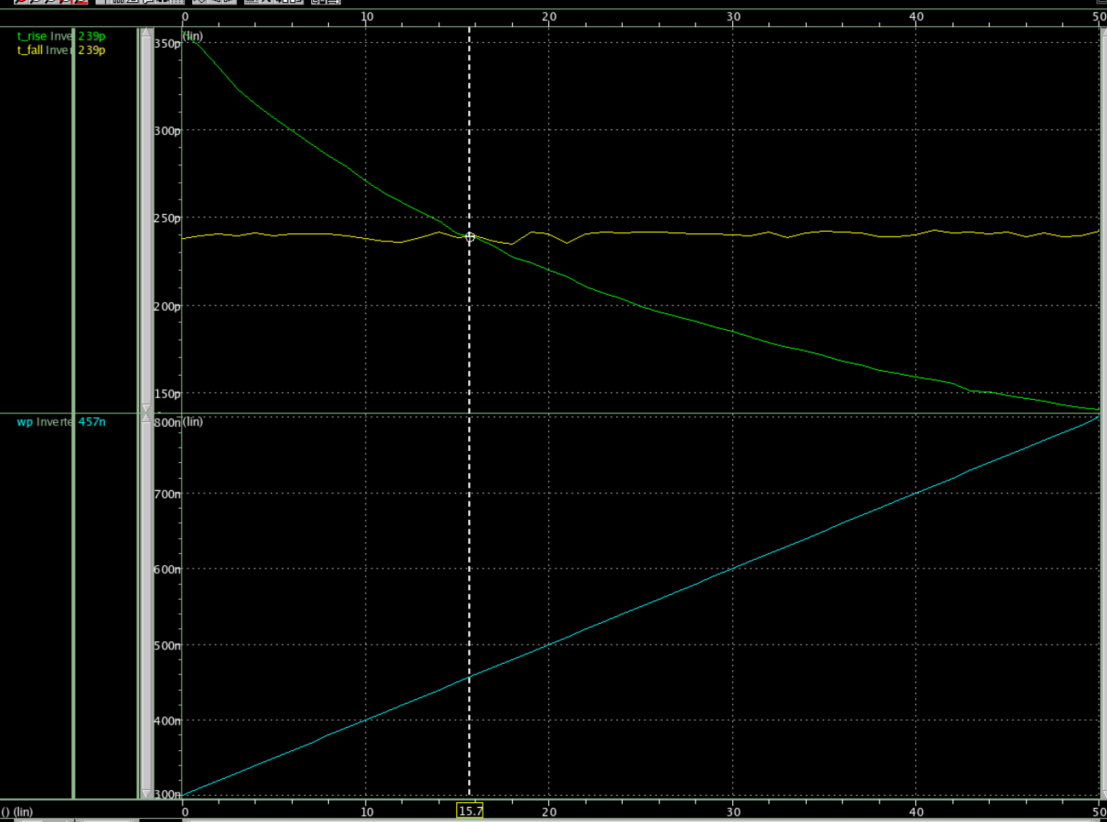
****

**Nmos:300nm**

**Pmos:457nm**

* 1. **Explain the sizing criteria used**



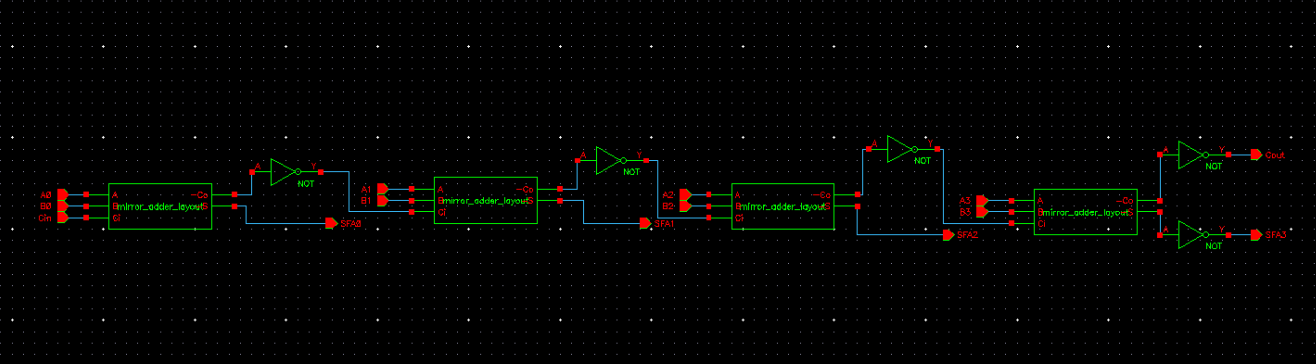
****

The minimum sized NMOS transistor you can use has WN = 300nm;I choose the mirror adder because it is easier to size the pmos transistor;all the pull-up network and pull-down network are symmetric;so I can sweep the pmos transistors sizes and get the suitable sizes to let Wp to match the LH and HL delay.

* 1. **Provide the sizes (W/L) of all your transistors**

**All the nmos transistors:300nm; All the pmos transistors:457nm**

* 1. **Provide the schematic of your 4-bit design**

****

* 1. **Provide any scaling you choose to do for the 4-bit design and justification for the choice**

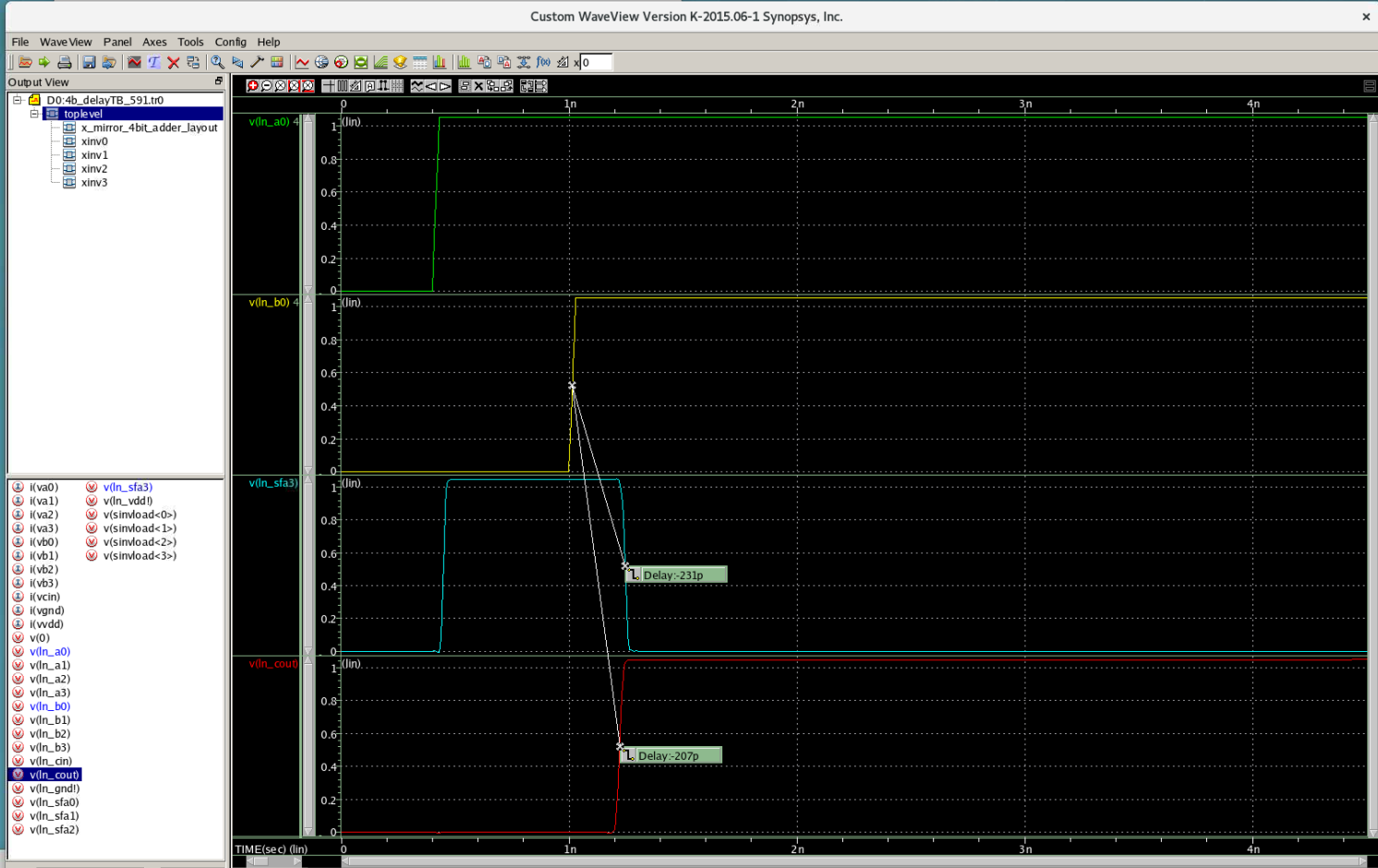
**I put the inverter outside the 1-bit adder design,and I just add the inverter to the Cout;I only have 5 inverters in my design.And it is easy to design and layout for the mirror\_adder.**

·**Simplicity**: The ripple-carry adder is easy to design and implement. It simply consists of a series of full adders (FA), each responsible for adding a bit from each operand along with a carry bit from the previous stage.

·**Low Hardware Cost**: Due to its simple design, the ripple-carry adder requires fewer components compared to other types of adders like carry-lookahead adders. It is cost-effective in terms of area and power consumption.

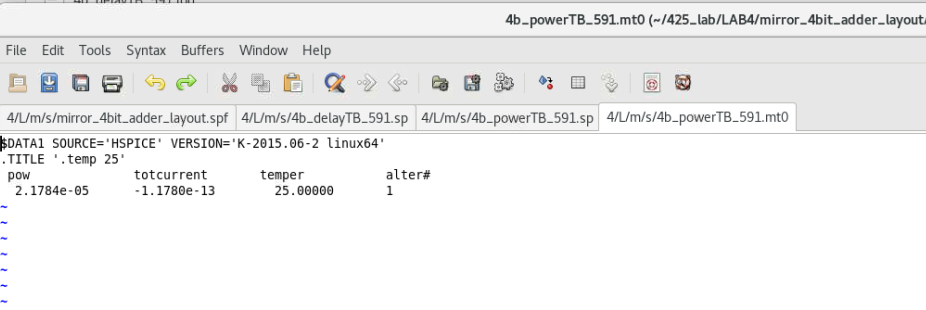
1. **Simulation results**
   1. **Include the worst case delay plots**

**Worst case delay = 231ps**

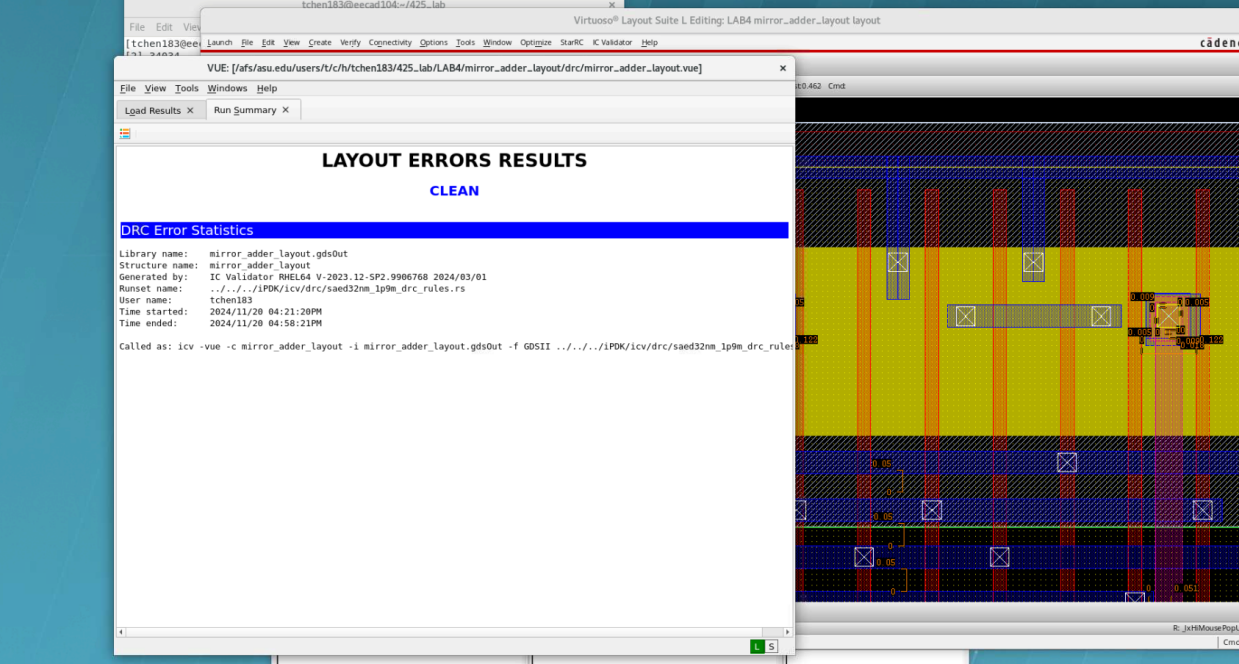
****

* 1. **Include the power consumption analysis results**

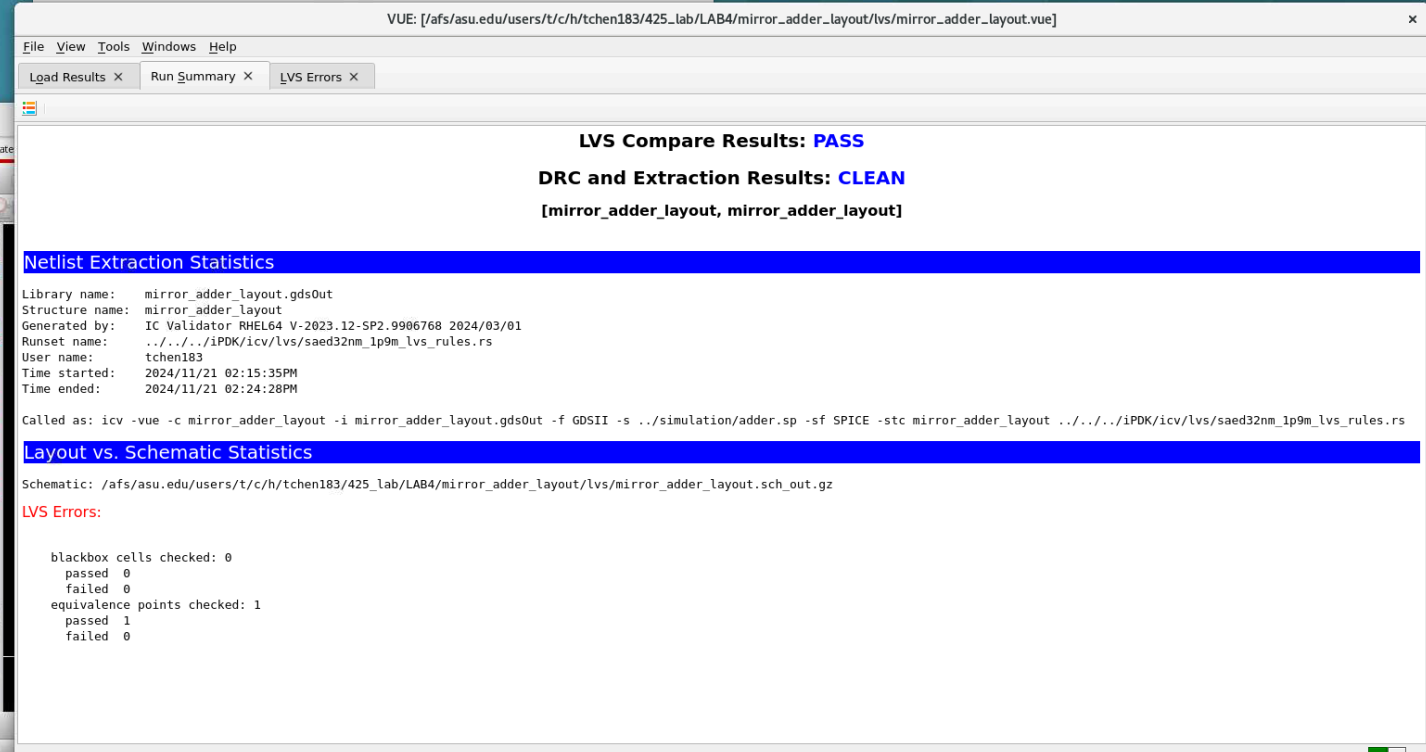
**Power=21.784uw**

****

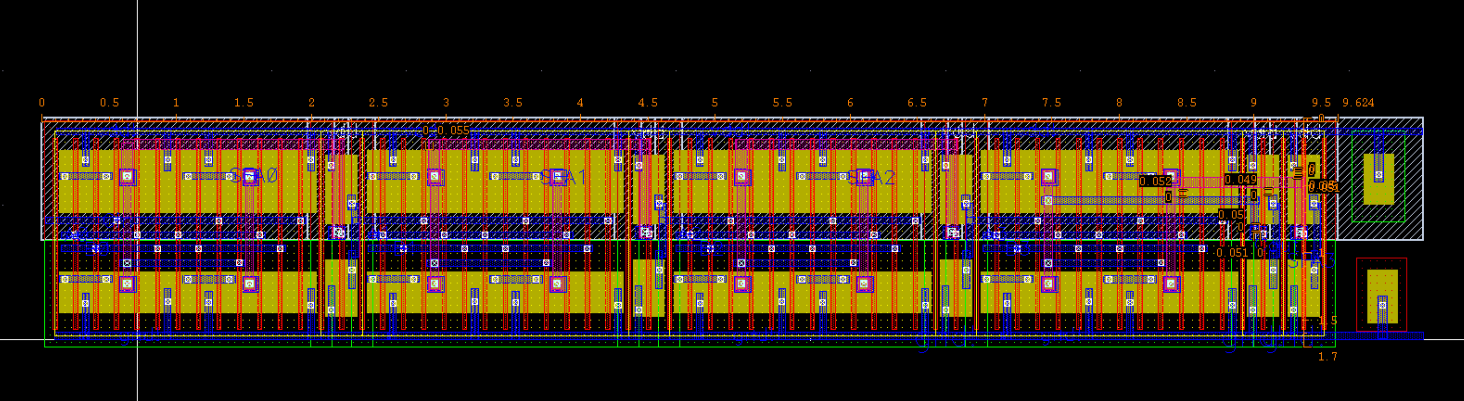
1. **Include confirmation of** 
   1. **Layout & DRC Pass**

****

* 1. **Layout & LVS Pass**

****

1. **Report the total area of your layout**

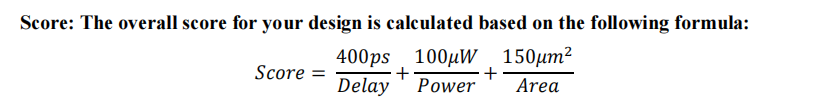
****

**Width = 9.624um**

**Height =1.7um**

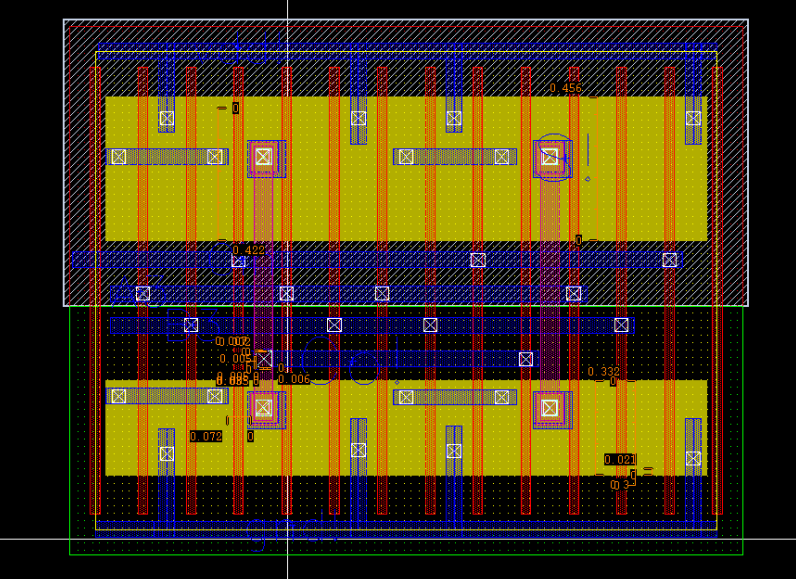
**Area = width \* height = 16.3608um^2**

1. **Report your overall score as outlined in the lab document**

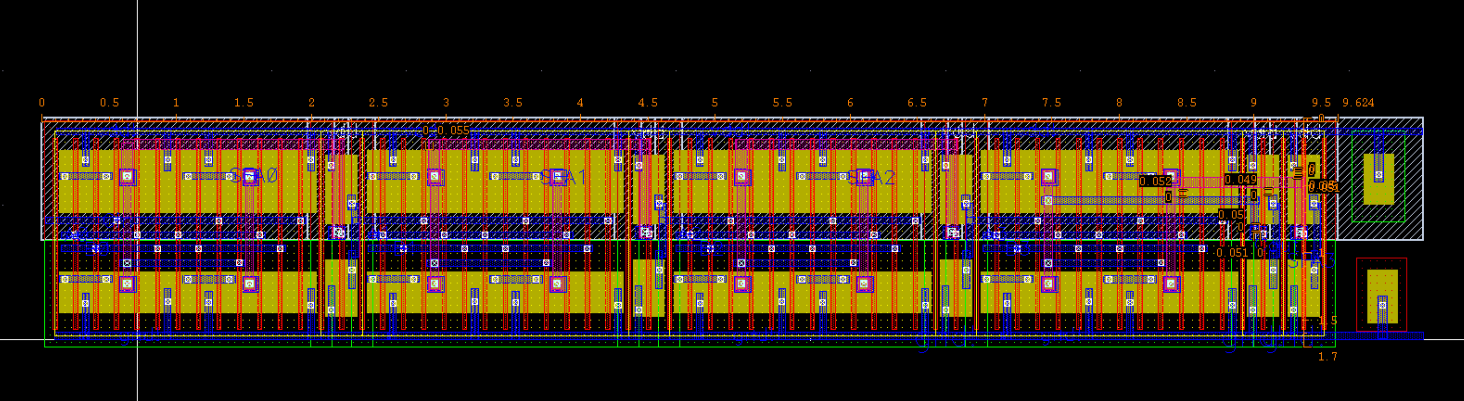


|  |  |
| --- | --- |
| Delay | 231ps |
| Power | 21.784uw |
| Area | 16.3608um^2 |
| Score | 15.5 |

**1-bit adder layout**

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**4-bit adder layout**

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