Yung-Chin (Jim) Chen

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Research Interests

VLSI Designs, Computer Architecture, In-memory Computing Processor, NN Accelerator

Education

Princeton University — Princeton, NJ, USA
Ph.D. student in Electrical and Computer Engineering (ECE) — *Sep 2024 - Present*
- GPA to date: 4.0 / 4.0

National Taiwan University (NTU) — Taipei, Taiwan
Bachelor of Science in Electrical Engineering (EE) — *Sep 2019 – Jan 2024*
- Phi Tau Phi Honorary Member (for top 1% of college graduates), Major GPA: 4.28 / 4.30

Keio University — Tokyo, Japan
Exchange Student with Full Scholarship — *Oct 2022 – Jul 2023*

Research Experience

PhD Student at Verma Lab — Jan 2025 – Now
Princeton University (Advisor: Prof. Naveen Verma) — *Princeton, NJ, USA*
- Researching on In-memory Computing (IMC) systems and architectures

Visiting RA at Computing and Sensing Group — Sep 2022 – Feb 2024
Keio University (Advisor: Prof. Kentaro Yoshioka) — *Kanagawa, Japan*
- Researched on saliency-aware IMC macro for Neural Network (NN)
- Researched on memory-centric algorithm-architecture co-design for novel NN framework

Undergrad RA at Energy-Efficient Circuits and Systems Lab — Sep 2021 – Feb 2024
National Taiwan University (Advisor: Prof. Tsung-Te Liu) — *Taipei, Taiwan*
- Taped out a 28nm SRAM CIM-based accelerator for end-to-end NN inference

Publications

[1] W. Zhang, S. Ando, **Yung-Chin Chen**, K. Yoshioka, "ASiM: Modeling and Analyzing Inference Accuracy of SRAM-Based Analog CiM Circuits", *in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2025*

[2] S. Ando, S. Miyagi, W. Zhang, **Yung-Chin Chen**, K. Yoshioka, "A 4541 TOPS/W Saliency-Aware Analog Computing In-Memory Macro with Charge-Domain Saliency Detector", *in IEEE European Solid-State Electronics Research Conference (ESSERC), 2025*

[3] **Yung-Chin Chen**, S. Ando, D. Fujiki, S. Takamaeda-Yamazaki, K. Yoshioka, "OSA-HCIM: On-The-Fly Saliency-Aware Hybrid SRAM CIM with Dynamic Precision Configuration", *in Asia and South Pacific Design Automation Conference (ASP-DAC), 2024*

[4] W. Zhang, S. Ando, **Yung-Chin Chen**, S. Miyagi, S. Takamaeda-Yamazaki, K. Yoshioka, "PaCiM: A Sparsity-Centric Hybrid Compute-in-Memory Architecture via Probabilistic Approximation", *in International Conference on Computer-Aided Design (ICCAD), 2024*

[5] **Yung-Chin Chen**, S. Ando, D. Fujiki, S. Takamaeda-Yamazaki, K. Yoshioka, "HALO-CAT: A Hidden Network Processor with Activation-Localized CIM Architecture and Layer-Penetrative Tiling", *on arXiv*

[6] S. Ando, **Yung-Chin Chen**, S. Miyagi, W. Zhang, K. Yoshioka, "A Saliency-Aware Analog Computing-In-Memory Macro with SAR-Embedded Saliency Detection Technique", *In International Conference on Solid State Devices and Materials (SSDM), 2024*

[7] K. Yoshioka, S. Ando, S. Miyagi, **Yung-Chin Chen**, W. Zhang, "Towards Efficient and Precise Analog Compute-in-Memory Circuits", *In International Conference on Solid State Devices and Materials (SSDM), 2024 (Invited)*

[8] K. Yoshioka, S. Ando, S. Miyagi, **Yung-Chin Chen**, W. Zhang, "A Review of SRAM-based Compute-in-Memory Circuits", *in Japanese Journal of Applied Physics (JJAP), 2024*

[9] S. Ando, **Yung-Chin Chen**, S. Miyagi, W. Zhang, K. Yoshioka, "A Saliency-Aware Analog Computing In-Memory with SAR-Embedded Detection Achieving 18.5% Power Reduction", *in Japanese Journal of Applied Physics (JJAP), 2024*

Honors and Awards

Irving T. Ho Memorial Scholarship - EE dept. at NTU	Dec 2022
The Memorial Scholarship Foundation to Lin Hsiung Chen (acc. rate: 2%)	Nov 2022
Research Grant - National Science and Technology Council (NSTC), Taiwan	Jul 2022 – Jan 2023
Research Grant - Taiwan Semiconductor Manufacturing Co., Ltd (TSMC)	Feb 2022 – Jun 2022
1st Place (Best Solver Award) - MakeNTU - largest student maker hackathon in Taiwan	Mar 2022
Principal Award - Awarded to top 2% NTUEE students for their academic excellences	Dec 2022

Teaching Experience

TA in Design of VLSI Systems, lectured by Prof. Naveen Verma	Sep 2025 – Dec 2026
TA in Computer Architectures, lectured by Prof. Tsung-Te Liu	Sep 2023 – Jan 2024
TA in EECS Lab Undergraduate Research, supervised by Prof. Tsung-Te Liu	Sep 2023 – Jan 2024
TA in Signal and Systems, lectured by Prof. Lin-Shan Lee	Feb 2022 – Jun 2022

Technical Skills

Programming: Verilog, System Verilog, Python, C++, MATLAB
IC Design Tools: NC-Verilog, Design Compiler, Innovus, Virtuoso, HSPICE, FPGA
Toolbox: PyTorch, TensorFlow, NumPy, LaTeX
Languages: Chinese (Native), English, Japanese

Activities

Vice President of Princeton Association of Taiwanese Students	Sep 2025 – Now
Compulsory Military Service in Taiwan	Mar 2024 – Jun 2024
Student Ambassador of National Taiwan University	Oct 2021 – Sep 2022
Vice Captain of NTUEE Baseball Team	Sep 2021 – Aug 2022
Vice President of NTU Escape Room and Puzzle Solving Club	Aug 2020 – Jul 2021