Yung-Chin (Jim) Chen

jim.chen.work@gmail.com yung-chin-jim-chen Chenyungchin chenyungchin.github.io

RESEARCH INTERESTS

AI Processor, Memory-centric Architectures, Hardware-friendly Algorithms for Neural Networks (NN), Computing-In-Memory (CIM) circuits, Computer Architectures

EDUCATION

B.S, Electrical Engineering (EE) Sep 2019 - Present

National Taiwan University, (NTU) Phi Tau Phi Honorary Member (for **top 1%** of college graduates)

Major GPA: **4.28** / 4.3, Overall GPA: **4.25** / 4.3, Rank: **4th** / 264 **(2%)**

RESEARCH EXPERIENCE

Computing and Sensing Group (Prof. Kentaro Yoshioka), Keio Univ., Japan Sep 2022 - Present

Computing-In-Memory (CIM) Macro for NN - with UTokyo **[1]**

- Proposed a **hybrid CIM macro** with concurrent digital & analog computation, providing a flexible trade-off between efficiency and accuracy
- Proposed a **saliency-aware framework** that dynamically allocates the computation into digital and analog domains based on the importance of the inputs, achieving a 1.95x energy efficiency gain

Hidden Network (HNN) Algorithm/Architecture Co-design - with UTokyo **[2]**

- Proposed **Layer-Penetrative Tiling (LPT)**, a significantly enhanced cross-layer computation algorithm for HNN, reducing the size of intermediate activation by 26x
- Designed an **end-to-end HNN CIM processor** capable of executing huge networks (ResNet50@ImageNet) with a mere 72KB activation memory, demonstrating a 14.2x reduction in memory size
- Proposed an **activation-localized (AL) dataflow** that preserves the locality between output and input activations, leading to a 1.6x reduction in the number of activation accesses
- Devised a **compact CIM macro** that reuses capacitors for both MAC computation and A/D conversion

Energy-Efficient Circuits and Systems (EECS) Lab (Prof. Tsung-Te Liu), NTU Sep 2021 - Present

End-to-End CIM Processor for NN - with TSMC and MediaTek **[3]**

- Designed an SRAM CIM processor with a **flexible input buffer** to maintain high data reuse under various dataflows and maximize hardware utilization rate among diverse input topologies
- Taped out a 28nm chip and achieved SOTA efficiencies of 1081.1 GOPS/mm^2 and 51.4 TOPS/W

PUBLICATIONS

[1] **Yung-Chin Chen**, S. Ando, D. Fujiki, S. Takamaeda-Yamazaki, K. Yoshioka, "OSA-HCIM: On-The-Fly Saliency-Aware Hybrid SRAM CIM with Dynamic Precision Configuration", ASP-DAC 2024

[2] **Yung-Chin Chen**, S. Ando, D. Fujiki, S. Takamaeda-Yamazaki, K. Yoshioka, "HALO-CAT: A Hidden Network Processor with Activation-Localized CIM Architecture and Layer-Penetrative Tiling", DAC 2024 **(Under Review)**

[3] T.-Y. Wu*, Y.-H. Pan*, **Yung-Chin Chen***, W.-C. Tseng* et al., "N2N-BP^{2}CIM: A 28nm 1018.1GOPS/mm^2 End-to-End Bit-Parallel, Bit-Parallel Computing-in-Memory DNN Processor with High-Bandwidth 14T-SRAM Bitcell", VLSI Symposium 2024 **(Submitted) (* denotes equally credited authors)**

HONORS AND AWARDS

Irving T. Ho Memorial Scholarship - EE dept. at NTU (~1300USD) *Dec 2022*

The Memorial Scholarship Foundation to Lin Hsiung Chen (~4800USD, acc. rate: 2%) *Nov 2022*

Research Grant - National Science and Technology Council (NSTC), Taiwan *Jul 2022 - Jan 2023*

Research Grant - Taiwan Semiconductor Manufacturing Co., Ltd (TSMC) *Feb 2022 - Jun 2022*

1st Place (Best Solver Award), MakeNTU - largest nationwide student maker hackathon *Mar 2022*

SELECTED PROJECTS

180nm ASIC chip for American Option Pricing Using Monte-Carlo Method (🔗) Verilog, Innovus

- Taped out a chip for American option pricing, attaining a 500x speedup compared to CPU benchmark
- Implemented a Monte-Carlo core with Sobol RNG for cash flow matrix simulation

Fully Motion-Controlled Doodle Jump Game on FPGA (🔗) Verilog, System Verilog, FPGA

- Designed a fully motion-controlled interactive game with player's hands and voice using FPGA
- Implemented DSP modules for motion and gesture recognition and realized real-time gaming display

WORKING EXPERIENCE

TA in Computer Architectures, lectured by Prof. Tsung-Te Liu Sep 2023 - Present

- Designed Verilog assignments including ALU, CPU, and Cache and delivered programming tutorials

TA in EECS Lab Undergraduate Research, supervised by Prof. Tsung-Te Liu Sep 2023 - Present

- Guided new lab members through the paper survey of CIM and relevant circuit simulation
- Established training courses for circuit design tools, encompassing HSPICE, Verilog, and Virtuoso

TA in Signal and Systems, lectured by Prof. Lin-Shan Lee Feb 2022 - Jun 2022

- Delivered MATLAB lectures, held weekly problem-solving seminars, and graded homework and exams

TECHNICAL SKILLS

Programming: Verilog, System Verilog, Python, C++, MATLAB

IC Design Tools: NC-Verilog, Design Compiler, Innovus, Virtuoso, HSPICE, FPGA

Languages: Chinese (Mandarin), English (TOEFL: MyBest 111/120, GRE: 333/340), Japanese (JLPT N1)

Toolbox: PyTorch, NumPy, LaTeX

ACTIVITIES

One-year Exchange Student at Keio University, Japan Oct 2022 - Sep 2023

- Accumulated extensive experience in cross-cultural learning and communication with foreigners

Student Ambassador of NTU Oct 2021 - Sep 2022

- Introduced Taiwan to foreign visitors, orchestrated international events, and guided campus tours
- Provided support for the integration of international scholars into Taiwanese life

Vice Captain of NTUEE Baseball Team Sep 2021 - Aug 2022

- Led and coached a team of 20+ players; provided personalized instructions and training menus

Vice President of NTU Escape Room and Puzzle Solving Club Aug 2020 - Jul 2021

- Led a club of 30+ members to design engaging puzzles and develop reality games
- Held 3 school-wide real escape games, attracting over 200 participants