YUNG-CHIN (JIM) CHEN

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EDUCATION

B.S, Electrical Engineering (EE) Sep 2019 - Present
National Taiwan University, (NTU) Phi Tau Phi Honorary Member (for **top 1%** of college graduates)
major GPA: **4.28** / 4.3, **overall GPA**: **4.25** / 4.3, **Rank**: **4th** / 264

RESEARCH EXPERIENCE

Energy-Efficient Circuits and Systems (EECS) Lab (Prof. Tsung-Te Liu), NTU Sep 2021 – Present

Computing-in-Memory (CIM) Neural Network Processor [2] - with TSMC and MediaTek

- Designed a bit-parallel, bit-parallel (BP^2) end-to-end CIM processor using 14T4x-bandwidth SRAM bit-cell, achieving state-of-the-art efficiencies of 1081.1 GOPS/mm^2 and 51.4 TOPS/W in chip performance

Computing and Sensing Group (Prof. Kentaro Yoshioka), Keio Univ., Japan Sep 2022 – Present

Macro Level Hybrid CIM [1] - with S. Takamaeda-Yamazaki (UTokyo) and D. Fujiki (Keio)

- Proposed a hybrid domain CIM macro and a saliency-aware framework that dynamically configures the computation ratio between DCIM and ACIM, achieving a 1.95x energy efficiency gain

PUBLICATIONS

[1] **Yung-Chin Chen** et al., "OSA-HCIM: On-The-Fly Saliency-Aware Hybrid SRAM CIM with Dynamic Precision Configuration", ASP-DAC 2024
[2] T.-Y. Wu*, Y.-H. Pan*, **Yung-Chin Chen***, W.-C. Tseng* et al., "N2N-BP^2CIM: A 28nm 1018.1GOPS/mm^2 End-to-End Bit-Parallel, Bit-Parallel Computing-in-Memory DNN Processor with High-Bandwidth 14T-SRAM Bitcell", ISSCC 2024 **(Under Review) (* denotes ECAs)**

HONORS AND AWARDS

Honorary Member, awarded to **top 1%** college graduates - The Phi Tau Phi Scholastic Society *Jun 2023*
Irving T. Ho Memorial Scholarship- EECS College at NTU *Dec 2022*
The Memorial Scholarship Foundation to Lin Hsiung Chen, acceptance rate: 2% *Nov 2022*
Undergraduate Research Grant - Ministry of Science and Technology, Taiwan *Jul 2022 - Jan 2023*

SELECTED PROJECTS

180nm ASIC chip for American Option Pricing Using Monte-Carlo Method (🔗) Verilog, Innovus
Hand-Motion-Controlled Doodle Jump Game on FPGA (🔗) Verilog, System Verilog, FPGA

WORKING EXPERIENCE

TA of Computer Architectures, lectured by Prof. Tsung-Te Liu Sep 2023 - Present
TA of EECS Lab Undergraduate Research, supervised by Prof. Tsung-Te Liu Sep 2022 - Present
TA of Signal and Systems, lectured by Prof. Lin-Shan Lee Feb 2022 - Jun 2022
Secondary Reviewer - ISSCC 2023, VLSI Symposium 2023, ISSCC 2024

TECHNICAL SKILLS

Programming: Verilog, System Verilog, Python, C++, Matlab
IC Design Tools: NC-Verilog, Design Compiler, Innovus, Virtuoso, HSPICE, FPGA
Languages: Chinese, English (TOEFL: 110/120, GRE: 333/340), Japanese (JLPT N1 passed)
Toolbox: Pytorch, NumPy, Latex