Yung-Chin (Jim) Chen

yc9182@princeton.edu | LinkedIn | Homepage | Google Scholar

Education

Princeton University — Princeton, NJ, USA
First-year Ph.D. student in Electrical and Computer Engineering — *Sep 2024 - Present*

National Taiwan University — Taipei, Taiwan
Bachelor of Science in Electrical Engineering — *Sep 2019 – Jan 2024*
- Phi Tau Phi Honorary Member (for top 1% of college graduates), Major GPA: 4.28 / 4.30

Keio University — Tokyo, Japan
Exchange Student with Full JASSO Scholarship — *Oct 2022 – Jul 2023*

Research Experience

Research Assistant at Computing and Sensing Group — Sep 2022 – Feb 2024
Keio University (Advisor: Prof. Kentaro Yoshioka) — *Kanagawa, Japan*
- Researched on saliency-aware Computing-In-Memory (CIM) macro for Neural Network (NN). **[1]-[3]**
- Researched on memory-centric algorithm-architecture codesign for novel NN framework. [***arXiv***]

Research Assistant at Energy-Efficient Circuits and Systems Lab — Sep 2021 – Feb 2024
National Taiwan University (Advisor: Prof. Tsung-Te Liu) — *Taipei, Taiwan*
- Taped out a 28nm SRAM CIM-based accelerator for end-to-end NN inference.

Publications

[1] **Yung-Chin Chen**, S. Ando, D. Fujiki, S. Takamaeda-Yamazaki, K. Yoshioka, "OSA-HCIM: On-The-Fly Saliency-Aware Hybrid SRAM CIM with Dynamic Precision Configuration", *ASP-DAC 2024*

[2] W. Zhang, S. Ando, **Yung-Chin Chen**, S. Miyagi, S. Takamaeda-Yamazaki, K. Yoshioka, "PaCiM: A Sparsity-Centric Hybrid Compute-in-Memory Architecture via Probabilistic Approximation", *ICCAD 2024 (to appear)*

[3] S. Ando, **Yung-Chin Chen**, S. Miyagi, W. Zhang, K. Yoshioka, "A Saliency-Aware Analog Computing-In-Memory Macro with SAR-Embedded Saliency Detection Technique", *SSDM 2024 (to appear)*

Projects

180nm ASIC chip for American Option Pricing Using Monte-Carlo Method | Verilog, Innovus
- Taped out a chip for American option pricing, attaining a 500x speedup compared to CPU benchmark

Fully Motion-Controlled Doodle Jump Game on FPGA | Verilog, System Verilog, FPGA
- Designed a fully motion-controlled interactive game with player's hands and voice using FPGA

Honors and Awards

Irving T. Ho Memorial Scholarship - EE dept. at NTU — Dec 2022
The Memorial Scholarship Foundation to Lin Hsiung Chen (acc. rate: 2%) — Nov 2022
Research Grant - National Science and Technology Council (NSTC), Taiwan — Jul 2022 – Jan 2023
Research Grant - Taiwan Semiconductor Manufacturing Co., Ltd (TSMC) — Feb 2022 – Jun 2022

Teaching Experience

TA in Computer Architectures, lectured by Prof. Tsung-Te Liu — Sep 2023 – Jan 2024
TA in EECS Lab Undergraduate Research, supervised by Prof. Tsung-Te Liu — Sep 2023 – Jan 2024
TA in Signal and Systems, lectured by Prof. Lin-Shan Lee — Feb 2022 – Jun 2022

Technical Skills

Programming: Verilog, System Verilog, Python, C++, MATLAB
IC Design Tools: NC-Verilog, Design Compiler, Innovus, Virtuoso, HSPICE, FPGA
Toolbox: PyTorch, NumPy, LaTeX
Languages: Chinese (Native), English (TOEFL: 110, GRE: 333), Japanese (JLPT N1)