




# Yung-Chin (Jim) Chen

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## RESEARCH INTERESTS

**AI Processor, Memory-centric Architectures, Hardware-friendly Algorithms for Neural Networks (NN), Computing-In-Memory (CIM) circuits, Computer Architectures**

## EDUCATION

**B.S, Electrical Engineering (EE)**

Sep 2019 - Present

National Taiwan University, (NTU)

Phi Tau Phi Honorary Member (for **top 1%** of college graduates)

Major GPA: **4.28** / 4.3, Overall GPA: **4.25** / 4.3, Rank: **4th** / 264 (**2%**)

## RESEARCH EXPERIENCE

**Computing and Sensing Group (Prof. Kentaro Yoshioka), Keio Univ., Japan**

Sep 2022 - Present

Computing-In-Memory (CIM) Macro for NN - with UTokyo [1]

- Proposed a **hybrid CIM macro** with concurrent digital & analog computation, providing flexible trade-off between efficiency and accuracy
- Proposed a **saliency-aware framework** that dynamically allocates the computation into digital and analog domains based on the importance of the inputs, achieving a 1.95x energy efficiency gain

Hidden Network (HNN) Algorithm/Architecture Co-design - with UTokyo [2]

- Proposed **Layer-Penetrative Tiling (LPT)**, a significantly enhanced cross-layer computation algorithm for HNN, reducing the size of intermediate activation by 26x
- Designed an **end-to-end HNN CIM processor** capable of executing huge networks (ResNet50@ImageNet) with a mere 72KB activation memory, demonstrating a 14.2x reduction in memory size
- Proposed an **activation-localized (AL) dataflow** that preserves the locality between output and input activations, leading to a 1.6x reduction in the number of activation accesses
- Devised a **compact CIM macro** that reuses capacitors for both MAC computation and A/D conversion

**Energy-Efficient Circuits and Systems (EECS) Lab (Prof. Tsung-Te Liu), NTU**

Sep 2021 - Present

End-to-End CIM Processor for NN - with TSMC and MediaTek [3]

- Designed an SRAM CIM processor with a **flexible input buffer** to maintain high data reuse under various dataflows and maximize hardware utilization rate among diverse input topologies
- Taped out a 28nm chip and achieved SOTA efficiencies of 1081.1 GOPS/mm<sup>2</sup> and 51.4 TOPS/W

## PUBLICATIONS

[1] **Yung-Chin Chen**, S. Ando, D. Fujiki, S. Takamaeda-Yamazaki, K. Yoshioka, "OSA-HCIM: On-The-Fly Saliency-Aware Hybrid SRAM CIM with Dynamic Precision Configuration", ASP-DAC 2024

[2] **Yung-Chin Chen**, S. Ando, D. Fujiki, S. Takamaeda-Yamazaki, K. Yoshioka, "HALO-CAT: A Hidden Network Processor with Activation-Localized CIM Architecture and Layer-Penetrative Tiling", DAC 2024 (**Under Review**)

[3] T.-Y. Wu\*, Y.-H. Pan\*, **Yung-Chin Chen\***, W.-C. Tseng\* et al., "N2N-BP<sup>2</sup>CIM: A 28nm 1018.1GOPS/mm<sup>2</sup> End-to-End Bit-Parallel, Bit-Parallel Computing-in-Memory DNN Processor with High-Bandwidth 14T-SRAM Bitcell", VLSI Symposium 2024 (**Waiting for Submission**) (\* denotes equally credited authors)

## HONORS AND AWARDS

<b>Irving T. Ho Memorial Scholarship</b> - EE dept. at NTU	<i>Dec 2022</i>
<b>The Memorial Scholarship Foundation to Lin Hsiung Chen</b> , acceptance rate: 2%	<i>Nov 2022</i>
<b>Research Grant</b> - National Science and Technology Council (NSTC), Taiwan	<i>Jul 2022 - Jan 2023</i>
<b>Research Grant</b> - Taiwan Semiconductor Manufacturing Co., Ltd (TSMC)	<i>Feb 2022 - Jun 2022</i>
<b>1st Place (Best Solver Award)</b> ,	<i>Mar 2022</i>

## SELECTED PROJECTS

<b>180nm ASIC chip for American Option Pricing Using Monte-Carlo Method (ㄅ)</b>	Verilog, Innovus
<ul style="list-style-type: none"><li>• Taped out a chip for American option pricing, attaining a 500x speedup compared to CPU benchmark</li><li>• Implemented a Monte-Carlo core with Sobol RNG for cash flow matrix simulation</li></ul>	
<b>Hand-Motion-Controlled Doodle Jump Game on FPGA (ㄅ)</b>	Verilog, System Verilog, FPGA
<ul style="list-style-type: none"><li>• Designed a fully motion-controlled interactive game with player's hands and voice using FPGA</li><li>• Implemented DSP modules for motion and gesture recognition and realized real-time gaming display</li></ul>	

## WORKING EXPERIENCE

<b>TA of Computer Architectures</b> , lectured by Prof. Tsung-Te Liu	Sep 2023 - Present
<ul style="list-style-type: none"><li>• Designed Verilog assignments including ALU, CPU, and Cache and delivered programming tutorials</li></ul>	
<b>TA of EECS Lab Undergraduate Research</b> , supervised by Prof. Tsung-Te Liu	Sep 2022 - Present
<ul style="list-style-type: none"><li>• Guided new lab members through the paper survey of CIM and relevant circuit simulation</li><li>• Established training courses for circuit design tools, encompassing HSPICE, Verilog, and Virtuoso</li></ul>	
<b>TA of Signal and Systems</b> , lectured by Prof. Lin-Shan Lee	Feb 2022 - Jun 2022
<ul style="list-style-type: none"><li>• Delivered MATLAB lectures, held weekly problem-solving seminars, and graded homeworks and exams</li></ul>	

## TECHNICAL SKILLS

**Programming:** Verilog, System Verilog, Python, C++, MATLAB  
**IC Design Tools:** NC-Verilog, Design Compiler, Innovus, Virtuoso, HSPICE, FPGA  
**Languages:** Chinese (Mandarin), English (TOEFL: MyBest 111/120, GRE: 333/340), Japanese (JLPT N1)  
**Toolbox:** PyTorch, NumPy,  $\LaTeX$

## ACTIVITIES

<b>One-year Exchange Student in Keio University, Japan</b>	Oct 2022 - Sep 2023
<ul style="list-style-type: none"><li>• Accumulated extensive experience in cross-cultural learning and communication with foreigners</li></ul>	
<b>Student Ambassador of NTU</b>	Oct 2021 - Sep 2022
<ul style="list-style-type: none"><li>• Introduced Taiwan to foreign visitors, orchestrated international events and guided campus tours</li><li>• Provided support for the integration of international scholars into Taiwanese life</li></ul>	
<b>Vice Captain of NTUEE Baseball Team</b>	Sep 2021 - Aug 2022
<ul style="list-style-type: none"><li>• Led and coached a team of 20+ players; provided personalized instructions and training menus</li></ul>	
<b>Vice President of NTU Escape Room and Puzzle Solving Club</b>	Aug 2020 - Jul 2021
<ul style="list-style-type: none"><li>• Led a club of 30+ members to design engaging puzzles and develop reality games</li><li>• Held 3 school-wide real escape games, attracting over 200 participants</li></ul>	