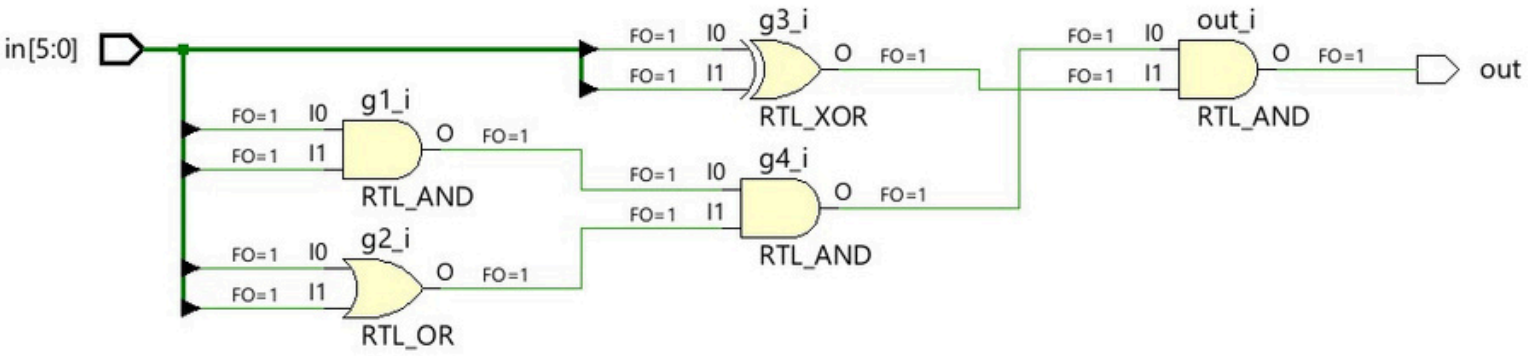
EX=01

```
module LogicDepth (
  input wire [5:0] in,
// 6 input signals
  output out
// Integer output (4-bit for flexibility)
);

wire g1, g2, g3, g4;
// 5 logic gates

// Example logic gate connections
assign g1 = in[0] & in[1];   // AND gate
assign g2 = in[2] | in[3];   // OR gate
assign g3 = in[4] ^ in[5];        // XOR gate
assign g4 = g1&g2;       // NOT gate
assign out = g4&g3;        // Final AND gate


endmodule
```



Generated model

Predected output

OUTPUT:01

FAN OUT:01

FAN IN :02

NO OF INPUT:06

NUMBER OF GATES:05