East West University
Department of Computer Science and Engineering
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Course Code: CSE345
Course Title: Digital Logic Design
Section: 02

Experiment Number: 05
Experiment Title: Full Adder using Decoder

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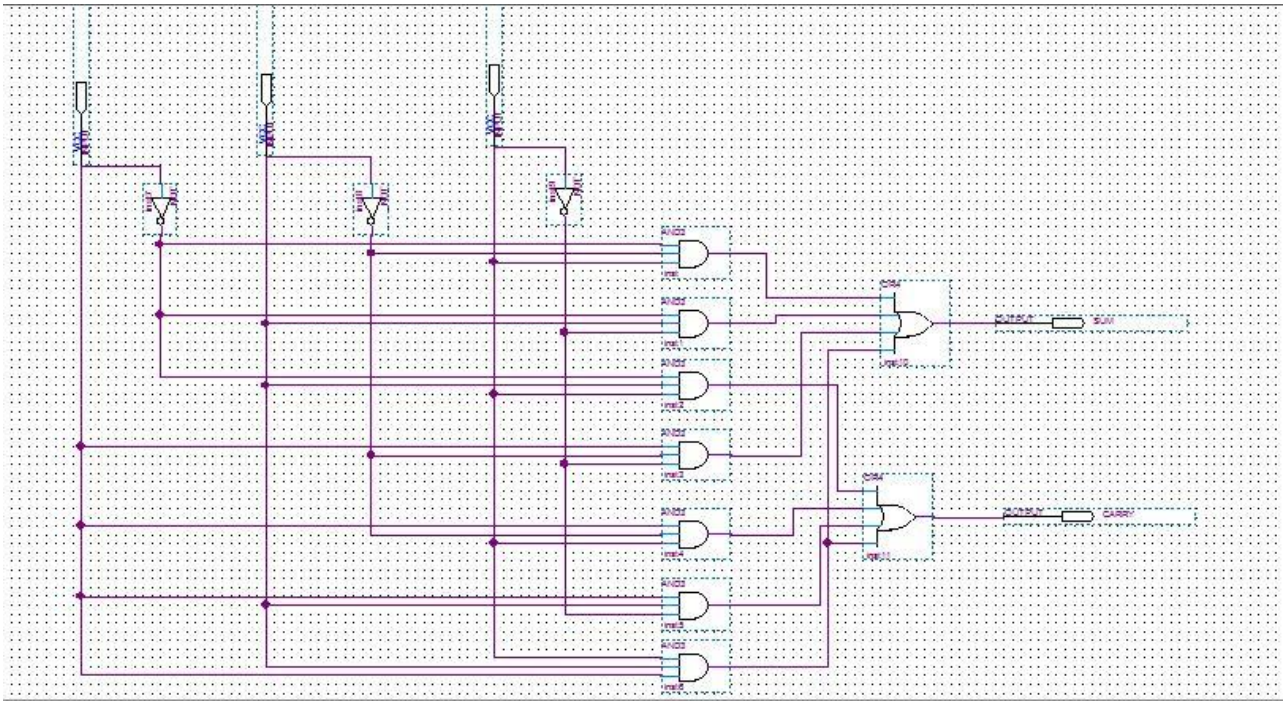
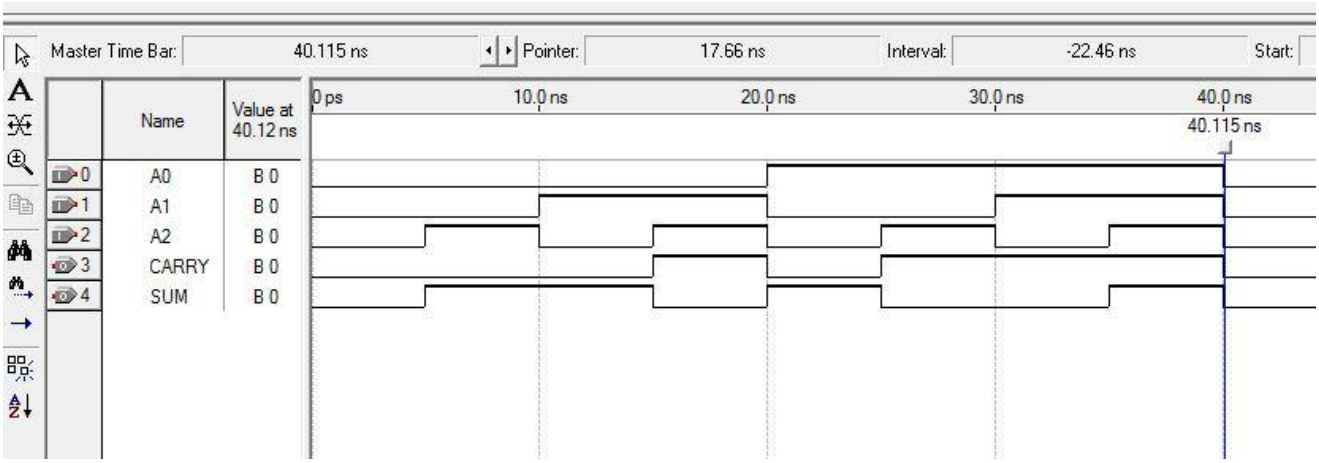
Schematic Diagram



Note – we avoid the D_0 - and gate of the built in decoder as it was not compiling and showing error of incomplete circuit.

Waveform



Brief Explanation

1. We implemented and simulated a **Full Adder** using a **Decoder** to demonstrate its functionality in generating the SUM and CARRY outputs.
2. The circuit design used the decoder's outputs and combined them with logic gates for correct functionality.
3. During the simulation, we faced an issue with the built-in decoder's incomplete D_0 output, so we adjusted the design to avoid compilation errors.
4. The waveform verified that the outputs matched the expected truth table for a full adder.
5. This experiment helped us understand the practical use of decoders in arithmetic circuits and the challenges in real-world digital design simulations.