East West University
Department of Computer Science and Engineering
Fall '24

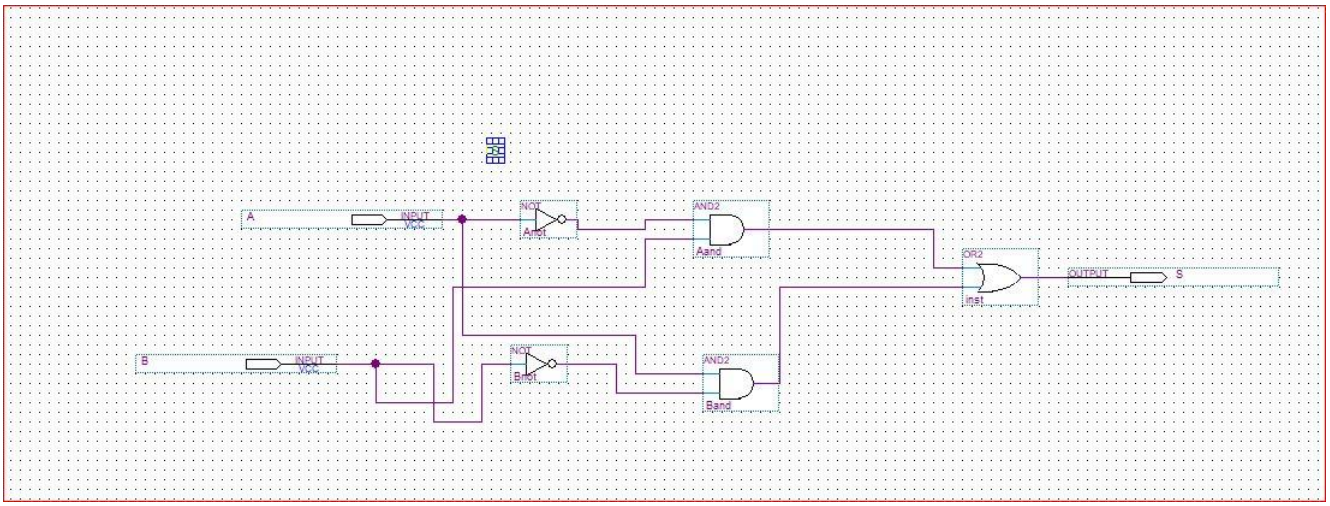
Course Code: CSE345
Course Title: Digital Logic Design
Section: 02

Experiment Number: 01
Experiment Title: Schematic and Structural Verilog Simulation of Combinational Logic Circuits

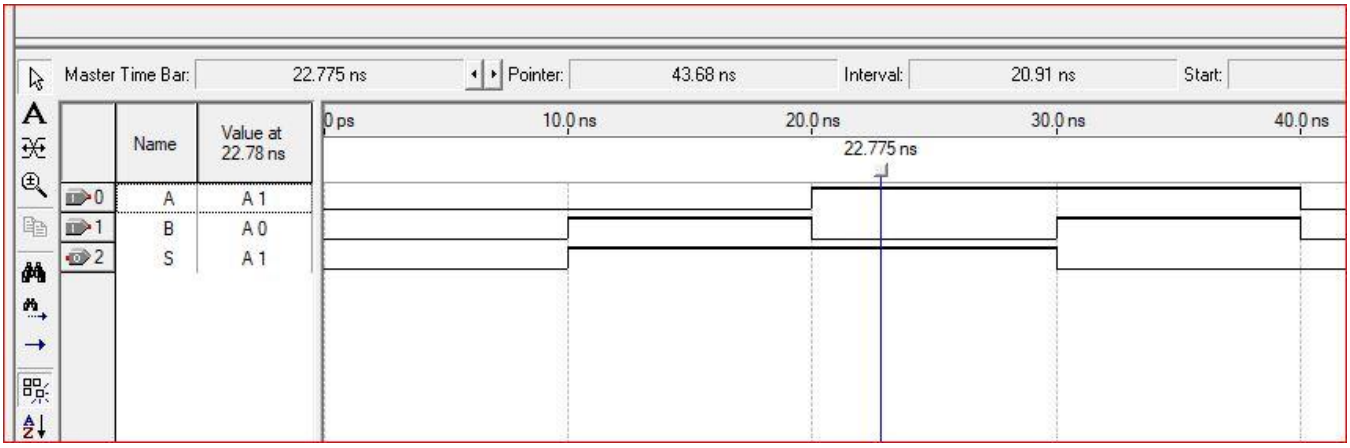
Name	Student ID
1. Riya Akter	2022-3-60-176
2. Mohua Akter	2022-3-60-112

Date of Submission: January 22, 2025

Schematic Diagram



Waveform



Brief Explanation

1. We simulated a simple combinational logic circuit to understand the basics of digital design.
2. The schematic and waveform confirmed the expected behavior of the circuit.
3. This circuit is a basic example often used in learning and in small-scale applications like signal routing.
4. While working, we identified minor risks, such as incorrect connections or timing mismatches, which could impact the circuit.
5. Overall, this experiment gave us hands-on experience with basic simulation tools and the fundamentals of circuit behavior.