



East West University
Department of Computer Science and Engineering
Fall '24

Course Code: CSE345
Course Title: Digital Logic Design
Section: 02

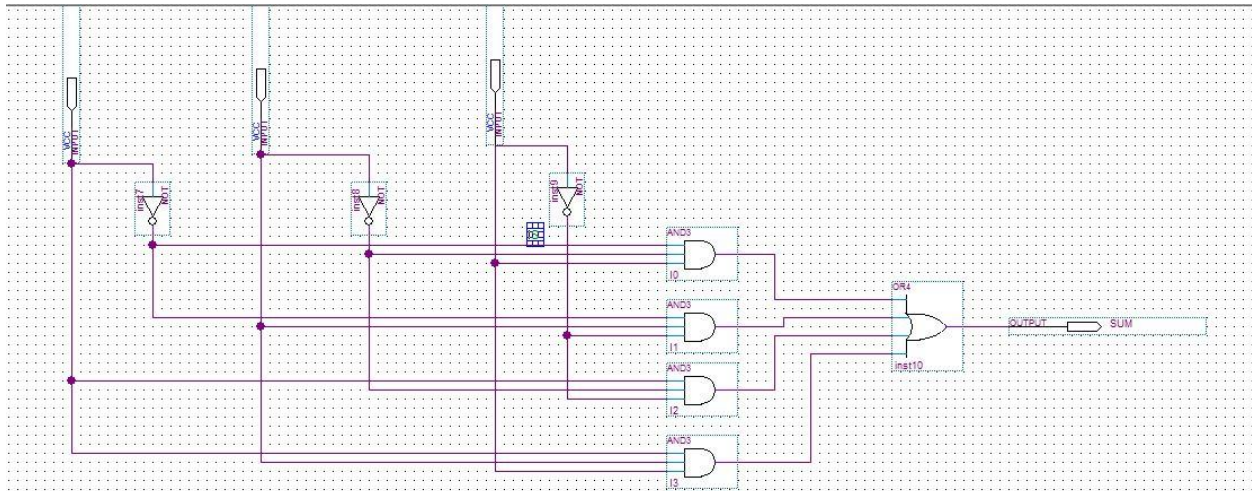
Experiment Number: 06
Experiment Title: Full Adder using Multiplexer

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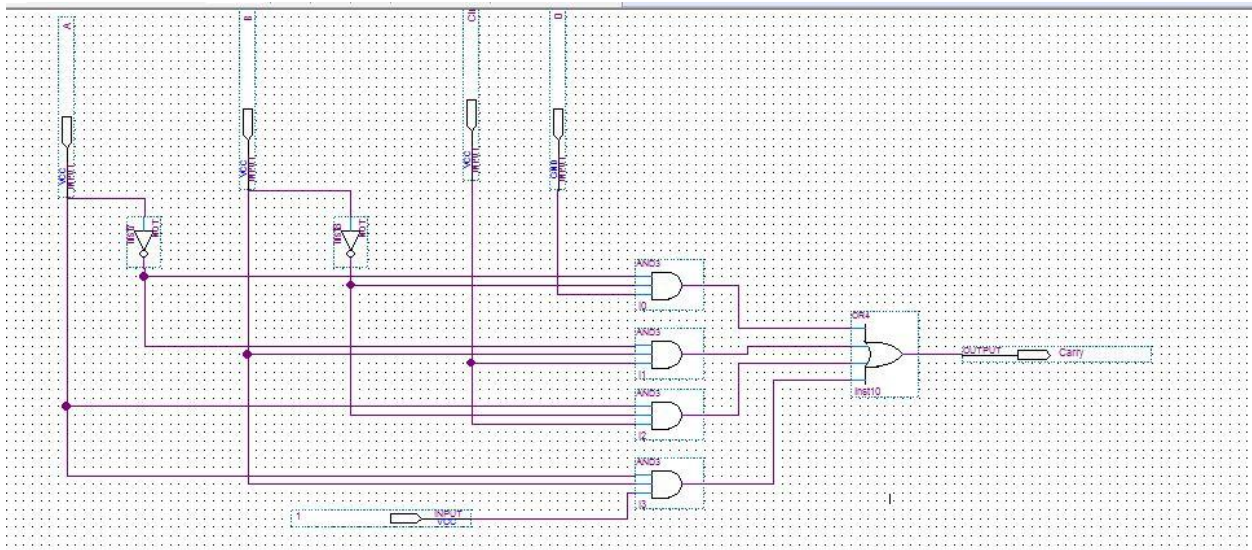
Date of Submission: January 22, 2025

Schematic Diagram

For SUM :

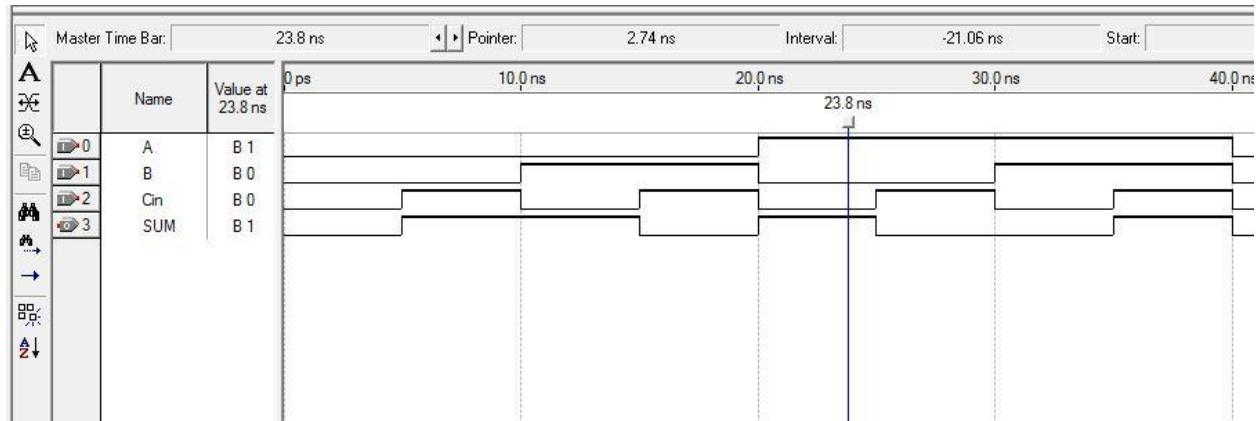


For Carry :

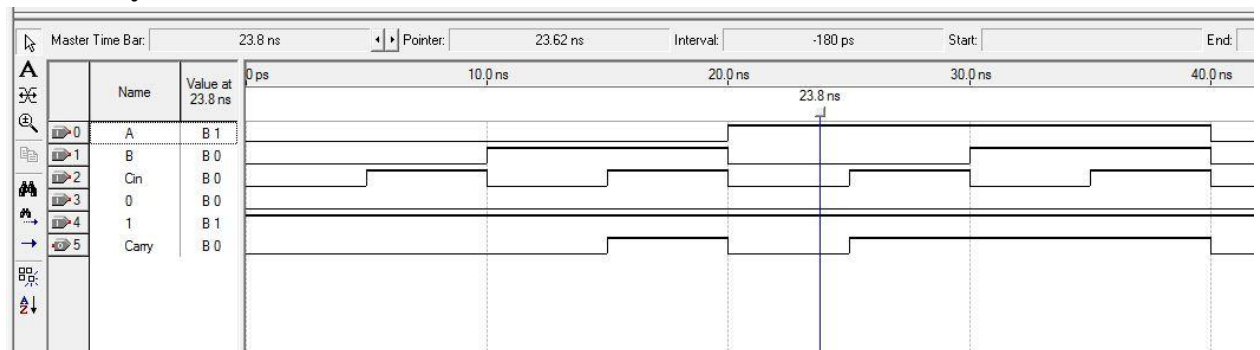


Waveform

For SUM :



For Carry :



DISCUSSION

For SUM:

1. The **AND gates** represent inputs as I0, I1, I2, and I3, which logically correspond to different truth table conditions for the SUM bit.
2. We use a different approach of Cin input, avoid separately taking I0, I1, I2, and I3 , as it was giving us correct output and no error in the waveform , in we use separate I0, I1, I2, and I3, the waveform act weird and shows error
3. The correct functionality of the SUM logic is verified with expected results.

For Carry:

1. We use a different approach of Cin input, avoid separately taking I0, I1, I2, and I3 , just for the same reason of sum
2. **Fixed Inputs:** To simplify the design:
 - **VCC** is used as a fixed 1 input.
 - **GND** is used as a fixed 0 input.

Summary:

1. The SUM and Carry outputs were verified through simulation. Both waveforms aligned with the theoretical outputs of the full adder truth table, confirming design correctness.
2. This implementation using a 4-to-1 multiplexer effectively showcased the full adder operation, balancing logical design with practical waveform validation.