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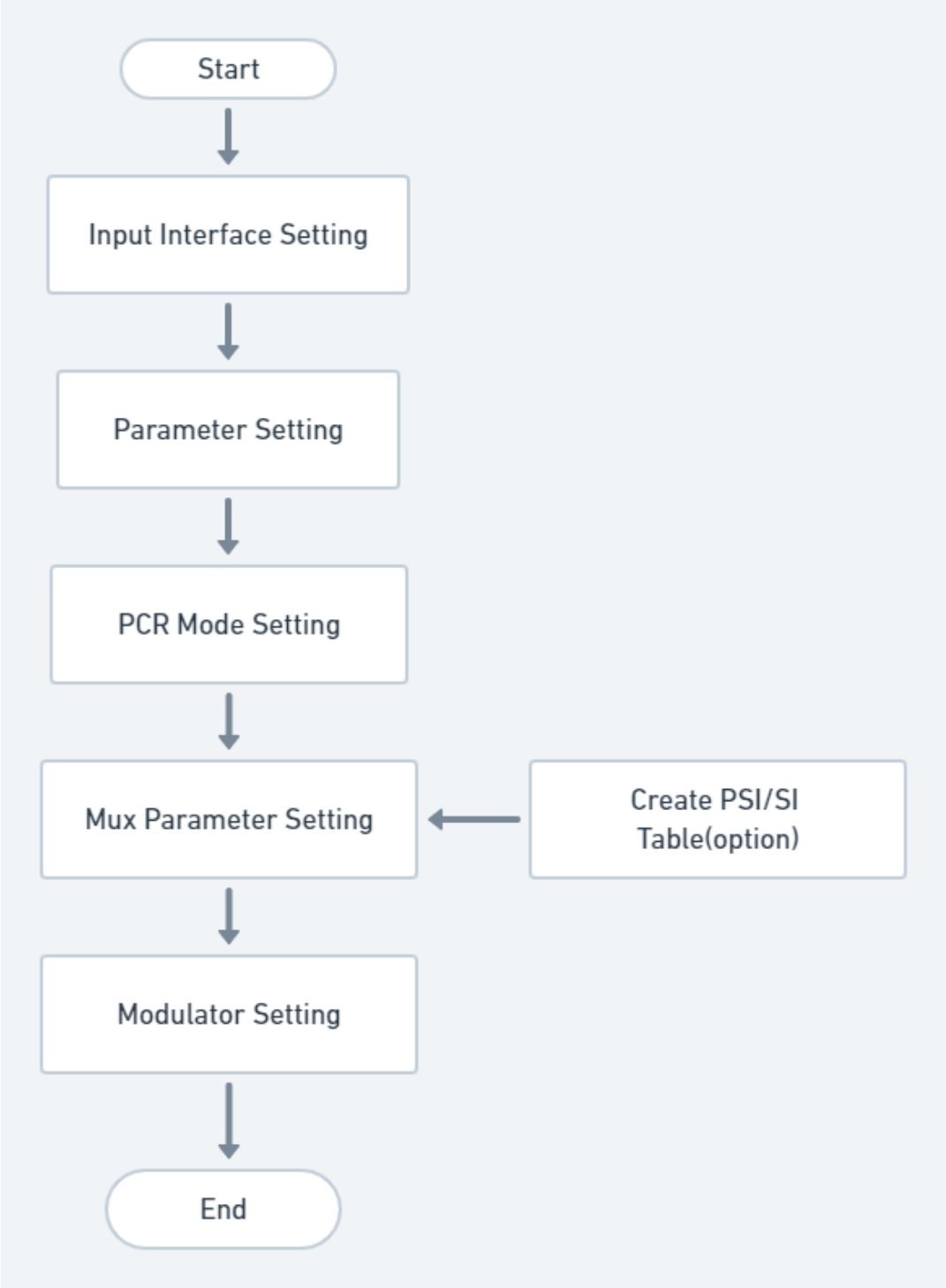
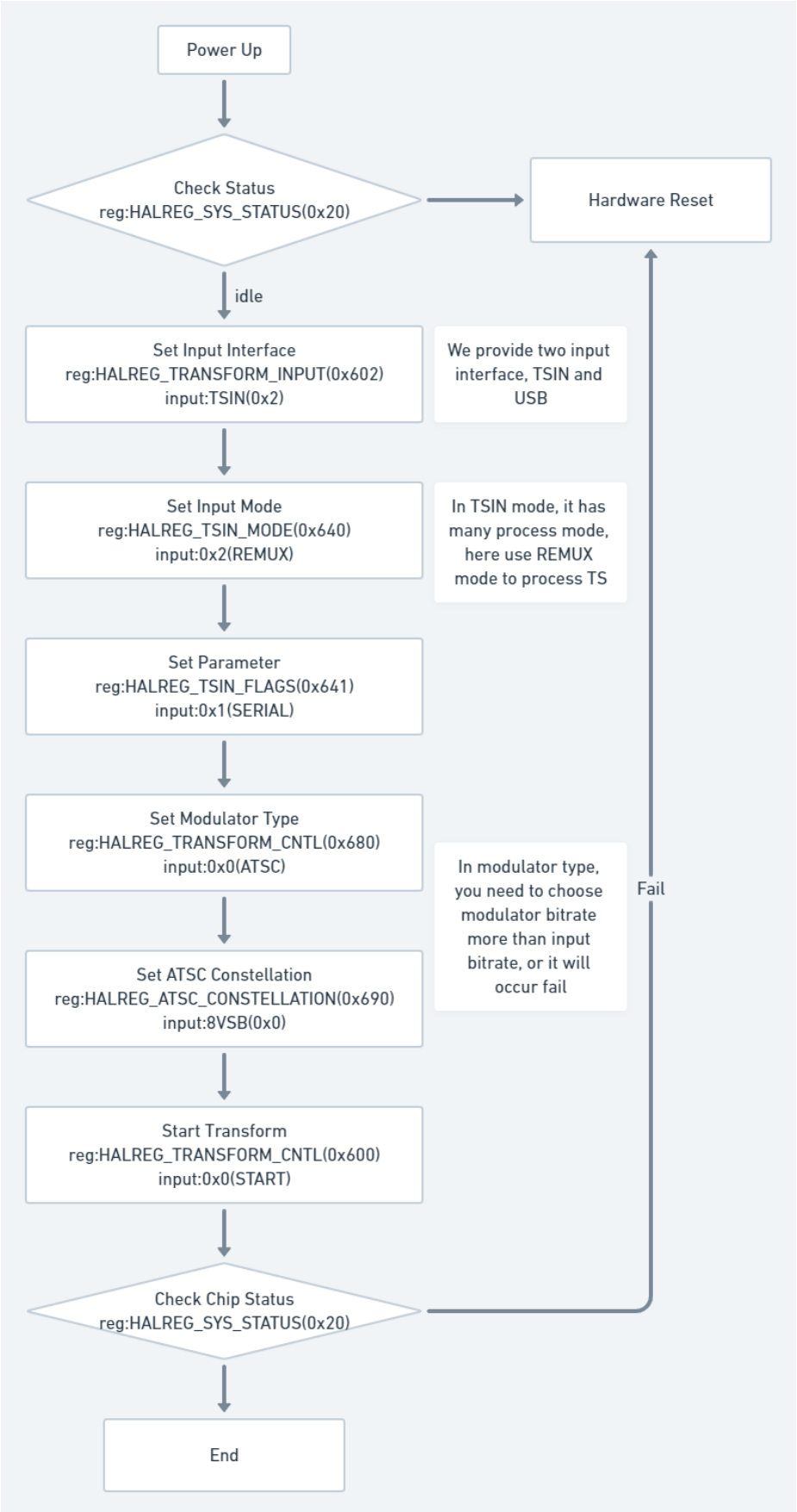
1.System Process

1.1 Process Overview



1.2 Process of Chip



2. Status Registers(BASE)

The BASE registers are basic information register sets for VATek chips. Base register sets help developer to understand chip basic information and real-time status, which includes chip status, chip ID, supported functions and information lists and error code as well.

2.1 System Status

0x20 - HALREG_SYS_STATUS_0: System Status Register

Bit #	Type	Value	Name
0-7	R	0xFF000001	SYS_STATUS_IDLE
	R	0xFF000002	SYS_STATUS_RUN
	R	0xFF000080	SYS_STATUS_ERRTAG
	R	0xFF000085	SYS_STATUS_LOADER FAIL
	R	0xFF000086	SYS_STATUS_SERVICE_FAIL
	R	0xFF000088	SYS_STATUS_EXCEPTION_FAIL
	R	0xFF00008E	SYS_STATUS_BADSTATUS
	R	0xFF00008F	SYS_STATUS_UNKNOWN_FAIL
8-23	--	Reserved	Reserved
24-31	R	0xFF000000	SYS_STATUS_TAG

Description

This register use to read chip status, when reset chip and power up, chip status will be SYS_STATUS_IDLE, if the service is running, status will be SYS_STATUS_RUN,

0x23 - HALREG_SYS_ERRCODE: System Error Code

Bit #	Type	Value	Name
0-31	R	0x80000001	SYS_ERRCODE_INIT
	R	0x80010001	LOADER_ERRCODE_NOAPP
	R	0x80010002	LOADER_ERRCODE_CRC32
	R	0x80010003	LOADER_ERRCODE_HW
	R	0x80020001	SERVICE_INIT_FAIL
	R	0x80020002	SERVICE_HW_FAIL

Description

This register use to show error code from chip, if firmware download fail in chip, the error code will happen.

0x24 - HALREG_CHIP_ID

Bit #	Type	Value	Name
0-31	R	0x00010100	HAL_CHIPID_A1
	R	0x00010300	HAL_CHIPID_A3
	R	0x00020100	HAL_CHIPID_B1
	R	0x00020200	HAL_CHIPID_B2
	R	0x00020201	HAL_CHIPID_B2_PLUS
	R	0x00020300	HAL_CHIPID_B3
	R	0x00020301	HAL_CHIPID_B3_PLUS

Description

This register will show what chip is connecting,

0x25 - HALREG_FW_VER

Bit #	Type	Value	Name
0~31	R	--	

Description

This register shows firmware version, version number made by create date of firmware(.v2app) in hex.

0x26 - HALREG_SERVICE_MODE: Chip Service Mode

Bit #	Type	Value	Name
0~31	R	0xFF000001	SERVICE_TAG_RESCUE
	R	0xF8000001	SERVICE_TAG_BROADCAST
	R	0xF8000002	SERVICE_TAG_TRANSFORM

Description

This register shows chip services, we provide two services base on different chip series, and rescue mode is use to update firmware, you can you romtool to update firmware or use HAL regiseter to write v2img in chip.

0x27 - HALREG_PERIPHERAL_EN: Peripheral Chip ID

Bit #	Type	Value	Name
0~31	R	0x000000FF	PERIPHERAL_RF_MASK
	R	0x00000002	PERIPHERAL_FINTEKR2
	R	0x00FF0000	PERIPHERAL_VIDEO_MASK
	R	0x00010000	PERIPHERAL_EP9555E

Description

This register shows what peripheral device we connect with chip.

0x28 - HALREG_INPUT_SUPPORT: Supported Functions

Bit #	Type	Value	Name
0	R	0x00000001	INPUT_EN_TEST
1	R	0x00000002	INPUT_EN_USB
2	R	0x00000004	INPUT_EN_TS
3	R	0x00000008	INPUT_EN_ENC
4	R	0x00000010	VENC_EN_MPEG2
5	R	0x00000020	VENC_EN_H264
7	--	Reserved	
8	R	0x00000100	VENC_EN_FULLHD
9 ~11	--	Reserved	
12	R	0x00001000	AENC_EN_MP1_L2
13	R	0x00002000	AENC_EN_AAC_LC_ADTS
14	R	0x00004000	AENC_EN_AC_3
15	R	0x00008000	AENC_EN_AAC_LC_LATM
16	R	0x00010000	TSIN_EN_BYPASS
17	R	0x00020000	TSIN_EN_TSSMOOTH
18	R	0x00040000	TSIN_EN_TSREMUX
19	R	0x00070000	TSIN_EN_ALL
20	R	0x00100000	TEST_EN_HW
21	R	0x00200000	TEST_EN_REMUX
22	R	0x00300000	TEST_EN_ALL
23-31	--	Reserved	Reserved

Description

This register shows many input we support, we support different input interfaced, and TS input interface has many process mode, BYPASS, TSSMOOTH, TSREMUX,

0x29 - HALREG_OUTPUT_SUPPORT: Supported Output Functions

Bit #	Type	Value	Name
0	R	0x00000001	OUTPUT_EN_MOD
2	R	0x00000004	OUTPUT_EN_TS
3	R	0x00000008	OUTPUT_EN_USB
4-6	--	Reserved	

8	R	0x00000100	MOD_EN_DVB_T
7	R	0x00000200	MOD_EN_J83_A
9	R	0x00000400	MOD_EN_ATSC
10	R	0x00000800	MOD_EN_J83_B
11	R	0x00001000	MOD_EN_DTMB
12	R	0x00002000	MOD_EN_ISDB_T
13	R	0x00004000	MOD_EN_J83_C
14	R	0x00008000	MOD_EN_DVB_T2
15	R	0x00005F00	MOD_EN_BASE
16	R	0x01000000	DVB_T2_EN_FFT32K
17-31	--	Reserved	Reserved

Description

This register shows output we support, we have many modulators you can choose based on different country.

2.2 Transform Status

0x620 - HALREG_BCINFO_STREAM: Show the setting value of HALREG_BROADCAST_STREAM.

Bit #	Type	Value	Name
0~2	R	0x00000000	STREAM_TESTMODE
	R	0x00000001	STREAM_USB
	R	0x00000002	STREAM_TSIN
	R	0x00000003	STREAM_ENCODER
3~31		Reserved	

Description

This register use to read what input interface using now,

0x621 - HALREG_BCINFO_OUTPUT: Show the setting value of HALREG_BROADCAST_OUTPUT.

Bit #	Type	Value	Name
0	R	0x00000000	OUTPUT_MODULATOR
1~31		Reserved	

Description

This register use to read output mode, we provide modulator mode to be

output, you can choose different modulator type.

0x622 - HALREG_BCINFO_MODRATE

Bit #	Type	Value	Name
0~31	R		

Description

This register use to read real output bitrate of modulator, bitrate size base on different modulator type.

0x623 - HALREG_BCINFO_MUXRATE: Show Bitrate of MUX.

Bit #	Type	Value	Name
0~31	R		

Description

This register use to read MUXER bitrate.

0x624 - HALREG_BCINFO_STATUS

Bit #	Type	Value	Name
0~1	R	0x00000000	BCSTATUS_IDLE
	R	0x00000001	BCSTATUS_WAIT_SOURCE
	R	0x00000002	BCSTATUS_BROADCAST
	R	0x00000003	BCSTATUS_FINISH
2~31		Reserved	
32	R	0x80000000	BCSTATUS_FAIL_UNKNOWN
	R	0x80000001	BCSTATUS_FAIL_SOURCE
	R	0x80000002	BCSTATUS_FAIL_TIMEOUT
	R	0x80000003	BCSTATUS_FAIL_CODECDROP
	R	0x80000004	BCSTATUS_FAIL_BUFFER
	R	0x80000005	BCSTATUS_FAIL_MUXER
	R	0x80000006	BCSTATUS_FAIL_ENCODE
	R	0x80000007	BCSTATUS_FAIL_MEDIA
	R	0x80000008	BCSTATUS_FAIL_DEMUX

Description

This register use to read broadcast status.

0x625 - HALREG_BCINFO_CURRATE: Show real bitrate of MUX.

Bit #	Type	Value	Name
0~31	R		

Description

This register use to read current bitrate of MUXER

3. Transform Input Registers

Broadcaster registers are the main switches to activate / deactivate modulator, RF mixer. The operating status indicators are also in the register set.

3.1 Transform Control

0x602 - HALREG_TRANSFORM_INPUT: Transform input Select

Bit #	Type	Value	Name
0~1	W	0x00000000	STREAM_NULL
	W	0x00000001	STREAM_USB
	W	0x00000002	STREAM_TSIN

3.2 A USB Mode Parameter

0x640 - HALREG_USB_INPUT_MODE: USB MODE Control

Bit #	Type	Value	Name
0	W		
1-31	--	Reserved	Reserved

0x641 - HALREG_USB_STREAM_FLAGS: USB MODE FLAGS

Bit #	Type	Value	Name
0	W		
1-31	--	Reserved	Reserved

0x642 - HALREG_USB_PCR_MODE: PCR MODE IN USB MODE

Bit #	Type	Value	Name
0	W		
1-31	--	Reserved	Reserved

0x643 - HALREG_USB_ADJUST_TICK: USB MODE ADJUST TICK SET

Bit #	Type	Value	Name
0	W		
1-31	--	Reserved	Reserved

3-2 B TSIN Mode

0x640 - HALREG_TSIN_MODE: TS mode select (Pure Modulator Only)

Bit #	Type	Value	Name
	W	0x00000001	STREAM_MODE_SMOOTH
	W	0x00000002	STREAM_MODE_REMUX
	W	0x00000003	STREAM_MODE_PASSTHROUGH
2-31	--	Reserved	Reserved

0x641 - HALREG_TSIN_FLAGS: TS interface function flags

Bit #	Type	Value	Name
0	W	0x00000001	TS_PIN_SERIAL
1	W	0x00000002	TS_PIN_NEGATIVE_CLK
2	W	0x00000004	TS_PIN_NEGATIVE_VALID
3	W	0x00000008	TS_PIN_NEGATIVE_SYNC
4-31	--	Reserved	Reserved

0x642 – HALREG_TSIN_PCR_MODE: TS PCR Mode

Bit #	Type	Value	Name
0	W	0x00000000	PCR_MODE_DISABLE
1	W	0x00000001	PCR_MODE_ADJUST
2	W	0x00000002	PCR_MODE_RETAG

4. MUX Registers

Regarding to the information of PSI/SI MUX insertion refers to psi insertion porting guide.

4.1 Mux Related Settings

0x610 - HALREG_MUX_PCR_PID: Register for Writing PCR PID

Bit #	Type	Value	Name
0~31	W		

0x611 - HALREG_MUX_PADDING_PID: Register for Writing Padding PID

Bit #	Type	Value	Name
0~31	W		

0x612 - HALREG_BITRATE: Register for Writing Bitrate Limitation

Bit #	Type	Value	Name
0~31	W		

0x2000 - HALREG_MUXPSI_MODE: Produce Mode of PSI

Bit #	Type	Value	Name
0	W	0x00000000	MUX_PURE
3	W	0x00000003	MUX_DEFSPEC
4~31		Reversed	

5. PSI Register

5.1 Playload Buffer Register

0x2100 - HALRANGE_PLAYLOAD_START: register of register PSI/SI table start tag, it's start at 0x2100.

Bit #	Type	Value	Name
0~31	W		

0x3000 - HALRANGE_PLAYLOAD_END: register of register PSI/SI table end tag, it's end at 0x3000

Bit #	Type	Value	Name
0~31	W		

5.2 PSI Pure Mode

Please follow appendix A

0x00 - HALOF_RAWPSI_TAG: start and end tag in PSI PURE mode, you need to use start tag when writing new PSI table, and use end tag after finishing table.

Bit #	Type	Value	Name
0~31	W	0xFF070600	RAWPSI_EN_TAG
	W	0xFF0706FF	RAWPSI_EN_ENDTAG

0x01 - HALOF_RAWPSI_INTERVAL: PSI Table Interval Time (ms)

Bit #	Type	Value	Name
0~31	W		

0x02 - HALOF_RAWPSI_PACKETS: PSI Table packet size

Bit #	Type	Value	Name
0~31	W		

0x03 – HALOF_RAWPSI_DATA: write PSI table data continuously

Bit #	Type	Value	Name
0~31	W		

5.3 Private PSI table

Please follow appendix B

Private PSI table is the way in PURE mode, it's only can be inserted table after chip start broadcast, but private PSI provide dynamically modify and insert table.

0x639 – HALREG_PRIVATE_START: private stream playload start address

Bit #	Type	Value	Name
0~31	W		

0x63A – HALREG_PRIVATE_END: private stream playload end address

Bit #	Type	Value	Name
0~31	W		

0x063B – HALREG_PRIVATE_CNTL: private stream control

Bit #	Type	Value	Name
0	W	0x80000000	PRIVATE_EN_CONTINUE
1	W	0x00000001	PRIVATE_EN_TIMES
2~31	W		

Description

- PRIVATE_EN_CONTINUE: when write and read pointer are not equal, user can use this flag to send PSI table to chip.
- PRIVATE_EN_TIMES: set PRIVATE_EN_TIMES can insert table one time after broadcast start.

0x63C – HALREG_PRIVATE_WPTR: Private stream write pointer (update by user)

Bit #	Type	Value	Name
0~31	W		

0x63D – HALREG_PRIVATE_RPTR: private stream read pointer

(update by hardware)

Bit #	Type	Value	Name
0~31	R		

6. Modulator Register

6.1 Modulator Related Settings

0x601 - HALREG_TRANSFORM_MODE: Transform Mode Select

Bit #	Type	Value	Name
	W	0x00000005	TRANSFORM_BROADCAST

0x680 - HALREG_MODULATOR: Modulation Standard Register

Bit #	Type	Value	Name
0~3	W	0x00000000	MOD_DVB_T
	W	0x00000001	MOD_J83A
	W	0x00000002	MOD_ATSC
	W	0x00000003	MOD_J83B
	W	0x00000004	MOD_DTMB
	W	0x00000005	MOD_ISDB_T
	W	0x00000006	MOD_J83C
	W	0x00000007	MOD_DVB_T2
4~31		Reserved	

0x681 - HALREG_MOD_IFMODE: Modulation Switch Register

Bit #	Type	Value	Name
0~1	W	0x00000001	IFMODE_DISABLE
	W	0x00000003	IFMODE_IQ_OFFSET
2~31		Reserved	

0x682 - HALREG_MOD_IFFREQ: Offset Setting Register

Bit #	Type	Value	Name
	W		

0x683 - HALREG_MOD_DACGAIN: DAC Gain Setting Register

Bit #	Type	Value	Name
	W		

0x684 - HALREG_MOD_BW_SB: Modulator Bandwidth or Symbol Rate Setting Register

Bit #	Type	Value	Name
	W		

6.2 DVB-T Settings

0x690 - HALREG_DVB_T_CONSTELLATION: DVB-T Constellation Register

Bit #	Type	Value	Name
0	W	0x00000000	DVB_T_QPSK
1	W	0x00000002	DVB_T_QAM16
2	W	0x00000004	DVB_T_QAM64
3~31		Reserved	--

0x691 - HALREG_DVB_T_FFT: DVB-T Carrier Mode Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DVB_T_FFT2K
	W	0x00000001	DVB_T_FFT8K
2~31		Reserved	--

0x692 - HALREG_DVB_T_GUARDINTERVAL: DVB-T Guard Interval Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DVB_T_GI_1_32
	W	0x00000001	DVB_T_GI_1_16
	W	0x00000002	DVB_T_GI_1_8
	W	0x00000003	DVB_T_GI_1_4
2~31		Reserved	--

0x693 - HALREG_DVB_T_CODERATE: DVB-T Code Rate Register

Bit #	Type	Value	Name
0~2	W	0x00000000	DVB_T_CODERATE_1_2
	W	0x00000001	DVB_T_CODERATE_2_3
	W	0x00000002	DVB_T_CODERATE_3_4
	W	0x00000003	DVB_T_CODERATE_5_6
	W	0x00000004	DVB_T_CODERATE_7_8
3~31		Reserved	--

6.3 DVB-C (J83A) Settings

0x690 - HALREG_J83A_CONSTELLATION: DVB-C (J83.A)
Constellation Register

Bit #	Type	Value	Name
0~2	W	0x00000000	J83A_QAM16
	W	0x00000001	J83A_QAM32
	W	0x00000002	J83A_QAM64
	W	0x00000003	J83A_QAM128
	W	0x00000004	J83A_QAM_256
3~31		Reserved	--

6.4 ATSC (8VSB) Settings

0x690 - HALREG_ATSC_ CONSTELLATION: ATSC (8VSB)
Constellation Register

Bit #	Type	Value	Name
0	W	0x00000000	ATSC_8VSB
1~31		Reserved	--

6.5 Clear QAM (J83.B) Settings

0x690 - HALREG_J83B_CONSTELLATION: Clear QAM(J83B)
Constellation Register

Bit #	Type	Value	Name
0~1	W	0x00000001	J83B_QAM64
	W	0x00000003	J83B_QAM128
2~31		Reserved	--

6.6 DTMB Settings

0x690 - HALREG_DTMB_CONSTELLATION: DTMB Constellation
Register

Bit #	Type	Value	Name
0~2	W	0x00000000	DTMB_QPSK
	W	0x00000001	DTMB_QAM16

	W	0x00000002	DTMB_QAM64
	W	0x00000004	DTMB_QAM32
3~31		Reserved	--

0x691 - HALREG_DTMB_TIME_INTERLEAVED: DTMB Time Interleaved Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DTMB_TI_DISABLE
	W	0x00000001	Reserved
	W	0x00000002	DTMB_TI_240
	W	0x00000003	DTMB_TI_720
2~31		Reserved	--

0x692 - HALREG_DTMB_CODERATE: DTMB Code Rate Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DTMB_CODERATE_0_4
	W	0x00000001	DTMB_CODERATE_0_6
	W	0x00000002	DTMB_CODERATE_0_8
2~31		Reserved	--

0x693 - HALREG_DTMB_CARRIERMODE: DTMB Carrier Register

Bit #	Type	Value	Name
0	W	0x00000000	DTMB_CARRIER_3780
	W	0x00000001	DTMB_CARRIER_1
1~31		Reserved	--

0x694 - HALREG_DTMB_SYNCFRAME: DTMB Sync Frame Mode Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DTMB_SYNC_420
	W	0x00000001	DTMB_SYNC_945
	W	0x00000002	DTMB_SYNC_595
2~31		Reserved	--

6.7 ISDB-T Settings

0x690 - HALREG_ISDB_T_CONSTELLATION: ISDB-T Constellation Register

Bit #	Type	Value	Name

0~1	W	0x00000000	ISDB_T_DQPSK
	W	0x00000001	ISDB_T_QPSK
	W	0x00000002	ISDB_T_QAM16
	W	0x00000003	ISDB_T_QAM64
2~31		Reserved	--

0x691 - HALREG_ISDB_T_FFT: ISDB-T Carrier Mode Register

Bit #	Type	Value	Name
0~1	W	0x00000000	ISDB_T_FFT2K
	W	0x00000001	ISDB_T_FFT8K
	W	0x00000002	ISDB_T_FFT4K
2~31		Reserved	--

0x692 - HALREG_ISDB_T_GUARDINTERVAL: ISDB-T Guard Interval Register

Bit #	Type	Value	Name
0~1	W	0x00000000	ISDB_T_GI_1_32
	W	0x00000001	ISDB_T_GI_1_16
	W	0x00000002	ISDB_T_GI_1_8
	W	0x00000003	ISDB_T_GI_1_4
2~31		Reserved	--

0x693 - HALREG_ISDB_T_CODERATE: ISDB-T Code Rate Register

Bit #	Type	Value	Name
0~2	W	0x00000000	ISDB_T_CODERATE_1_2
	W	0x00000001	ISDB_T_CODERATE_2_3
	W	0x00000002	ISDB_T_CODERATE_3_4
	W	0x00000003	ISDB_T_CODERATE_5_6
	W	0x00000004	ISDB_T_CODERATE_7_8
3~31		Reserved	--

0x694 - HALREG_ISDB_T_TIME_INTERLEAVED: ISDB-T Time Interleave Register

Bit #	Type	Value	Name
0~1	W	0x00000000	ISDB_T_TI_DISABLE
	W	0x00000001	ISDB_T_TI_MODE1
	W	0x00000002	ISDB_T_TI_MODE2
	W	0x00000003	ISDB_T_TI_MODE3
2~31		Reserved	--

6.8 J83.C Settings

0x690 - HALREG_J83C_CONSTELLATION: J83.C Constellation Register

Bit #	Type	Value	Name
0	W	Reserved	
1	W	0x00000002	J83C_QAM64
2	W	0x00000004	J83C_QAM256
3~31		Reserved	--

6.9 DVB-T2 Settings

0x691 - HALREG_DVB_T2_FLAGS: DVB-T2 Control Register

Bit #	Type	Value	Name
0	W	0x00000001	T2EN_EXTEND_CARRIER_MODE
1	W	0x00000002	T2EN_CONSTELLATION_ROTATION
2	W	0x00000004	T2EN_INPUT_TS_HEM
3	W	0x00000008	T2EN_DELETE_NULL_PACKET
4	W	0x00000010	T2EN_VBR_CODING
5	W	0x00000020	T2EN_TIME_INTERVAL
6~31		Reserved	--

0x692 - HALREG_DVB_T2_ISSY: DVB-T2 ISSY Register

Bit #	Type	Value	Name
0~1	W	0x00000000	T2_ISSY_DISABLE
	W	0x00000002	T2_ISSY_SHORT
	W	0x00000003	T2_ISSY_LONG
2~31		Reserved	--

0x693 - HALREG_DVB_T2_NIT: DVB-T2 NIT Register

Bit #	Type	Value	Name
0	W	0x00000000	T2_NTI_DISABLE
1~31		Reserved	--

0x694 - HALREG_DVB_T2_L1_CONSTELLATION: DVB-T2 L1 Constellation Register

Bit #	Type	Value	Name

0~2	W	0x00000000	T2_L1_BPSK
	W	0x00000001	T2_L1_QPSK
	W	0x00000002	T2_L1_QAM16
	W	0x00000003	T2_L1_QAM64
3~31		Reserved	--

0x695 - HALREG_DVB_T2_PLP_CONSTELLATION: DVB-T2 PLP Constellation Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_PLP_QPSK
	W	0x00000001	T2_PLP_QAM16
	W	0x00000002	T2_PLP_QAM64
	W	0x00000003	T2_PLP_QAM256
3~31		Reserved	--

0x696 - HALREG_DVB_T2_FFT: DVB-T2 Carrier Mode Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_FFT_1K
	W	0x00000001	T2_FFT_2K
	W	0x00000002	T2_FFT_4K
	W	0x00000003	T2_FFT_8K
	W	0x00000004	T2_FFT_16K
	W	0x00000005	T2_FFT_32K
3~31		Reserved	--

0x697 - HALREG_DVB_T2_CODERATE: DVB-T2 Code Rate Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_CODERATE_1_2
	W	0x00000001	T2_CODERATE_3_5
	W	0x00000002	T2_CODERATE_2_3
	W	0x00000003	T2_CODERATE_3_4
	W	0x00000004	T2_CODERATE_4_5
	W	0x00000005	T2_CODERATE_5_6
	W	0x00000006	T2_CODERATE_1_3
	W	0x00000007	T2_CODERATE_2_5
3~31		Reserved	--

0x698 - HALREG_DVB_T2_GUARDINTERVAL: DVB-T2 Guard Interval Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_GI_1_32
	W	0x00000001	T2_GI_1_16
	W	0x00000002	T2_GI_1_8
	W	0x00000003	T2_GI_1_4
	W	0x00000004	T2_GI_1_128
	W	0x00000005	T2_GI_19_128
	W	0x00000006	T2_GI_19_256
3~31		Reserved	--

0x699 - HALREG_DVB_T2_PILOTPATTERN: DVB-T2 Pilot Pattern Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_PP_1
	W	0x00000001	T2_PP_2
	W	0x00000002	T2_PP_3
	W	0x00000003	T2_PP_4
	W	0x00000004	T2_PP_5
	W	0x00000005	T2_PP_6
	W	0x00000006	T2_PP_7
	W	0x00000007	T2_PP_8
3~31		Reserved	--

0x69A - HALREG_DVB_T2_FECTYPE: DVB-T2 FEC Frame Length Register

Bit #	Type	Value	Name
0	W	0x00000000	T2_FEC_16200
	W	0x00000001	T2_FEC_64800
1~31		Reserved	--

7. Transform Relate Register

7.1 General Register

0x600 - HALREG_TRANSFORM_CNTL: Transform Control

Bit #	Type	Value	Name
0	W/R	0x00000001	BASE_CMD_START
1	W/R	0x00000002	BASE_CMD_STOP
2	W/R	0x00000004	BASE_CMD_TEST_START_SINE
3	W/R	0x00000008	BASE_CMD_TEST_START

4-7	--	Reserved	Reserved
8	W/R	0x00000100	BC_REBOOT
9	W/R	0x00000200	BC_REBOOT_RESCUE
10-11	--	Reserved	Reserved
12	W/R	0x00001000	BC_RFMIXER_START
13	W/R	0x00002000	BC_RFMIXER_STOP
14-30	--	Reserved	Reserved

*type W/R register: The register will be cleared after commend executed.

Description

- BASE_CMD_START: service start command.
- BASE_CMD_STOP: service stop command.
- BASE_CMD_TEST_START_SINE: use sine wave starting.
- BASE_CMD_TEST_START: test mode start.
- BASE_CMD_REBOOT: software reset command using with BASE_CMD_REBOOT_RESCURE, if user want to reset chip by software reset, can using this command without chip fail.
- BASE_CMD_REBOOT_RESCURE: software reset command using with BASE_CMD_REBOOT, if user want to reset chip by software reset, can using this command without chip fail.
- RFMIXER_CMD_START: RF start command, control by VATek chip.
- RFMIXER_CMD_STOP: RF start command, control by VATek chip.

7.2 RF Mixer Registers

0x1200 - HALREG_RF_COM_STATUS: R2 RF MIXER Status Register

Bit #	Type	Value	Name
0-1	R	0x00000001	RF_STATUS_IDLE
	R	0x00000002	RF_STATUS_ACTIVE
2-30	--	Reserved	Reserved
31	R	0x80000000	RF_STATUS_FAIL

0x1202 - HALREG_RF_COM_FREQ: R2 RF MIXER Frequency Register

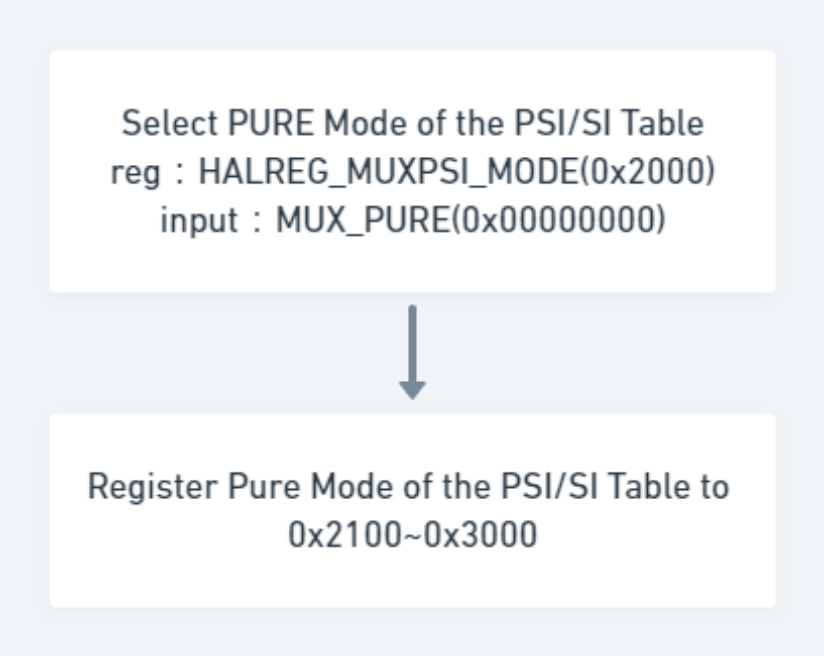
Bit #	Type	Value	Name
0-31	W/R	--	Write desired Frequency (Mhz). - Frequency minimum step is 1 MHz

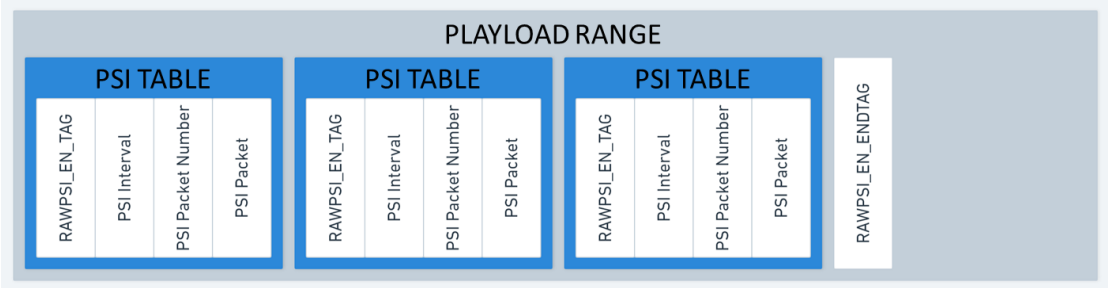
			- Frequency Range from 50Mhz ~ 950MHz

Appendix

A. Register PSI/SI table by using PSI PURE mode

Register table during 0x2100 to 0x3000，refer 5.2。



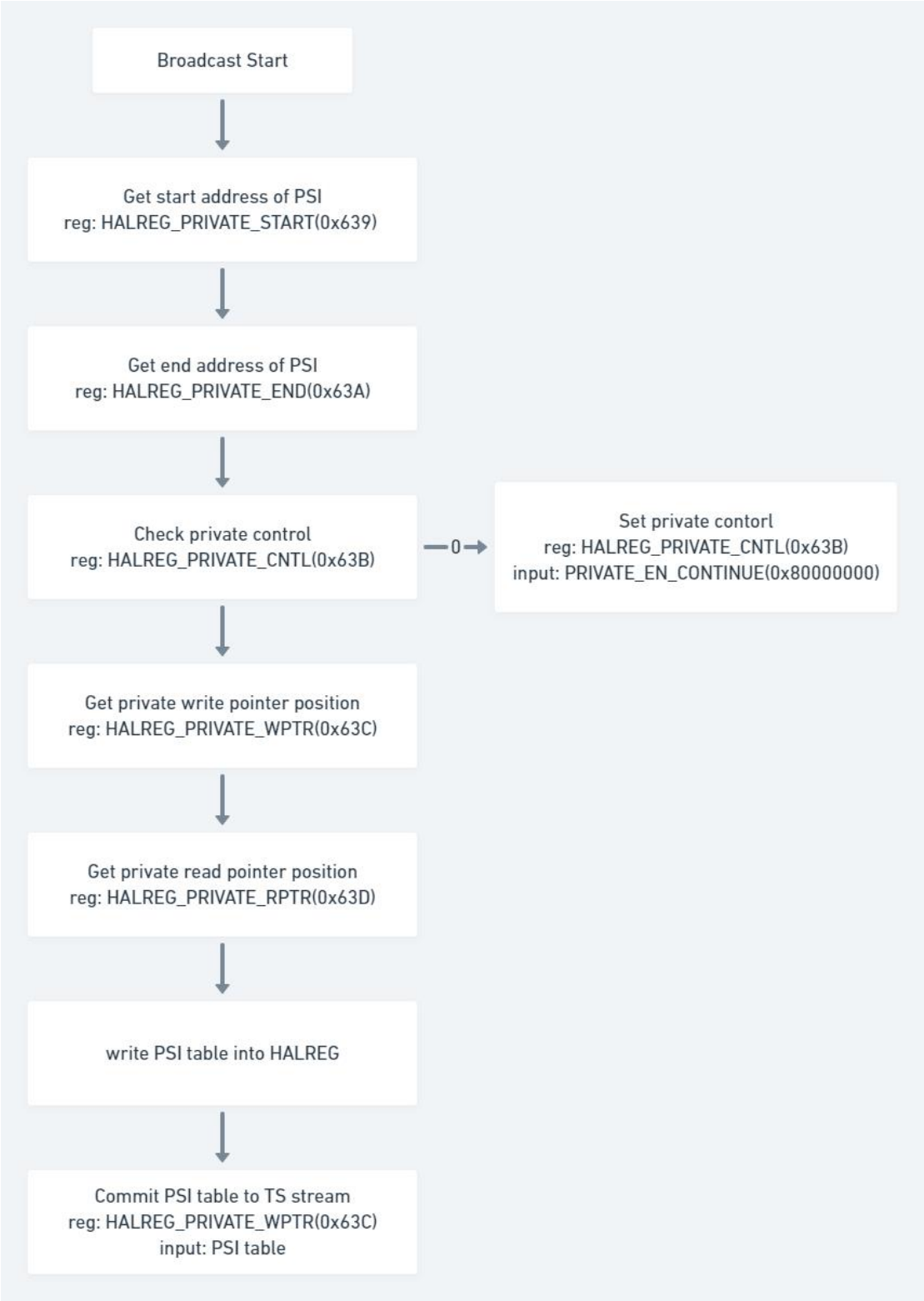


Syntax	Bits
PSITABLE_REGISTER() {	
for (i=0; i<Table_Number; i++) {	
RAWPSI_EN_TAG	32
HALOF_RAWPSI_INTERVAL	32
HALOF_RAWPSI_PACKETS	32
HALOF_RAWPSI_DATA	32*N
}	
RAWPSI_EN_ENDTAG	32
}	

Table_Number: number of register PSI/SI table，16 is maximum。
RAWPSI_EN_TAG: start tag when registering PSI/SI table。
HALOF_RAWPSI_INTERVAL: interval of transport table。
HALOF_RAWPSI_PACKETS: packet number of PSI/SI table，each packet max is 188 Bytes。
HALOF_RAWPSI_DATA: data of register PSI/SI。
RAWPSI_EN_ENDTAG: end tag of register PSI/SI。

B. Insert PSI/SI table by using PSI PURE mode

Insert table during 0x2100 to 0x3000, refer 5.3



C. RF start flow (for VATek R2)