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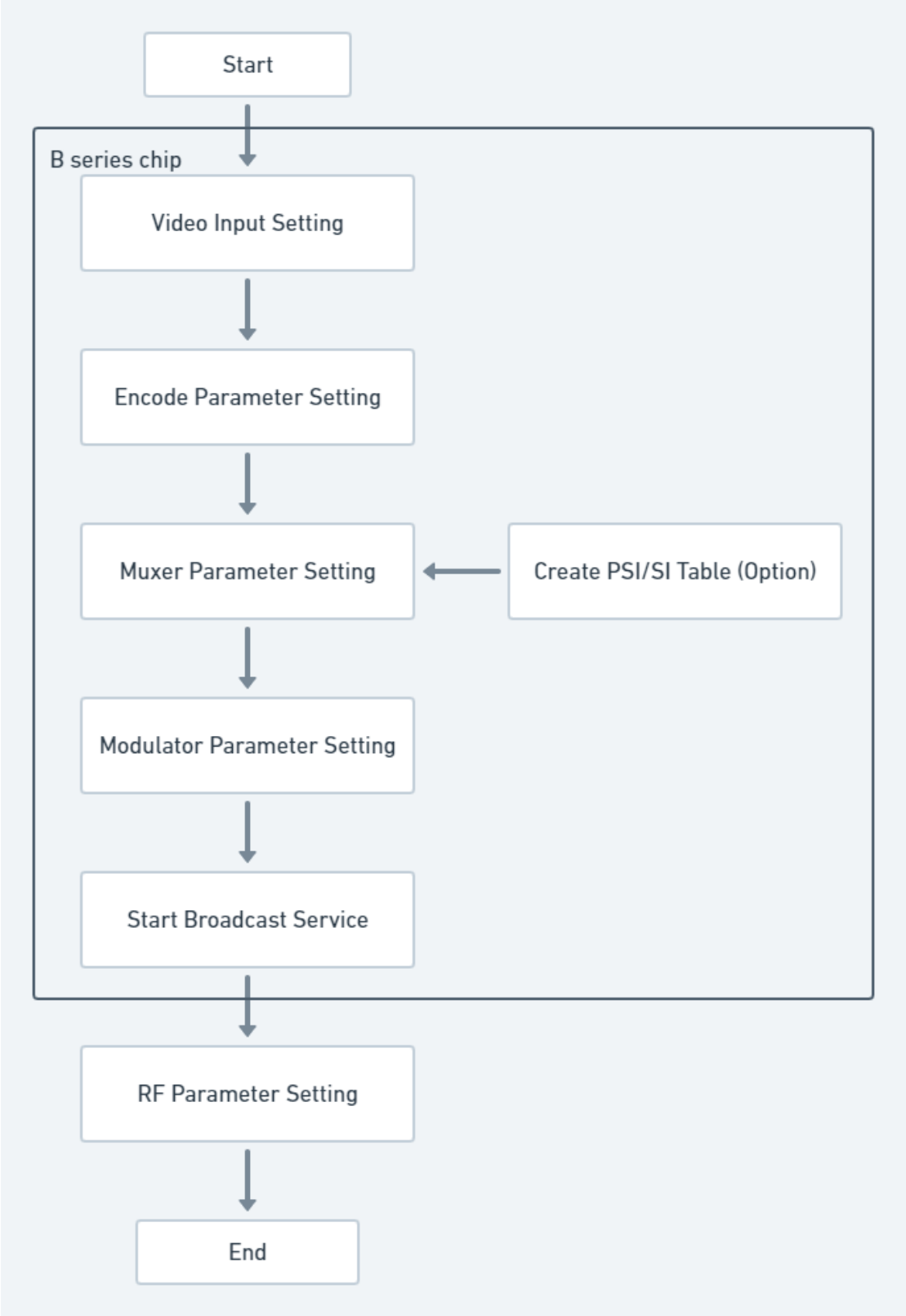
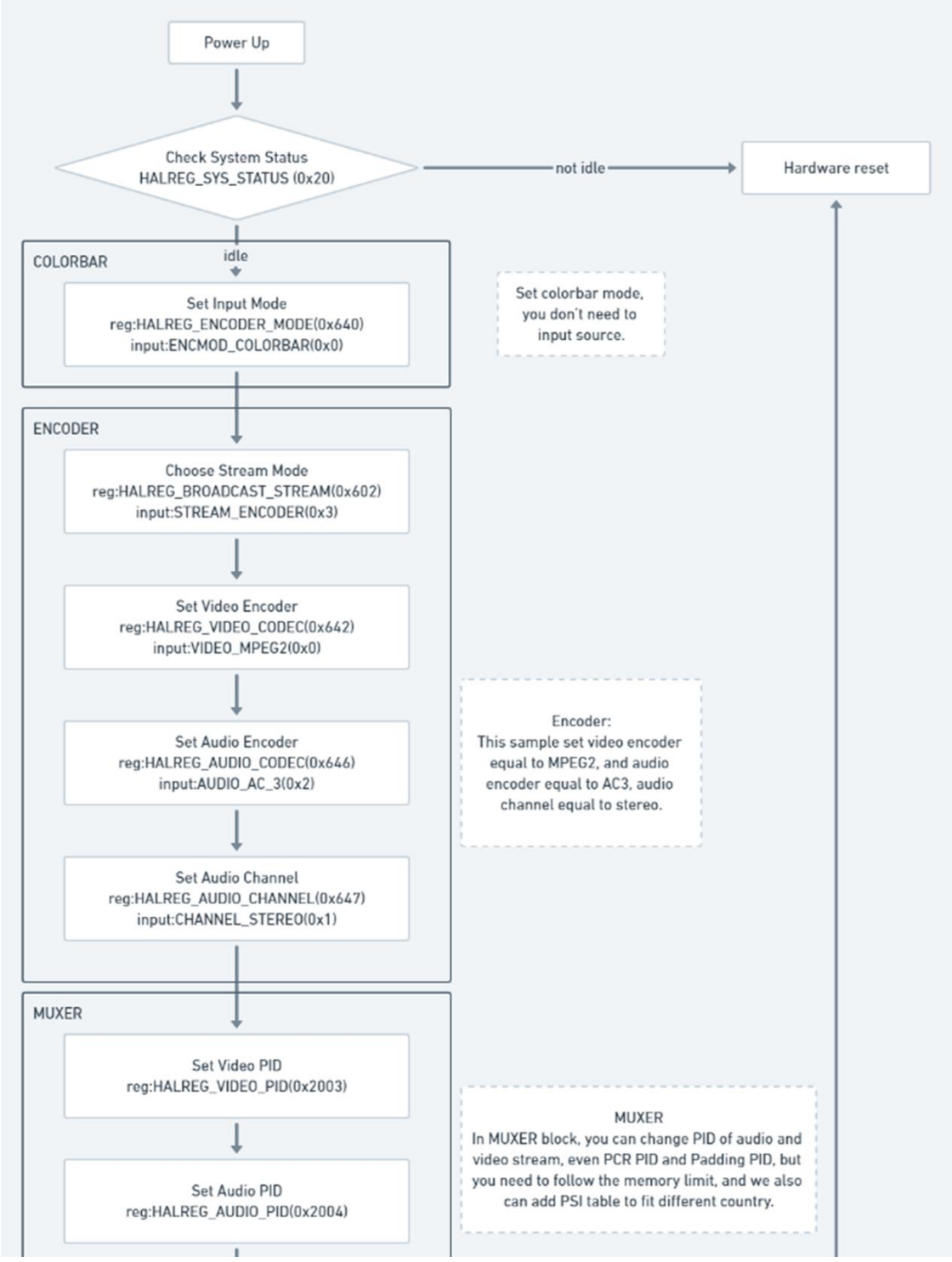
1. System Process

1.1 Process Overview



1.2 Process of chip (color bar)

You can use color bar as input source without input extra source.



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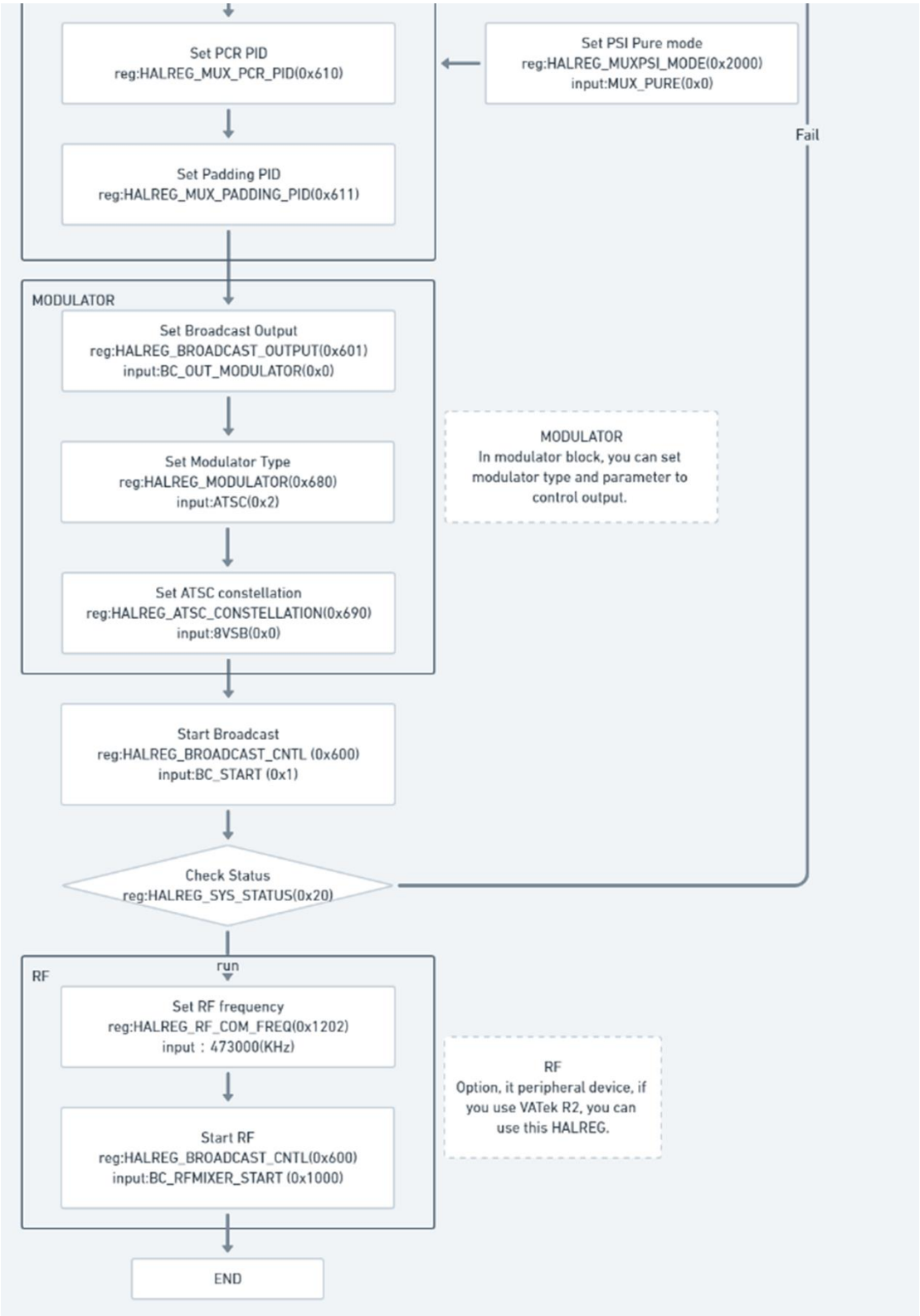
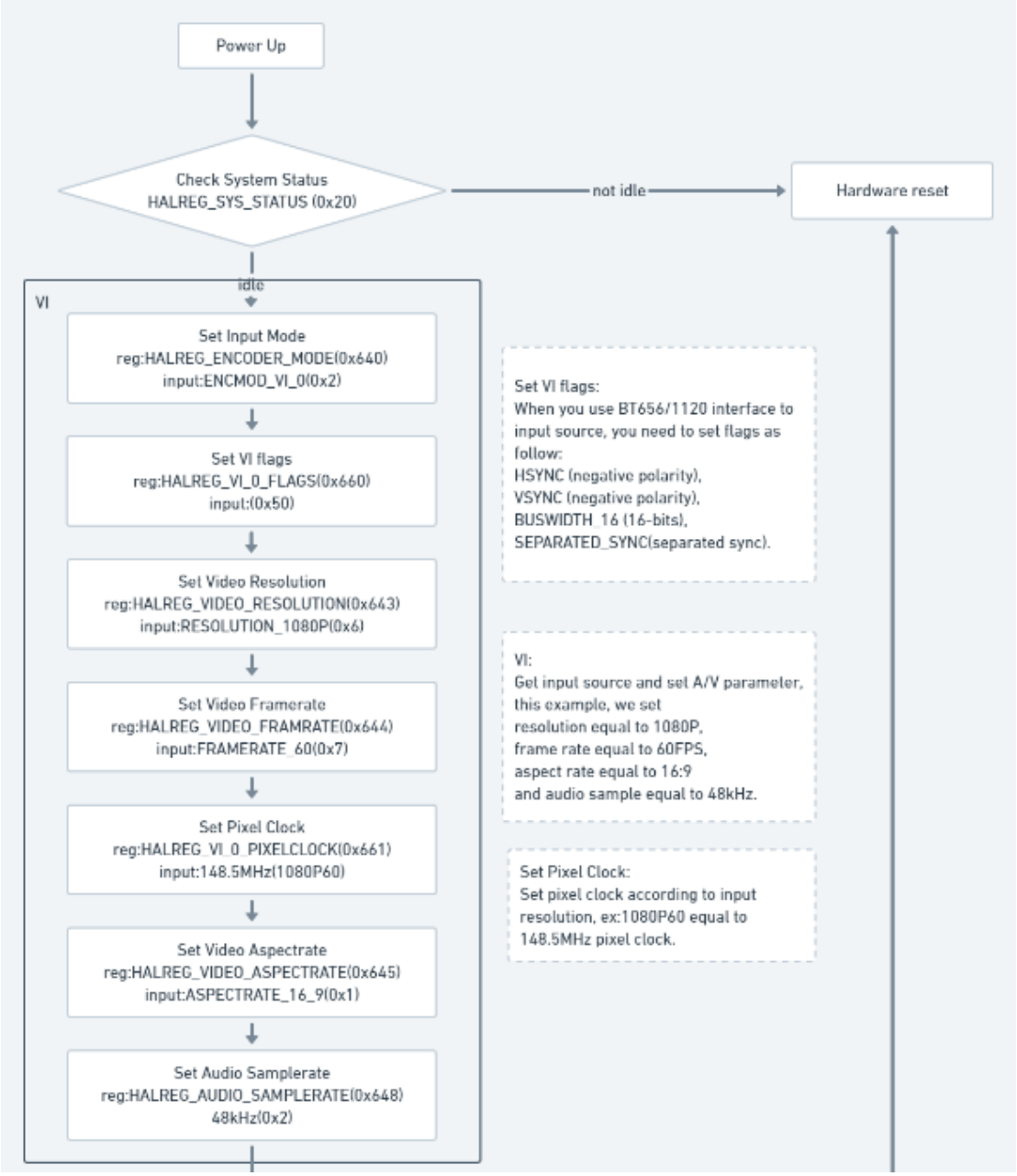


1.3 Process of chip (VI)

To using VI mode, you need to finish setting input PHY at the front end.


Power Up
Check System Status
HALREG_SYS_STATUS (0x20)
not idle
Hardware reset
idle
VI
Set Input Mode
reg:HALREG_ENCODER_MODE(0x640)
input:ENCMOD_VI_0(0x2)
Set VI flags
reg:HALREG_VI_0_FLAGS(0x660)
input:(0x50)
Set Video Resolution
reg:HALREG_VIDEO_RESOLUTION(0x643)
input:RESOLUTION_1080P(0x6)
Set Video Framerate
reg:HALREG_VIDEO_FRAMRATE(0x644)
input:FRAMERATE_60(0x7)
Set Pixel Clock
reg:HALREG_VI_0_PIXELCLOCK(0x661)
input:148.5MHz(1080P60)
Set Video Aspectrate
reg:HALREG_VIDEO_ASPECTRATE(0x645)
input:ASPECTRATE_16_9(0x1)
Set Audio Samplerate
reg:HALREG_AUDIO_SAMPLERATE(0x648)
48kHz(0x2)
Set VI flags:
When you use BT656/1120 interface to input source, you need to set flags as follow:
HSYNC (negative polarity),
VSYNC (negative polarity),
BUSWIDTH_16 (16-bits),
SEPARATED_SYNC(separated sync).
VI:
Get input source and set A/V parameter, this example, we set
resolution equal to 1080P,
frame rate equal to 60FPS,
aspect rate equal to 16:9
and audio sample equal to 48kHz.
Set Pixel Clock:
Set pixel clock according to input resolution, ex:1080P60 equal to 148.5MHz pixel clock.

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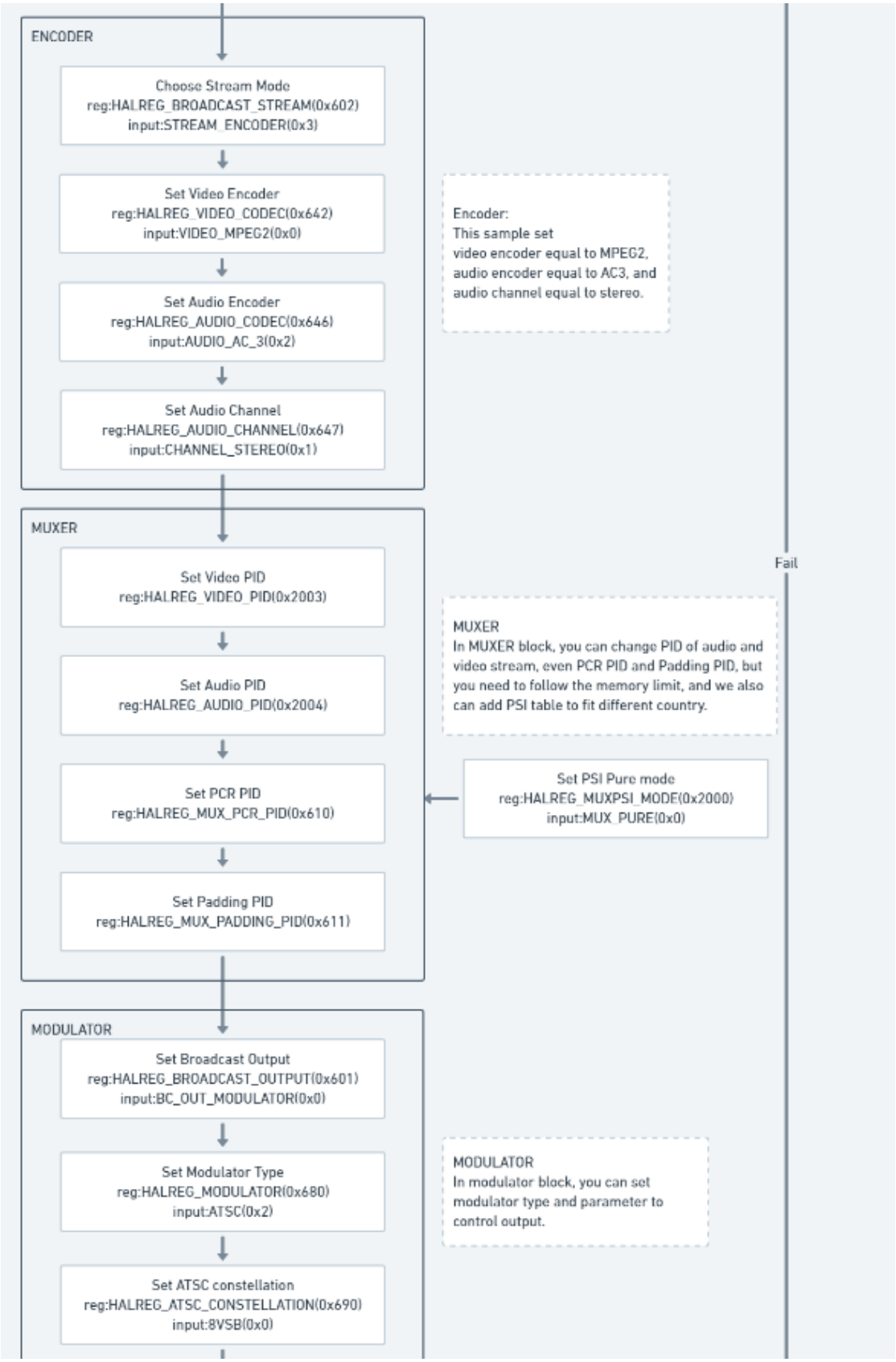
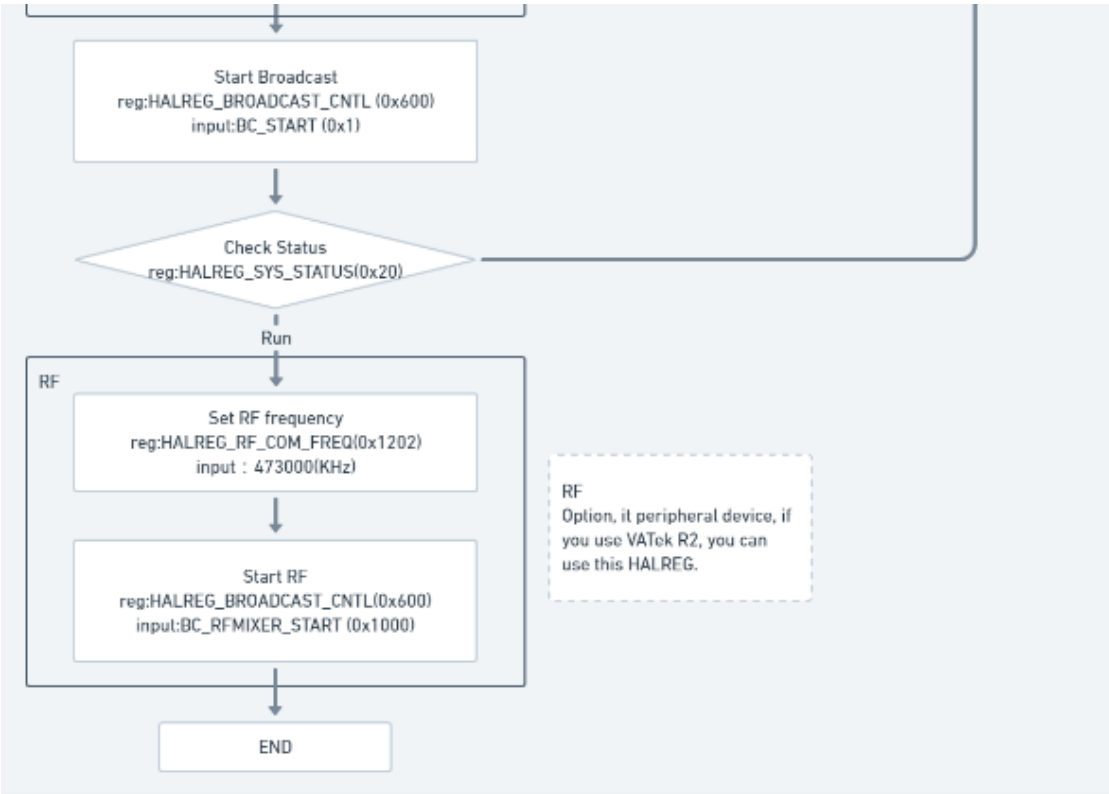

ENCODER
Choose Stream Mode
reg:HALREG_BROADCAST_STREAM(0x602)
input:STREAM_ENCODER(0x3)
Set Video Encoder
reg:HALREG_VIDEO_CODEC(0x642)
input:VIDEO_MPEG2(0x0)
Set Audio Encoder
reg:HALREG_AUDIO_CODEC(0x646)
input:AUDIO_AC_3(0x2)
Set Audio Channel
reg:HALREG_AUDIO_CHANNEL(0x647)
input:CHANNEL_STEREO(0x1)
Encoder:
This sample set
video encoder equal to MPEG2,
audio encoder equal to AC3, and
audio channel equal to stereo.
MUXER
Set Video PID
reg:HALREG_VIDEO_PID(0x2003)
Set Audio PID
reg:HALREG_AUDIO_PID(0x2004)
Set PCR PID
reg:HALREG_MUX_PCR_PID(0x610)
Set Padding PID
reg:HALREG_MUX_PADDING_PID(0x611)
Fail
MUXER
In MUXER block, you can change PID of audio and
video stream, even PCR PID and Padding PID, but
you need to follow the memory limit, and we also
can add PSI table to fit different country.
Set PSI Pure mode
reg:HALREG_MUXPSI_MODE(0x2000)
input:MUX_PURE(0x0)
MODULATOR
Set Broadcast Output
reg:HALREG_BROADCAST_OUTPUT(0x601)
input:BC_OUT_MODULATOR(0x0)
Set Modulator Type
reg:HALREG_MODULATOR(0x680)
input:ATSC(0x2)
Set ATSC constellation
reg:HALREG_ATSC_CONSTELLATION(0x690)
input:8VSB(0x0)
MODULATOR
In modulator block, you can set
modulator type and parameter to
control output.

續下頁



2. Status Registers (BASE)

2.1 System Status

0x20 - HALREG_SYS_STATUS_0: System Status Register 0

Bit #	Type	Value	Name
0~31	R	0xFF000001	SYS_STATUS_IDLE:
	R	0xFF000002	SYS_STATUS_RUN:
	R	0xFF000085	SYS_STATUS_LOADER_FAIL
	R	0xFF000086	SYS_STATUS_SERVICE_FAIL
	R	0xFF000088	SYS_STATUS_EXCEPTION_FAIL
	R	0xFF00008E	SYS_STATUS_BADSTATUS
	R	0xFF00008F	SYS_STATUS_UNKNOWN_FAIL

0x23 - HALREG_SYS_ERRCODE: System Error Code Register

Bit #	Type	Value	Name
0~31	R	0x80000001	SYS_ERRCODE_INIT
	R	0x80010001	LOADER_ERRCODE_NOAPP
	R	0x80010002	LOADER_ERRCODE_CRC32
	R	0x80010003	LOADER_ERRCODE_HW
	R	0x80020001	SERVICE_INIT_FAIL

0x24 - HALREG_CHIP_ID: CHIP ID Register

Bit #	Type	Value	Name
0~31	R	0x00010100	HAL_CHIPID_A1
	R	0x00010300	HAL_CHIPID_A3
	R	0x00020100	HAL_CHIPID_B1
	R	0x00020200	HAL_CHIPID_B2
	R	0x00020201	HAL_CHIPID_B2_PLUS
	R	0x00020300	HAL_CHIPID_B3
	R	0x00020301	HAL_CHIPID_B3_PLUS

0x25 - HALREG_FW_VER: Firmware Version Register

Bit #	Type	Value	Name
0~31	R		

0x26 - HALREG_SERVICE_MODE: Service Mode Register

Bit #	Type	Value	Name
0~31	R	0xFF000001	SERVICE_TAG_RESCUE
	R	0xF8000001	SERVICE_TAG_BROADCAST
	R	0xF8000002	SERVICE_TAG_TRANSFORM

0x27 - HALREG_PERIPHERAL_EN: Peripheral Switch Register

Bit #	Type	Value	Name
0		Reserved	
1	R	0x00000002	PERIPHERAL_FINTEKR2
2~15		Reserved	
16	R	0x00010000	PERIPHERAL_EP9555E
17	R	0x00000100	PERIPHERAL_USBBULK
18	R	0x00000200	PERIPHERAL_AUXSTREAM_USB
19	R	0x00000400	PERIPHERAL_AUXSTREAM_FLASH
20	R	0x00000800	PERIPHERAL_AUXSTREAM_TSIN
21	R	0x01000000	PERIPHERAL_CALIBRATION
22	R	0x70000000	PERIPHERAL_HWID_MASK
23~31		Reserved	

0x28 - HALREG_INPUT_SUPPORT: Media Source Register

Bit #	Type	Value	Name
0	R	0x00000001	INPUT_EN_TEST
1	R	0x00000002	INPUT_EN_USB
2	R	0x00000004	INPUT_EN_TS

3	R	0x00000008	INPUT_EN_ENC
4	R	0x00000010	VENC_EN_MPEG2
5	R	0x00000020	VENC_EN_H264
7		Reserved	
8	R	0x00000100	VENC_EN_FULLHD
9~11		Reserved	--
12	R	0x00001000	AENC_EN_MP1_L2
13	R	0x00002000	AENC_EN_AAC_LC_ADTS
14	R	0x00004000	AENC_EN_AC_3
15	R	0x00008000	AENC_EN_AAC_LC_LATM
20	R	0x00100000	TEST_EN_HW
21	R	0x00200000	TEST_EN_REMUX
22~31		Reserved	

0x29 - HALREG_OUTPUT_SUPPORT: Output Mode Register

Bit #	Type	Value	Name
0	R	0x00000001	OUTPUT_EN_MOD
1	R	0x00000002	OUTPUT_EN_SINEWAVE
2	R	0x00000004	OUTPUT_EN_TS
3	R	0x00000008	OUTPUT_EN_USB
5~7		Reserved	
8	R	0x00000100	MOD_EN_DVB_T
9	R	0x00000200	MOD_EN_J83_A
10	R	0x00000400	MOD_EN_ATSC
11	R	0x00000800	MOD_EN_J83_B
12	R	0x00001000	MOD_EN_DTMB
13	R	0x00002000	MOD_EN_ISDB_T
14	R	0x00004000	MOD_EN_J83_C
15	R	0x00008000	MOD_EN_DVB_T2
16	R	0x00005F00	MOD_EN_BASE
17~31		Reserved	

2.2 Broadcast Status

0x620 - HALREG_BCINFO_STREAM: Enable stream mode

Bit #	Type	Value	Name
3~31	W	Reserved	

0x621 - HALREG_BCINFO_OUTPUT: Enable output mode

Bit #	Type	Value	Name
1~31	W	Reserved	

0x622 - HALREG_BCINFO_MODRATE: Show output bitrate of MODULATOR.

Bit #	Type	Value	Name
0~31	R		

0x623 - HALREG_BCINFO_MUXRATE: Show output bitrate of MUX

Bit #	Type	Value	Name
0~31	R		

0x624 - HALREG_BCINFO_STATUS: Broadcast Status Register

Bit #	Type	Value	Name
0~1	R	0x00000000	BCSTATUS_IDLE
	R	0x00000001	BCSTATUS_WAIT_SOURCE
	R	0x00000002	BCSTATUS_BROADCAST
	R	0x00000003	BCSTATUS_FINISH
2~31		Reserved	
32	R	0x80000000	BCSTATUS_FAIL_UNKNOWN
	R	0x80000001	BCSTATUS_FAIL_SOURCE
	R	0x80000002	BCSTATUS_FAIL_TIMEOUT
	R	0x80000003	BCSTATUS_FAIL_CODECDROP
	R	0x80000004	BCSTATUS_FAIL_BUFFER
	R	0x80000005	BCSTATUS_FAIL_MUXER
	R	0x80000006	BCSTATUS_FAIL_ENCODE
	R	0x80000007	BCSTATUS_FAIL_MEDIA
	R	0x80000008	BCSTATUS_FAIL_DEMUX

0x625 - HALREG_BCINFO_CURRATE: Show real bitrate of MUX

Bit #	Type	Value	Name
0~31	R		

0x626 - HALREG_BCINFO_DATARATE: Show PES bitrate.

Bit #	Type	Value	Name
0~31	R		

0x627 - HALREG_BCINFO_QUERYBUF: Show buffer length.

Bit #	Type	Value	Name

0~31	R		

3.AV Control Registers (Stream Registers)

3.1 Registers for Video Input Settings

0x643 - HALREG_VIDEO_RESOLUTION: Video Encoder resolution

Bit #	Type	Value	Name
0~2	W	0x00000000	RESOLUTION_480I
	W	0x00000001	RESOLUTION_480P
	W	0x00000002	RESOLUTION_576I
	W	0x00000003	RESOLUTION_576P
	W	0x00000004	RESOLUTION_720P
	W	0x00000005	RESOLUTION_1080I
	W	0x00000006	RESOLUTION_1080P
3~31		Reserved	

0x644 - HALREG_VIDEO_FRAMERATE: Video Encoder framerate

Bit #	Type	Value	Name
0~2	W	0x00000000	FRAMERATE_23_97
	W	0x00000001	FRAMERATE_24
	W	0x00000002	FRAMERATE_25
	W	0x00000003	FRAMERATE_29_97
	W	0x00000004	FRAMERATE_30
	W	0x00000005	FRAMERATE_50
	W	0x00000006	FRAMERATE_59_94
	W	0x00000007	FRAMERATE_60
3~31		Reserved	

0x645 - HALREG_VIDEO_ASPECTRATE: Video Encoder aspect rate

Bit #	Type	Value	Name
0	W	0x00000000	ASPECTRATE_4_3
	W	0x00000001	ASPECTRATE_16_9
1~31		Reserved	

0x647 - HALREG_AUDIO_CHANNEL: Audio Encode Mode Select Register

Bit #	Type	Value	Name
0~2	W	0x00000000	CHANNEL_MUTE

	W	0x00000001	CHANNEL_STEREO
	W	0x00000002	CHANNEL_MONO_L
	W	0x00000003	CHANNEL_MONO_R
	W	0x00000004	CHANNEL_STEREO_MONO_L
	W	0x00000005	CHANNEL_STEREO_MONO_R
3~31		Reserved	--

0x648 - HALREG_AUDIO_SAMPLERATE: Audio Sample Rate Register

Bit #	Type	Value	Name
0~1	W	0x00000000	SAMPLERATE_32KHZ
	W	0x00000001	SAMPLERATE_44_1KHZ
	W	0x00000002	SAMPLERATE_48KHZ
3~31		Reserved	

0x660 - HALREG_VI_0_FLAGS: Video Interface Setup Register

Bit #	Type	Value	Name
0~3		Reserved	
4	W	0x00000010	VI_BUSWIDTH_16
5		Reserved	--
6	W	0x00000040	VI_SEPARATED_SYNC
7~8		Reserved	--
9	W	0x00000200	VI_CLK_INVERSE
10	W	0x00000400	VI_HSYNC_INVERSE
11		Reserved	--
12	W	0x00001000	VI_VSYNC_INVERSE
13~23		Reserved	--
24	W	0x01000000	VI_FIELDID_SIGNAL
25~27		Reserved	
28	W	0x10000000	VI_EXT_HALF_FPS
29	W	0x20000000	VI_FIELD_INVERSE

Description

- VI_BUSWIDTH_16: setting output base on PHY, default is 0. 0 is 8-bits data; 1 is 16-bits data.
- VI_SEPARATED_SYNC: setting output base on PHY, default is 0。0 is Embedded Sync; 1 is Separated Sync.
- VI_CLK_INVERSE: setting output base on PHY, default is 0. 0 is trigger at rising edge; 1 is trigger at falling edge.

- VI_HSYNC_INVERSE: setting output base on PHY, default is 0. 0 is Negative Polarity; 1 is Positive Polarity.
- VI_VSYNC_INVERSE: setting output base on PHY, default is 0. 0 is Negative Polarity; 1 is Positive Polarity。
- VI_FIELDID_SIGNAL: setting output base on PHY, default is 0. 0 is using Field ID pin; 1 is detecting Field ID from timing.
- VI_EXT_HALF_FPS: minus half frame rate from input. 0 is disable; 1 is enable.
- VI_FIELD_INVERSE: setting output base on PHY, default is 0. 0 is top field first; 1 is bottom field first.

0x661 - HALREG_VI_0_PIXELCLOCK: Video Input Pixel Clock Register

Bit #	Type	Value	Name
0~31	W		

3.2 Registers for AV Encoder Settings

0x602 - HALREG_BROADCAST_STREAM: Setting stream mode

Bit #	Type	Value	Name
0	W	0x00000003	STREAM_ENCODER
1	W	0x00001000	STREAM_SINE
2	W	0x00001001	STREAM_TEST
2~31		Reserved	--

0x640 - HALREG_ENCODER_MODE: Encoder Mode Control Register

Bit #	Type	Value	Name
0	W	0x00000000	ENCMOD_COLORBAR
1	W	0x00000001	ENCMOD_BOOTLOGO
2	W	0x00000002	ENCMOD_VI_0
3~31		Reserved	--

Description

- ENCMOD_COLORBAR: use SMPTE COLORBAR to be the output.
- ENCMOD_BOOTLOGO: use boot logo to be the output which already store in v2img firmware file by user.

- ENCMOD_VI_0: use real input source from HDMI or CVBS interface

0x641 - HALREG_ENCODER_FLAGS: Encoder Mode Switch Register

Bit #	Type	Value	Name
0		Reserved	
1	W	0x00000001	ENC_EN_DISABLE_DEINTERLACED
2	W	0x00000004	ENC_EN_PROGRESSIVE_2_I
3	W	0x00000008	ENC_EN_DISABLE_ADTS_CRC
4	W	0x00000100	ENC_DIS_LATENCY_Q
4~31		Reserved	--

Description

- ENC_EN_DISABLE_DEINTERLACED: specific function in chip of B3+ combine H1 HDMI PHY, if user want to input interlaced format and don't need to change format, user can enable this function.
- ENC_EN_PROGRESSIVE_2_I: change progressive format to interlaced format and output interlaced format, 0 is disable, 1 is enable.
- ENC_EN_DISABLE_ADTS_CRC: in ADTS audio encoder, it needs to check, use this flag will skip the check and output audio information, 0 is disable, 1 is enable.
- ENC_DIS_LATENCY_Q: user can remove relation of latency and quantity by enable this flag.

0x642 - HALREG_VIDEO_CODEC: Encoder format

Bit #	Type	Value	Name
0~1	W	0x00000000	VIDEO_MPEG2
	W	0x00000001	VIDEO_H264
2~31		Reserved	

0x646 - HALREG_AUDIO_CODEC: Audio Encoder format

Bit #	Type	Value	Name
0~1	W	0x00000000	AUDIO_MP1_L2
	W	0x00000001	AUDIO_AAC_LC_ADTS
	W	0x00000002	AUDIO_AC_3

	W	0x00000003	AUDIO_AAC_LC_LATM
2~31		Reserved	

0x2002 - HALREG_ENCODER_PMTPID: set PMT PID in default mode.

Bit #	Type	Value	Name
0~31	W		

0x2003 - HALREG_VIDEO_PID: set PID of video PES

Bit #	Type	Value	Name
0~31	W		

0x2004 - HALREG_AUDIO_PID: set PID of audio PES

Bit #	Type	Value	Name
0~31	W		

4. MUXER register

4.1 Mux Related Settings

0x610 - HALREG_MUX_PCR_PID: set PID of PCR

Bit #	Type	Value	Name
0~31	W		

0x611 - HALREG_MUX_PADDING_PID: set PID of padding buffer

Bit #	Type	Value	Name
0~31	W		

0x612 - HALREG_MUX_BITRATE: set limitation of MUX bitrate

Bit #	Type	Value	Name
0~31	W		

0x630 – HALREG_AUXDATA_CNTL: use in BML async mode

Bit #	Type	Value	Name
0~1	W	0x00000001	AUXDATA_EN_STOP
2~31		Reserved	

Description

AUXDATA_EN_STOP: if you use BML async mode, you need to write this flag in HALREG, and update BML stream.

0x631 - HALREG_AUXDATA_STATUS:

Bit #	Type	Value	Name
0	R	0x00000000	AUXDATA_IDLE
1	R	0x00000001	AUXDATA_ASYNC
2	R	0x00000002	AUXDATA_SYNC
3~31		Reserved	-

0x632 - HALREG_AUXDATA_PACHETNUMS: BML stream packet numbers

Bit #	Type	Value	Name
0~31		Reserved	

0x2000 - HALREG_MUXPSI_MODE: Produce mode of PSI

Bit #	Type	Value	Name
0~2	W	0x00000000	MUX_PURE
3~31		Reserved	

Description

MUX_PURE: set PSI mode as PURE mode, VATEK provide PURE mode, user can set PSI table create by themselves.

5. PSI Register

5.1 Playload Buffer Register

0x2100 - HALRANGE_PLAYLOAD_START: register of register PSI/SI table start tag, it's start at 0x2100.

Bit #	Type	Value	Name
0~31	W		

0x3000 - HALRANGE_PLAYLOAD_END: register of register PSI/SI table end tag, it's end at 0x3000

Bit #	Type	Value	Name
0~31	W		

5.2 PSI Pure Mode

Please follow appendix A

0x00 - HALOF_RAWPSI_TAG: start and end tag in PSI PURE mode, you need to use start tag when writing new PSI table, and use end tag

after finishing table.

Bit #	Type	Value	Name
0~31	W	0xFF070600	RAWPSI_EN_TAG
	W	0xFF0706FF	RAWPSI_EN_ENDTAG

0x01 - HALOF_RAWPSI_INTERVAL: PSI Table Interval Time (ms)

Bit #	Type	Value	Name
0~31	W		

0x02 - HALOF_RAWPSI_PACKETS: PSI Table packet size

Bit #	Type	Value	Name
0~31	W		

0x03 – HALOF_RAWPSI_DATA: write PSI table data continuously

Bit #	Type	Value	Name
0~31	W		

5.3 Private PSI table

Please follow appendix B

Private PSI table is the way in PURE mode, it's only can be inserted table after chip start broadcast, but private PSI provide dynamically modify and insert table.

0x639 – HALREG_PRIVATE_START: private stream playload start address

Bit #	Type	Value	Name
0~31	W		

0x63A – HALREG_PRIVATE_END: private stream playload end address

Bit #	Type	Value	Name
0~31	W		

0x063B – HALREG_PRIVATE_CNTL: private stream control

Bit #	Type	Value	Name
0	W	0x80000000	PRIVATE_EN_CONTINUE
1	W	0x00000001	PRIVATE_EN_TIMES
2~31	W		

Description

- PRIVATE_EN_CONTINUE: when write and read pointer are not equal, user can use this flag to send PSI table to chip.
- PRIVATE_EN_TIMES: set PRIVATE_EN_TIMES can insert table one time after broadcast start.

0x63C – HALREG_PRIVATE_WPTR: Private stream write pointer (update by user)

Bit #	Type	Value	Name
0~31	W		

0x63D – HALREG_PRIVATE_RPTR: private stream read pointer (update by hardware)

Bit #	Type	Value	Name
0~31	R		

6. Modulator Register

6.1 Modulator Related Settings

0x601 - HALREG_BROADCAST_OUTPUT: Broadcast Output Mode Register

Bit #	Type	Value	Name
0	W	0x00000003	RUNMODE_BROADCAST
1~31		Reserved	--

0x680 - HALREG_MOD_MOD: Modulation Standard Register

Bit #	Type	Value	Name
0~3	W	0x00000000	MOD_DVB_T
	W	0x00000001	MOD_J83A
	W	0x00000002	MOD_ATSC
	W	0x00000003	MOD_J83B
	W	0x00000004	MOD_DTMB
	W	0x00000005	MOD_ISDB_T
	W	0x00000006	MOD_J83C
	W	0x00000007	MOD_DVB_T2
4~31		Reserved	

0x681 - HALREG_MOD_IFMODE: Modulation Switch Register

Bit #	Type	Value	Name
0~1	W	0x00000001	IFMODE_DISABLE
	W	0x00000003	IFMODE_IQ_OFFSET
2~31		Reserved	

Description

IFMODE_IQ_OFFSET: If you want to use ISDB-T modulator type, you should use IFMODE_IQ_OFFSET function. VATEK provide baseband offset function, you can set offset value

0x682 - HALREG_MOD_IFFREQ: baseband offset setting register

Bit #	Type	Value	Name
	W		

Description

VATEK provide baseband offset function, you can set offset value when you use IFMODE_IQ_OFFSET function, it’s usually use in ISDB-T modulator type.

0x683 - HALREG_MOD_DACGAIN: DAC gain setting register

Bit #	Type	Value	Name
0	W	0x00000000	DACGAIN_DEFAULT
1~31	W		

Description

VATEK provide the default DACGAIN value, but user also can modify DACGAIN value by using this HAL register.

0x684 - HALREG_MOD_BW_SB: Modulator bandwidth or symbol rate setting register

Bit #	Type	Value	Name
1~31	W		

6.2 DVB-T Settings

0x690 - HALREG_DVB_T_CONSTELLATION: DVB-T Constellation Register

Bit #	Type	Value	Name
0	W	0x00000000	DVB_T_QPSK
1	W	0x00000002	DVB_T_QAM16
2	W	0x00000004	DVB_T_QAM64
3~31		Reserved	--

0x691 - HALREG_DVB_T_FFT: DVB-T Carrier Mode Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DVB_T_FFT2K
	W	0x00000001	DVB_T_FFT8K
2~31		Reserved	--

0x692 - HALREG_DVB_T_GUARDINTERVAL: DVB-T Guard Interval Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DVB_T_GI_1_32
	W	0x00000001	DVB_T_GI_1_16
	W	0x00000002	DVB_T_GI_1_8
	W	0x00000003	DVB_T_GI_1_4
2~31		Reserved	--

0x693 - HALREG_DVB_T_CODERATE: DVB-T Code Rate Register

Bit #	Type	Value	Name
0~2	W	0x00000000	DVB_T_CODERATE_1_2
	W	0x00000001	DVB_T_CODERATE_2_3
	W	0x00000002	DVB_T_CODERATE_3_4
	W	0x00000003	DVB_T_CODERATE_5_6
	W	0x00000004	DVB_T_CODERATE_7_8
3~31		Reserved	--

6.3 DVB-C (J83A) Settings

0x690 - HALREG_J83A_CONSTELLATION: DVB-C (J83.A) Constellation Register

Bit #	Type	Value	Name
0~2	W	0x00000000	J83A_QAM16
	W	0x00000001	J83A_QAM32
	W	0x00000002	J83A_QAM64
	W	0x00000003	J83A_QAM128
	W	0x00000004	J83A_QAM_256
3~31		Reserved	--

6.4 ATSC (8VSB) Settings

0x690 - HALREG_ATSC_ CONSTELLATION: ATSC (8VSB) Constellation Register

Bit #	Type	Value	Name
0	W	0x00000000	ATSC_8VSB
1~31		Reserved	--

6.5 Clear QAM (J83.B) Settings

0x690 - HALREG_J83B_CONSTELLATION: Clear QAM(J83B) Constellation Register

Bit #	Type	Value	Name
0~1	W	0x00000001	J83B_QAM64
	W	0x00000003	J83B_QAM256
2~31		Reserved	--

6.6 DTMB Settings

0x690 - HALREG_DTMB_CONSTELLATION: DTMB Constellation Register

Bit #	Type	Value	Name
0~2	W	0x00000000	DTMB_QPSK
	W	0x00000001	DTMB_QAM16
	W	0x00000002	DTMB_QAM64
	W	0x00000004	DTMB_QAM32
3~31		Reserved	--

0x691 - HALREG_DTMB_TIME_INTERLEAVED: DTMB Time

Interleaved Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DTMB_TI_DISABLE
	W	0x00000001	Reserved
	W	0x00000002	DTMB_TI_240
	W	0x00000003	DTMB_TI_720
2~31		Reserved	--

0x692 - HALREG_DTMB_CODERATE: DTMB Code Rate Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DTMB_CODERATE_0_4
	W	0x00000001	DTMB_CODERATE_0_6
	W	0x00000002	DTMB_CODERATE_0_8
2~31		Reserved	--

0x693 - HALREG_DTMB_CARRIERMODE: DTMB Carrier Register

Bit #	Type	Value	Name
0	W	0x00000000	DTMB_CARRIER_3780
	W	0x00000001	DTMB_CARRIER_1
1~31		Reserved	--

0x694 - HALREG_DTMB_SYNCFRAME: DTMB Sync Frame Mode Register

Bit #	Type	Value	Name
0~1	W	0x00000000	DTMB_SYNC_420
	W	0x00000001	DTMB_SYNC_945
	W	0x00000002	DTMB_SYNC_595
2~31		Reserved	--

6.7 ISDB-T Settings

0x690 - HALREG_ISDB_T_CONSTELLATION: ISDB-T Constellation Register

Bit #	Type	Value	Name
0~1	W	0x00000000	ISDB_T_DQPSK
	W	0x00000001	ISDB_T_QPSK
	W	0x00000002	ISDB_T_QAM16
	W	0x00000003	ISDB_T_QAM64

2~31		Reserved	--

0x691 - HALREG_ISDB_T_FFT: ISDB-T Carrier Mode Register

Bit #	Type	Value	Name
0~1	W	0x00000000	ISDB_T_FFT2K
	W	0x00000001	ISDB_T_FFT8K
	W	0x00000002	ISDB_T_FFT4K
2~31		Reserved	--

0x692 - HALREG_ISDB_T_GUARDINTERVAL: ISDB-T Guard Interval Register

Bit #	Type	Value	Name
0~1	W	0x00000000	ISDB_T_GI_1_32
	W	0x00000001	ISDB_T_GI_1_16
	W	0x00000002	ISDB_T_GI_1_8
	W	0x00000003	ISDB_T_GI_1_4
2~31		Reserved	--

0x693 - HALREG_ISDB_T_CODERATE: ISDB-T Code Rate Register

Bit #	Type	Value	Name
0~2	W	0x00000000	ISDB_T_CODERATE_1_2
	W	0x00000001	ISDB_T_CODERATE_2_3
	W	0x00000002	ISDB_T_CODERATE_3_4
	W	0x00000003	ISDB_T_CODERATE_5_6
	W	0x00000004	ISDB_T_CODERATE_7_8
3~31		Reserved	--

0x694 - HALREG_ISDB_T_TIME_INTERLEAVED: ISDB-T Time Interleave Register

Bit #	Type	Value	Name
0~1	W	0x00000000	ISDB_T_TI_DISABLE
	W	0x00000001	ISDB_T_TI_MODE1
	W	0x00000002	ISDB_T_TI_MODE2
	W	0x00000003	ISDB_T_TI_MODE3
2~31		Reserved	--

0x695 - HALREG_ISDB_T_FLAGS: ISDB-T Flag Register

Bit #	Type	Value	Name
0~1	W	0x00000001	ISDB_T_EN_AC_1
	W	0x00000002	ISDB_T_EN_AC_2

	W	0x00000004	ISDB_T_EN_EMERGENCY
2~31		Reserved	--

6.8 J83.C Settings

0x690 - HALREG_J83C_CONSTELLATION: J83.C Constellation Register

Bit #	Type	Value	Name
0	W	Reserved	
1	W	0x00000002	J83C_QAM64
2	W	0x00000004	J83C_QAM256
3~31		Reserved	--

6.9 DVB-T2 Settings

0x691 - HALREG_DVB_T2_FLAGS: DVB-T2 Control Register

Bit #	Type	Value	Name
0	W	0x00000001	T2EN_EXTEND_CARRIER_MODE
1	W	0x00000002	T2EN_CONSTELLATION_ROTATION
2	W	0x00000004	T2EN_INPUT_TS_HEM
3	W	0x00000008	T2EN_DELETE_NULL_PACKET
4	W	0x00000010	T2EN_VBR_CODING
5	W	0x00000020	T2EN_TIME_INTERVAL
6~31		Reserved	--

0x692 - HALREG_DVB_T2_ISSY: DVB-T2 ISSY Register

Bit #	Type	Value	Name
0~1	W	0x00000000	T2_ISSY_DISABLE
	W	0x00000002	T2_ISSY_SHORT
	W	0x00000003	T2_ISSY_LONG
2~31		Reserved	--

0x693 - HALREG_DVB_T2_NIT: DVB-T2 NIT Register

Bit #	Type	Value	Name
0	W	0x00000000	T2_NTI_DISABLE
1~31		Reserved	--

0x694 - HALREG_DVB_T2_L1_CONSTELLATION: DVB-T2 L1

Constellation Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_L1_BPSK
	W	0x00000001	T2_L1_QPSK
	W	0x00000002	T2_L1_QAM16
	W	0x00000003	T2_L1_QAM64
3~31		Reserved	--

0x695 - HALREG_DVB_T2_PLP_CONSTELLATION: DVB-T2 PLP

Constellation Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_PLP_QPSK
	W	0x00000001	T2_PLP_QAM16
	W	0x00000002	T2_PLP_QAM64
	W	0x00000003	T2_PLP_QAM256
3~31		Reserved	--

0x696 - HALREG_DVB_T2_FFT: DVB-T2 Carrier Mode Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_FFT_1K
	W	0x00000001	T2_FFT_2K
	W	0x00000002	T2_FFT_4K
	W	0x00000003	T2_FFT_8K
	W	0x00000004	T2_FFT_16K
	W	0x00000005	T2_FFT_32K
3~31		Reserved	--

0x697 - HALREG_DVB_T2_CODERATE: DVB-T2 Code Rate Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_CODERATE_1_2
	W	0x00000001	T2_CODERATE_3_5
	W	0x00000002	T2_CODERATE_2_3
	W	0x00000003	T2_CODERATE_3_4
	W	0x00000004	T2_CODERATE_4_5
	W	0x00000005	T2_CODERATE_5_6
	W	0x00000006	T2_CODERATE_1_3
	W	0x00000007	T2_CODERATE_2_5
3~31		Reserved	--

0x698 - HALREG_DVB_T2_GUARDINTERVAL: DVB-T2 Guard Interval Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_GI_1_32
	W	0x00000001	T2_GI_1_16
	W	0x00000002	T2_GI_1_8
	W	0x00000003	T2_GI_1_4
	W	0x00000004	T2_GI_1_128
	W	0x00000005	T2_GI_19_128
	W	0x00000006	T2_GI_19_256
3~31		Reserved	--

0x699 - HALREG_DVB_T2_PILOTPATTERN: DVB-T2 Pilot Pattern Register

Bit #	Type	Value	Name
0~2	W	0x00000000	T2_PP_1
	W	0x00000001	T2_PP_2
	W	0x00000002	T2_PP_3
	W	0x00000003	T2_PP_4
	W	0x00000004	T2_PP_5
	W	0x00000005	T2_PP_6
	W	0x00000006	T2_PP_7
	W	0x00000007	T2_PP_8
3~31		Reserved	--

0x69A - HALREG_DVB_T2_FECTYPE: DVB-T2 FEC Frame Length Register

Bit #	Type	Value	Name
0	W	0x00000000	T2_FEC_16200
	W	0x00000001	T2_FEC_64800
1~31		Reserved	--

0x69B - HALREG_DVB_T2_NID: DVB-T2 NID Register

Bit #	Type	Value	Name
1~31		Reserved	--

0x69C - HALREG_DVB_T2_SID: DVB-T2 SID Register

Bit #	Type	Value	Name
1~31		Reserved	--

0x69D - HALREG_DVB_T2_FECBN: DVB-T2 FECBN Register

Bit #	Type	Value	Name

1~31		Reserved	--

0x69E - HALREG_DVB_T2_SBN: DVB-T2 SBN Register

Bit #	Type	Value	Name
1~31		Reserved	--

7. Broadcast Related Registers

7.1 General Settings

0x600 - HALREG_SERVICE_BASE_CNTL: Broadcast Control Register

Bit #	Type	Value	Name
0	W	0x00000001	BASE_CMD_START
1	W	0x00000002	BASE_CMD_STOP
2	W	0x00000004	BASE_CMD_TEST_START_SINE
3	W	0x00000008	BASE_CMD_TEST_START
2~7		Reserved	--
8	W	0x00000100	BASE_CMD_REBOOT
9	W	0x00000200	BASE_CMD_REBOOT_RESCURE
10~11		Reserved	
12	W	0x00001000	RFMIXER_CMD_START
13	W	0x00002000	RFMIXER_CMD_STOP
14~31		Reserved	--

Description

- BASE_CMD_START: service start command.
- BASE_CMD_STOP: service stop command.
- BASE_CMD_TEST_START_SINE: use sine wave starting.
- BASE_CMD_TEST_START: test mode start.
- BASE_CMD_REBOOT: software reset command using with BASE_CMD_REBOOT_RESCURE, if user want to reset chip by software reset, can using this command without chip fail.
- BASE_CMD_REBOOT_RESCURE: software reset command using with BASE_CMD_REBOOT, if user want to reset chip by software reset, can using this command without chip fail.
- RFMIXER_CMD_START: RF start command, control by VATek chip.
- RFMIXER_CMD_STOP: RF start command, control by VATek chip.

7.2 RF Related Settings (For VATEK R2 Control)

0x1200 - HALREG_RF_COM_STATUS: R2 Status Register

Bit #	Type	Value	Name
0	R	0x00000001	RF_STATUS_IDLE
1	R	0x00000002	RF_STATUS_ACTIVE
2~30		Reserved	
31	R	0x80000000	RF_STATUS_FAIL

0x1202 - HALREG_RF_COM_FREQ: R2 Frequency Register

Bit #	Type	Value	Name
0	W		___KHz
1~31		Reversed	

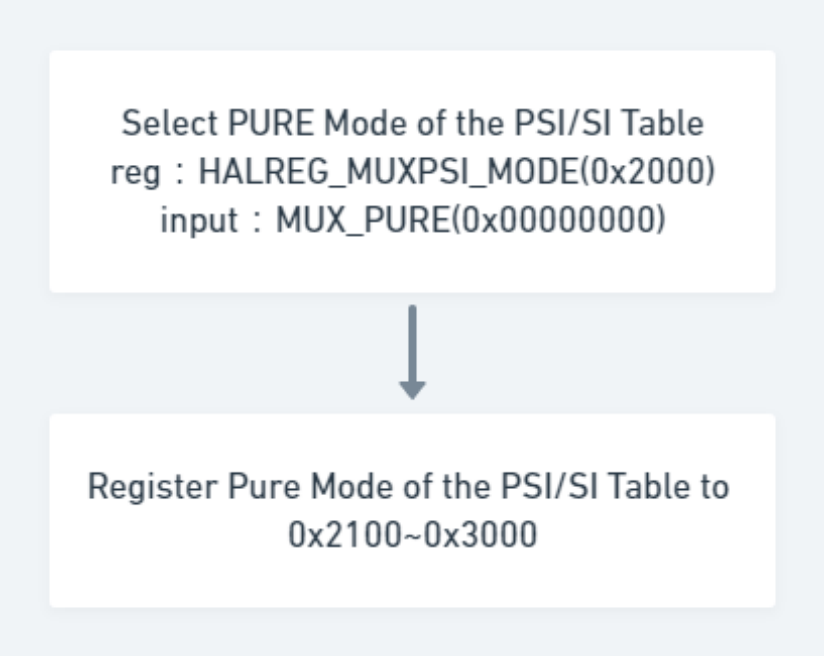
Description

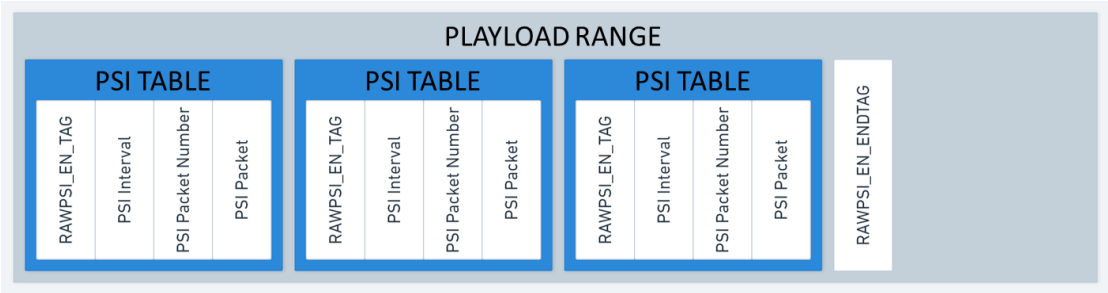
User only need to set RF frequency and write RF start command, RF will start output.

Appendix

A. Register PSI/SI table by using PSI PURE mode

Register table during 0x2100 to 0x3000，refer 5.2。



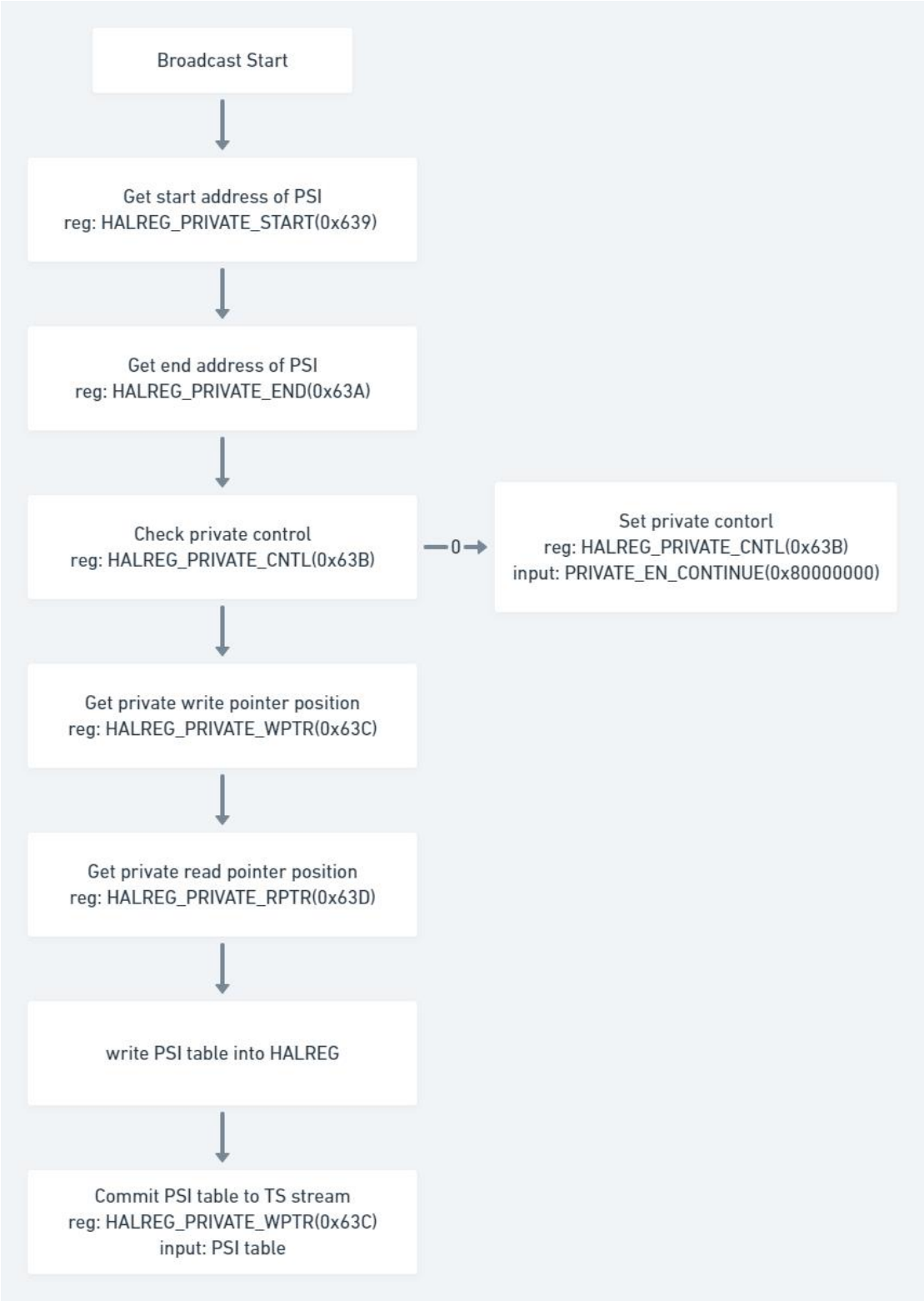


Syntax	Bits
PSITABLE_REGISTER() {	
for (i=0; i<Table_Number; i++) {	
RAWPSI_EN_TAG	32
HALOF_RAWPSI_INTERVAL	32
HALOF_RAWPSI_PACKETS	32
HALOF_RAWPSI_DATA	32*N
}	
RAWPSI_EN_ENDTAG	32
}	

Table_Number: number of register PSI/SI table，16 is maximum。
RAWPSI_EN_TAG: start tag when registering PSI/SI table。
HALOF_RAWPSI_INTERVAL: interval of transport table。
HALOF_RAWPSI_PACKETS: packet number of PSI/SI table，each packet max is 188 Bytes。
HALOF_RAWPSI_DATA: data of register PSI/SI。
RAWPSI_EN_ENDTAG: end tag of register PSI/SI。

B. Insert PSI/SI table by using PSI PURE mode

Insert table during 0x2100 to 0x3000, refer 5.3



C. RF start flow (for VATek R2)