NAME : CHETAN NARENDRA THORAT BATCH : B 10

DIV : BE (III) ROLL NO : 052

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity modncount is
    Port ( clk : in  STD_LOGIC;
           clr : in  STD_LOGIC;
           q : inout  STD_LOGIC_VECTOR (2 downto 0));
end modncount;

architecture Behavioral of modncount is
signal count: std_logic_vector(2 downto 0);
begin
```

```
process(clk)
begin
 if (clr='1') then count <= "000";

elsif (rising_edge (clk)) then
if (count="100")
then  count <= "000";

else
count<=count+ 1;
end if;
end if;
end process;
q<=count;
end Behavioral;
```

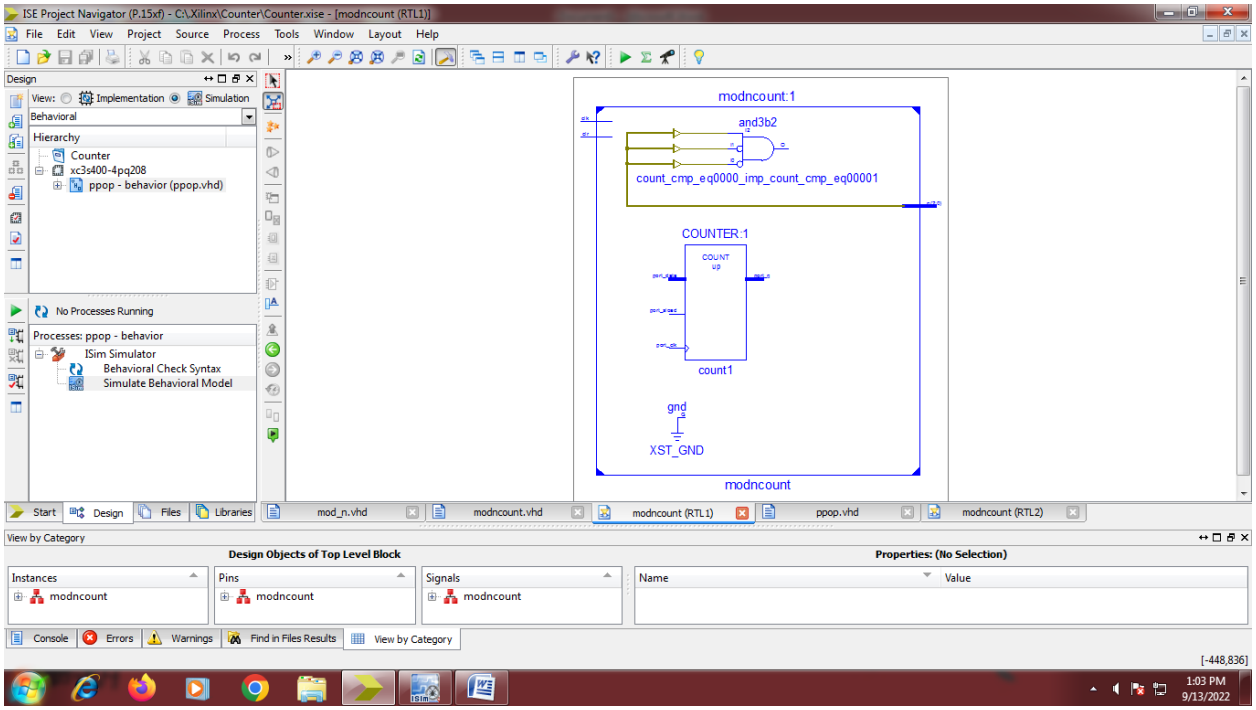
TEST BENTCH

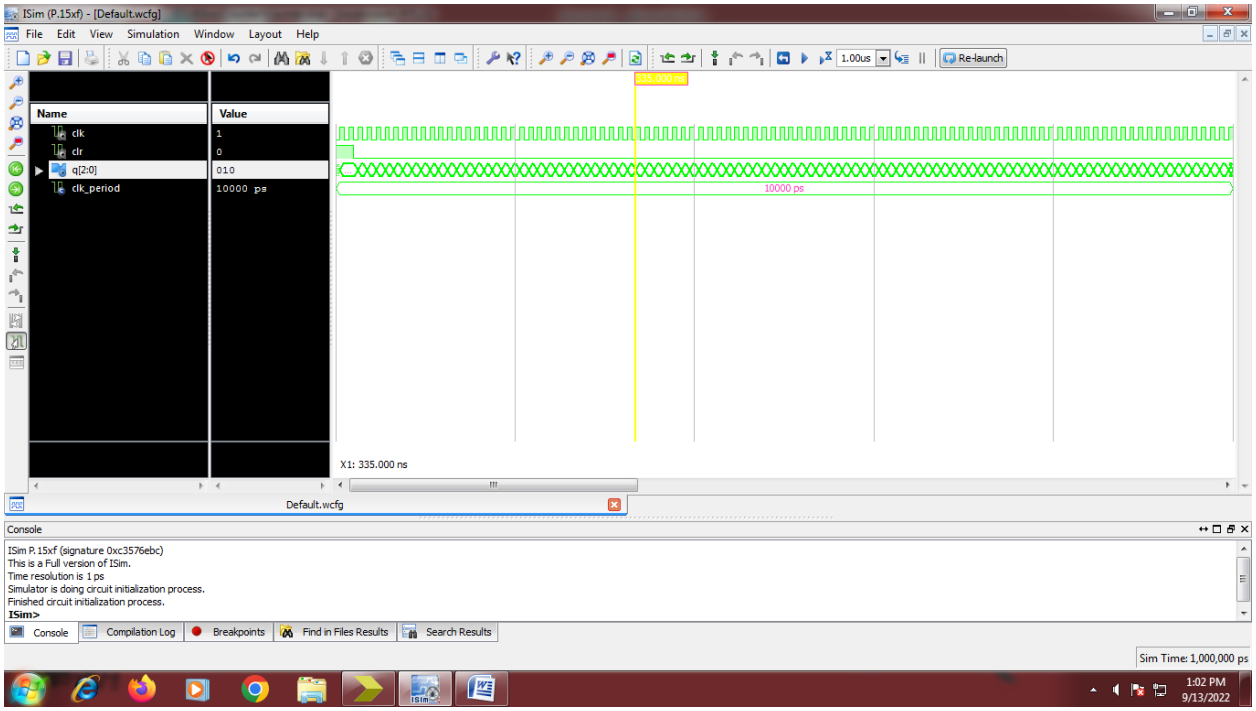
```
--------------------------------------------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;
```

```
ENTITY ppop IS

END ppop;

ARCHITECTURE behavior OF ppop IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT modncount

   PORT(

        clk : IN  std_logic;

        clr : IN  std_logic;

        q : INOUT  std_logic_vector(2 downto 0)

       );

   END COMPONENT;

  --Inputs

  signal clk : std_logic := '0';

  signal clr : std_logic := '0';


          --BiDirs

  signal q : std_logic_vector(2 downto 0);

  -- Clock period definitions

  constant clk_period : time := 10 ns;


BEGIN


          -- Instantiate the Unit Under Test (UUT)

  uut: modncount PORT MAP (
```

```
        clk => clk,
        clr => clr,
        q => q
       );
   -- Clock process definitions
   clk_process :process
   begin
                clk <= '0';
                wait for clk_period/2;
                clk <= '1';
                wait for clk_period/2;
   end process;
   -- Stimulus process
   stim_proc: process
   begin
clr<='1' ;
      -- hold reset state for 100 ns.
      wait for 20 ns;
                clr<='0' ;
      -- hold reset state for 100 ns.
      wait for 20 ns;
      wait for clk_period*10;
      -- insert stimulus here
      wait;
   end process;
```

END;


ISE Project Navigator (P.15xf) - C:\Xilinx\Counter\Counter.xise - [modncount (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
Counter
xc3s400-4pq208
ppop - behavior (ppop.vhd)
No Processes Running
Processes: ppop - behavior
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
modncount:1
and3b2
count_cmp_eq0000_imp_count_cmp_eq00001
COUNTER:1
COUNT
up
count1
gnd
XST_GND
modncount
Start Design Files Libraries
mod_n.vhd
modncount.vhd
modncount (RTL1)
ppop.vhd
modncount (RTL2)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
modncount
Console Errors Warnings Find in Files Results View by Category
[-448,836]
1:03 PM
9/13/2022


ISim (P.15xf) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
clk
1
clr
0
q[2:0]
010
clk_period
10000 ps
335.000 ns
10000 ps
X1: 335.000 ns
Default.wcfg
Console
ISim P.15xf (signature 0xc3576ebc)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps
1:02 PM
9/13/2022