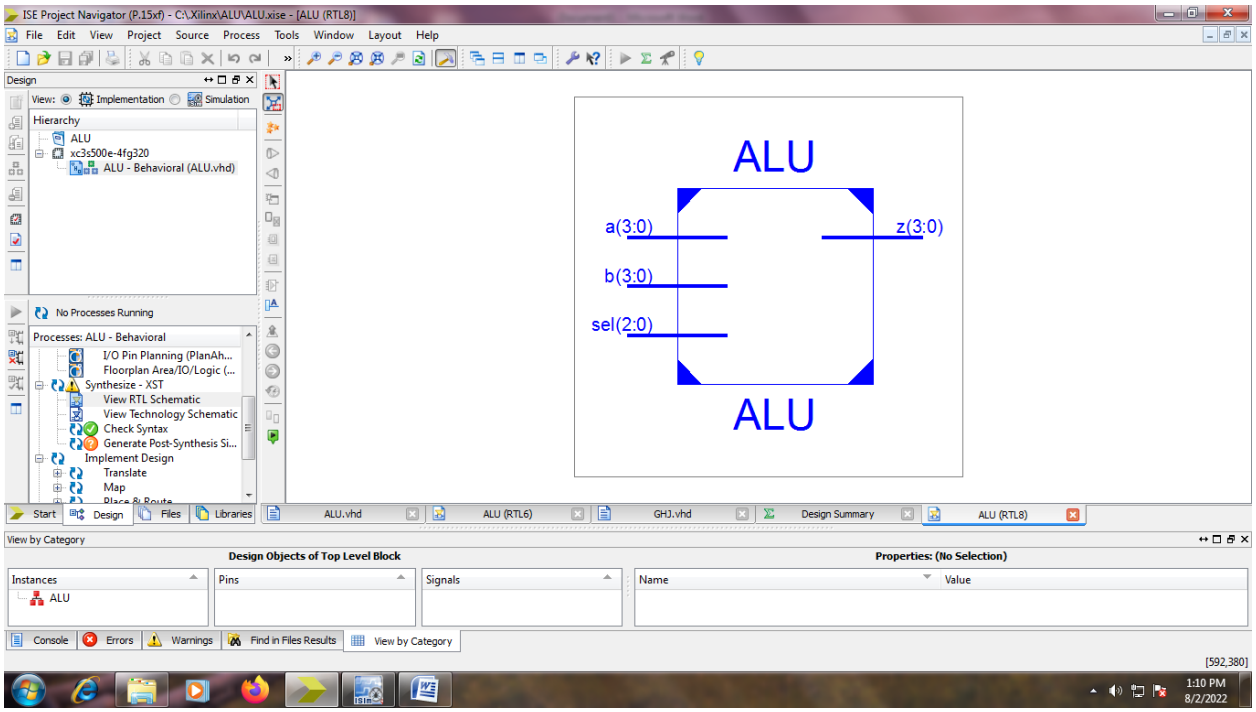
NAME: CHETAN NARENDRA THORAT ROLL NO: 052
CLASS: BE (III) BATCH: B10

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_ARITH.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity ALU is

   Port ( a : in  STD_LOGIC_VECTOR(3 DOWNTO 0);

          b : in  STD_LOGIC_VECTOR(3 DOWNTO 0);

          sel : in  STD_LOGIC_VECTOR(2 DOWNTO 0);

          z : out STD_LOGIC_VECTOR(3 DOWNTO 0));

end ALU;

architecture Behavioral of ALU is

begin

process(a,b,sel)

begin

case sel is

when "000" => z <= a+b;
```

```
when "001" => z <= a-b;

when "010" => z <= a AND b;

when "011" => z <= a OR b;

when "100" => z <= a XOR b;

when "101" => z <= a NAND b;

when "110" => z <=a;

when others => null;

end case;

end process;

end Behavioral;
```

RTL SCHEMATIC MAIN :



TEST BENCH PROGRAM :

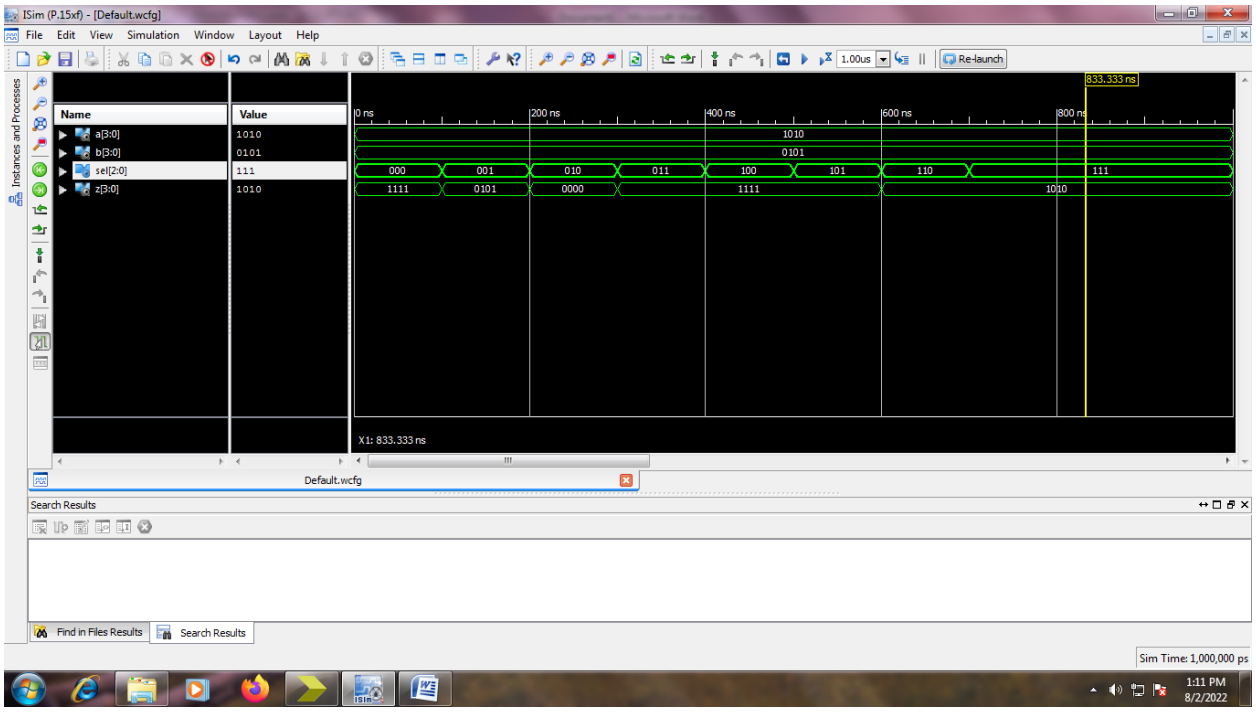
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
 -- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;
 ENTITY GHJ IS
END GHJ;
 ARCHITECTURE behavior OF GHJ IS
     -- Component Declaration for the Unit Under Test (UUT)
     COMPONENT ALU
    PORT(
         a : IN  std_logic_vector(3 downto 0);
         b : IN  std_logic_vector(3 downto 0);
         sel : IN  std_logic_vector(2 downto 0);
         z : OUT  std_logic_vector(3 downto 0)
        );
    END COMPONENT;
       --Inputs
   signal a : std_logic_vector(3 downto 0) := (others => '0');
   signal b : std_logic_vector(3 downto 0) := (others => '0');
   signal sel : std_logic_vector(2 downto 0) := (others => '0');
             --Outputs
   signal z : std_logic_vector(3 downto 0);
BEGIN
```

```
        -- Instantiate the Unit Under Test (UUT)
uut: ALU PORT MAP (
      a => a,
      b => b,
      sel => sel,
      z => z
    );
-- Stimulus process
stim_proc: process
begin
          a<="1010";
          b<="0101";
          sel<="000";
  -- hold reset state for 100 ns.
  wait for 100 ns;
                    a<="1010";
          b<="0101";
          sel<="001";
  -- hold reset state for 100 ns.
  wait for 100 ns;
                    a<="1010";
          b<="0101";
          sel<="010";
  -- hold reset state for 100 ns.
```

```
wait for 100 ns;
                a<="1010";
        b<="0101";
        sel<="011";
-- hold reset state for 100 ns.
wait for 100 ns;
                a<="1010";
        b<="0101";
        sel<="100";
-- hold reset state for 100 ns.
wait for 100 ns;
                a<="1010";
        b<="0101";
        sel<="101";
-- hold reset state for 100 ns.
wait for 100 ns;
                a<="1010";
        b<="0101";
        sel<="110";
-- hold reset state for 100 ns.
wait for 100 ns;
                a<="1010";
        b<="0101";
        sel<="111";
-- hold reset state for 100 ns.
```

```
      wait for 100 ns;
--      wait for <clock>_period*10;
      -- insert stimulus here
      wait;
   end process;
END;
```

TEST BENCH WAVEFORM :



DESIGN SUMMARY :

SYNTHESIS REPORT :

Release 14.1 - xst P.15xf (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.10 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.10 secs

--> Reading design: ALU.prj

TABLE OF CONTENTS

9.3) TIMING REPORT

```
=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "ALU.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "ALU"
Output Format                      : NGC
Target Device                      : xc3s500e-4-fg320

---- Source Options
Top Module Name                    : ALU
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
```

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 24

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

==========

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* HDL Compilation *

```
=========================================================================

Compiling vhdl file "C:/.Xilinx/ALU/ALU.vhd" in Library work.

Entity <alu> compiled.

Entity <alu> (Architecture <behavioral>) compiled.


=========================================================================

*                  Design Hierarchy Analysis                    *

=========================================================================

Analyzing hierarchy for entity <ALU> in library <work> (architecture <behavioral>).


=========================================================================

*                      HDL Analysis                         *

=========================================================================

Analyzing Entity <ALU> in library <work> (Architecture <behavioral>).

Entity <ALU> analyzed. Unit <ALU> generated.


=========================================================================

*                      HDL Synthesis                        *

=========================================================================


Performing bidirectional port resolution...


Synthesizing Unit <ALU>.
```

Related source file is "C:/.Xilinx/ALU/ALU.vhd".

WARNING:Xst:737 - Found 4-bit latch for signal <z>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

Found 4-bit addsub for signal <z$addsub0000>.

Found 4-bit 7-to-1 multiplexer for signal <z$mux0001>.

Found 4-bit xor2 for signal <z$xor0000> created at line 52.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 4 Multiplexer(s).

Unit <ALU> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

==========

HDL Synthesis Report

Macro Statistics

Adders/Subtractors : 1

4-bit addsub : 1

Latches : 1

4-bit latch : 1

Multiplexers : 1

4-bit 7-to-1 multiplexer : 1

Xors : 1

4-bit xor2 : 1

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* Advanced HDL Synthesis *

==========

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Advanced HDL Synthesis Report

Macro Statistics

Adders/Subtractors : 1

4-bit addsub : 1

Latches : 1

4-bit latch : 1

Multiplexers : 1

4-bit 7-to-1 multiplexer : 1

Xors : 1

4-bit xor2 : 1

===

===

* Low Level Synthesis *

===

Optimizing unit <ALU> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block ALU, actual ratio is 0.

Final Macro Processing ...

===

Final Register Report

Found no macro

===

===

* Partition Report *

===

Partition Implementation Status

No Partitions were found in this design.

==========

* Final Report *

==========

Final Results

RTL Top Level Output File Name : ALU.ngr

Top Level Output File Name : ALU

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 15

Cell Usage :

BELS : 25

LUT3 : 9

LUT4 : 11

MUXF5 : 5

FlipFlops/Latches : 4

```
#      LD_1                    : 4
# IO Buffers                   : 15
#      IBUF                    : 11
#      OBUF                    : 4
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s500efg320-4

 Number of Slices:                      11  out of   4656     0%
 Number of 4 input LUTs:                20  out of   9312     0%
 Number of IOs:                         15
 Number of bonded IOBs:                 15  out of    232     6%
   IOB Flip Flops:                      4

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

===

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
z_cmp_eq0000(z_cmp_eq00001:O)	NONE(*)(z_0)	4

(*) This 1 clock signal(s) are generated by combinatorial logic,

and XST is not able to identify which are the primary clock signals.

Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.

INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: 8.521ns

Maximum output required time after clock: 4.368ns

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

===

Timing constraint: Default OFFSET IN BEFORE for Clock 'z_cmp_eq0000'

Total number of paths / destination ports: 77 / 4

Offset: 8.521ns (Levels of Logic = 7)

Source: sel<0> (PAD)

Destination: z_3 (LATCH)

Destination Clock: z_cmp_eq0000 rising

Data Path: sel<0> to z_3

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)

```
    ----------------------------------------  ------------
    IBUF:I->O           11   1.218   1.012  sel_0_IBUF (sel_0_IBUF)
    LUT3:I1->O           3   0.704   0.531  z_mux00001 (z_mux00001)
    MUXF5:S->O           2   0.739   0.622  Maddsub_z_addsub0000_cy<1>1_f5
(Maddsub_z_addsub0000_cy<1>)
    LUT4:I0->O           1   0.704   0.455  Maddsub_z_addsub0000_xor<3>11_SW0 (N10)
    LUT3:I2->O           1   0.704   0.499  Maddsub_z_addsub0000_xor<3>11 (z_addsub0000<3>)
    LUT3:I1->O           1   0.704   0.000  Mmux_z_mux0001_43 (Mmux_z_mux0001_43)
    MUXF5:I0->O          1   0.321   0.000  Mmux_z_mux0001_2_f5_2 (z_mux0001<3>)
    LD_1:D                   0.308          z_3
    ----------------------------------------
    Total                    8.521ns (5.402ns logic, 3.119ns route)
                             (63.4% logic, 36.6% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'z_cmp_eq0000'
  Total number of paths / destination ports: 4 / 4
-------------------------------------------------------------------------
Offset:              4.368ns (Levels of Logic = 1)
  Source:            z_3 (LATCH)
  Destination:       z<3> (PAD)
  Source Clock:      z_cmp_eq0000 rising

  Data Path: z_3 to z<3>
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

---------- ----------

LD_1:G->Q 1 0.676 0.420 z_3 (z_3)

OBUF:I->O 3.272 z_3_OBUF (z<3>)

Total 4.368ns (3.948ns logic, 0.420ns route)

(90.4% logic, 9.6% route)

==========

Total REAL time to Xst completion: 3.00 secs

Total CPU time to Xst completion: 3.47 secs

-->

Total memory usage is 254100 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 1 (0 filtered)

Number of infos : 3 (0 filtered)