NAME : CHETAN NARENDRA THORAT   BATCH : B10

DIV :   BE (III)   ROLL NO : 052

Program:

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

use IEEE.STD_LOGIC_ARITH.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;


entity srr is

   Port ( Pi : in  STD_LOGIC_VECTOR (7 downto 0);

        Po : out  STD_LOGIC_VECTOR (7 downto 0);

        Si : in  STD_LOGIC;

        So : out  STD_LOGIC;

        rst : in  STD_LOGIC;

        clk : in  STD_LOGIC;

        mode : in  STD_LOGIC_VECTOR (1 downto 0));
```

```vhdl
end srr;


architecture Behavioral of srr is

signal temp: STD_LOGIC_VECTOR (7 downto 0);

signal count : integer range 0 to 7 ;

begin

process (clk,rst,Pi,Si,mode)

begin

if(rst='1') then

Po<="00000000";

So<='0';

else if (clk'event and clk='1') then

case mode is

when "00"=> temp <= Si & temp(7 downto 1);

So<=temp(0);

when "01"=> temp <= Si & temp(7 downto 1);

Po<=temp;

when "10"=>temp<=Pi;

Po<=temp;

when "11"=>

if count = 0 then

So<=temp(0);

count<= count+1;

elsif count<7 then

temp(6 downto 0)<=temp(7 downto 1);
```

So<=temp(0);

count<=count+1;

end if;

when others => null;

end case;

end if;

end if;

end process;

end Behavioral;

Test Bench Program:

```vhdl
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;

 -- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric_std.ALL;

 ENTITY srrrr IS

END srrrr;

 ARCHITECTURE behavior OF srrrr IS


   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT srr

  PORT(

     Pi : IN  std_logic_vector(7 downto 0);
```

```vhdl
        Po : OUT  std_logic_vector(7 downto 0);

        Si : IN  std_logic;

        So : OUT  std_logic;

        rst : IN  std_logic;

        clk : IN  std_logic;

        mode : IN  std_logic_vector(1 downto 0)

      );
 END COMPONENT;
--Inputs
signal Pi : std_logic_vector(7 downto 0) := (others => '0');

signal Si : std_logic := '0';

signal rst : std_logic := '0';

signal clk : std_logic := '0';

signal mode : std_logic_vector(1 downto 0) := (others => '0');


      --Outputs
signal Po : std_logic_vector(7 downto 0);

signal So : std_logic;


 -- Clock period definitions
constant clk_period : time := 10 ns;


BEGIN


        -- Instantiate the Unit Under Test (UUT)
```

```vhdl
uut: srr PORT MAP (

    Pi => Pi,

    Po => Po,

    Si => Si,

    So => So,

    rst => rst,

    clk => clk,

    mode => mode

    );
-- Clock process definitions
clk_process :process
begin

                clk <= '0';

                wait for clk_period/2;

                clk <= '1';

                wait for clk_period/2;

end process;
 -- Stimulus process
stim_proc: process
begin
rst<='0';
mode<="00";
Si<='1';
Pi<="10101010";
    -- hold reset state for 100 ns.
```

```vhdl
    wait for 100 ns;

                Si<='1';

Pi<="10101010";

mode<="01";

    -- hold reset state for 100 ns.

    wait for 100 ns;       Si<='1';

Pi<="10101010";

mode<="10";

    -- hold reset state for 100 ns.

    wait for 100 ns;

                Si<='1';

Pi<="10101010";

mode<="11";

    -- hold reset state for 100 ns.

    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here

    wait;

  end process;

END;
```

DESIGN SUMMARY:

Release 14.1 - xst P.15xf (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.10 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.10 secs

--> Reading design: srr.prj

TABLE OF CONTENTS

===

*   Synthesis Options Summary   *

===

---- Source Parameters

Input File Name   : "srr.prj"

Input Format   : mixed

Ignore Synthesis Constraint File   : NO

---- Target Parameters

Output File Name   : "srr"

Output Format   : NGC

Target Device   : xc3s500e-4-fg320

---- Source Options

Top Module Name   : srr

Automatic FSM Extraction   : YES

FSM Encoding Algorithm   : Auto

Safe Implementation   : No

FSM Style   : LUT

RAM Extraction   : Yes

RAM Style   : Auto

ROM Extraction   : Yes

Mux Style   : Auto

Decoder Extraction   : YES

Priority Encoder Extraction   : Yes

Shift Register Extraction   : YES

Logical Shifter Extraction   : YES

XOR Collapsing   : YES

ROM Style   : Auto

Mux Extraction   : Yes

Resource Sharing   : YES

Asynchronous To Synchronous   : NO

Multiplier Style   : Auto

Automatic Register Balancing   : No

---- Target Options

Add IO Buffers   : YES

Global Maximum Fanout   : 500

Add Generic Clock Buffer(BUFG)   : 24

Register Duplication   : YES

Slice Packing   : YES

Optimize Instantiated Primitives   : NO

Use Clock Enable   : Yes

Use Synchronous Set   : Yes

Use Synchronous Reset   : Yes

Pack IO Registers into IOBs   : Auto

Equivalent register Removal   : YES

---- General Options

Optimization Goal   : Speed

Optimization Effort   : 1

Keep Hierarchy   : No

Netlist Hierarchy   : As_Optimized

RTL Output   : Yes

Global Optimization   : AllClockNets

Read Cores   : YES

Write Timing Constraints   : NO

Cross Clock Analysis   : NO

Hierarchy Separator   : /

Bus Delimiter   : <>

Case Specifier   : Maintain

Slice Utilization Ratio   : 100

BRAM Utilization Ratio   : 100

Verilog 2001   : YES

Auto BRAM Packing   : NO

Slice Utilization Ratio Delta   : 5

===

===

*   HDL Compilation   *

===

Compiling vhdl file "C:/.Xilinx/Shift_Register/srr.vhd" in Library work.

Architecture behavioral of Entity srr is up to date.

===

*   Design Hierarchy Analysis   *

===

Analyzing hierarchy for entity <srr> in library <work> (architecture <behavioral>).

===

*   HDL Analysis   *

===

Analyzing Entity <srr> in library <work> (Architecture <behavioral>).

Entity <srr> analyzed. Unit <srr> generated.

===

*   HDL Synthesis   *

===

Performing bidirectional port resolution...

Synthesizing Unit <srr>.

  Related source file is "C:/.Xilinx/Shift_Register/srr.vhd".

  Found 8-bit register for signal <Po>.

  Found 1-bit register for signal <So>.

  Found 3-bit up counter for signal <count>.

  Found 3-bit comparator greatequal for signal <count$cmp_ge0000> created at line 64.

  Found 8-bit 4-to-1 multiplexer for signal <Po$mux0000> created at line 54.

  Found 1-bit 4-to-1 multiplexer for signal <So$mux0000> created at line 54.

  Found 8-bit register for signal <temp>.

  Found 3-bit comparator less for signal <temp_0$cmp_lt0000> created at line 64.

  Found 1-bit 4-to-1 multiplexer for signal <temp_0$mux0000> created at line 54.

  Found 1-bit 4-to-1 multiplexer for signal <temp_1$mux0000> created at line 54.

  Found 1-bit 4-to-1 multiplexer for signal <temp_2$mux0000> created at line 54.

  Found 1-bit 4-to-1 multiplexer for signal <temp_3$mux0000> created at line 54.

  Found 1-bit 4-to-1 multiplexer for signal <temp_4$mux0000> created at line 54.

  Found 1-bit 4-to-1 multiplexer for signal <temp_5$mux0000> created at line 54.

  Found 1-bit 4-to-1 multiplexer for signal <temp_6$mux0000> created at line 54.

  Found 1-bit 4-to-1 multiplexer for signal <temp_7$mux0000> created at line 54.

  Summary:

      inferred   1 Counter(s).

      inferred 17 D-type flip-flop(s).

      inferred   2 Comparator(s).

      inferred 17 Multiplexer(s).

Unit <srr> synthesized.

==

HDL Synthesis Report

Macro Statistics

Counters   : 1

 3-bit up counter   : 1

Registers   : 10

 1-bit register   : 9

 8-bit register   : 1

Comparators   : 2

 3-bit comparator greatequal   : 1

 3-bit comparator less   : 1

Multiplexers   : 10

 1-bit 4-to-1 multiplexer   : 9

 8-bit 4-to-1 multiplexer   : 1

==

==
*   Advanced HDL Synthesis   *
==

==

Advanced HDL Synthesis Report

Macro Statistics

Counters   : 1

 3-bit up counter   : 1

Registers   : 17

 Flip-Flops   : 17

Comparators   : 2

 3-bit comparator greatequal   : 1

 3-bit comparator less   : 1

Multiplexers   : 10

 1-bit 4-to-1 multiplexer   : 9

 8-bit 4-to-1 multiplexer   : 1

===

===

*   Low Level Synthesis   *

===

Optimizing unit <srr> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block srr, actual ratio is 0.

Final Macro Processing ...

===

Final Register Report

Macro Statistics

Registers   : 20

 Flip-Flops   : 20

===

===
*   Partition Report   *
===

Partition Implementation Status

  No Partitions were found in this design.

===
*   Final Report   *

==

Final Results

RTL Top Level Output File Name   : srr.ngr

Top Level Output File Name   : srr

Output Format   : NGC

Optimization Goal   : Speed

Keep Hierarchy   : No

Design Statistics

IOs   : 22

Cell Usage :

BELS   : 41

INV   : 2

LUT2   : 1

LUT2_L   : 1

LUT3   : 10

LUT4   : 19

MUXF5   : 8

FlipFlops/Latches   : 20

FDC   : 8

FDCE   : 1

FDE   : 11

Clock Buffers   : 1

BUFGP   : 1

IO Buffers   : 21

IBUF   : 12

OBUF   : 9

===

Device utilization summary:

Selected Device : 3s500efg320-4

Number of Slices: 16 out of   4656   0%

Number of Slice Flip Flops: 20 out of   9312   0%

Number of 4 input LUTs: 33 out of   9312   0%

Number of IOs: 22

Number of bonded IOBs: 22 out of   232   9%

Number of GCLKs: 1 out of   24   4%

Partition Resource Summary:

 No Partitions were found in this design.

```
================================================================

TIMING REPORT


NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

    FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

    GENERATED AFTER PLACE-and-ROUTE.


Clock Information:

------------------

--------------------------------+----------------------+-------+

Clock Signal                | Clock buffer(FF name)  | Load  |

--------------------------------+----------------------+-------+

clk                | BUFGP              | 20    |

--------------------------------+----------------------+-------+


Asynchronous Control Signals Information:

----------------------------------------

--------------------------------+----------------------+-------+

Control Signal              | Buffer(FF name)      | Load  |

--------------------------------+----------------------+-------+

rst                | IBUF              | 9     |

--------------------------------+----------------------+-------+


Timing Summary:
```

Speed Grade: -4

   Minimum period: 4.102ns (Maximum Frequency: 243.784MHz)

   Minimum input arrival time before clock: 5.646ns

   Maximum output required time after clock: 4.310ns

   Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

==

Timing constraint: Default period analysis for Clock 'clk'

  Clock period: 4.102ns (frequency: 243.784MHz)

  Total number of paths / destination ports: 78 / 24

Delay: 4.102ns (Levels of Logic = 3)

  Source: count_2 (FF)

  Destination: temp_6 (FF)

  Source Clock: clk rising

  Destination Clock: clk rising

  Data Path: count_2 to temp_6

                 Gate   Net

  Cell:in->out   fanout Delay Delay Logical Name (Net Name)

   ------------------------------------- -----------

FDE:C->Q   4 0.591 0.762 count_2 (count_2)

LUT3:I0->O   7 0.704 0.712 Mmux_temp_0_mux0000211 (N01)

LUT4:I3->O   1 0.704 0.000 Mmux_temp_6_mux00002_G (N42)

MUXF5:I1->O   1 0.321 0.000 Mmux_temp_6_mux00002 (temp_6_mux0000)

FDE:D   0.308   temp_6

Total   4.102ns (2.628ns logic, 1.474ns route)

                  (64.1% logic, 35.9% route)

==

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

 Total number of paths / destination ports: 71 / 28

Offset: 5.646ns (Levels of Logic = 3)

 Source: mode<1> (PAD)

 Destination: count_0 (FF)

 Destination Clock: clk rising

 Data Path: mode<1> to count_0

                 Gate   Net

  Cell:in->out   fanout Delay Delay Logical Name (Net Name)

  --------------------------------------- ------------

  IBUF:I->O   26 1.218 1.435 mode_1_IBUF (mode_1_IBUF)

  LUT3:I0->O   1 0.704 0.499 Mmux_So_mux0000311_SW0 (N37)

  LUT4:I1->O   3 0.704 0.531 count_and00001 (count_and0000)

```
   FDE:CE              0.555        count_0

   ---------------------------------------

   Total                 5.646ns (3.181ns logic, 2.465ns route)

                         (56.3% logic, 43.7% route)



==============================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

  Total number of paths / destination ports: 9 / 9

-----------------------------------------------------------------------

Offset:          4.310ns (Levels of Logic = 1)

  Source:        Po_7 (FF)

  Destination:     Po<7> (PAD)

  Source Clock:    clk rising


  Data Path: Po_7 to Po<7>

                    Gate     Net

   Cell:in->out     fanout  Delay  Delay  Logical Name (Net Name)

   ---------------------------------------  ------------

   FDC:C->Q         2   0.591   0.447  Po_7 (Po_7)

   OBUF:I->O            3.272      Po_7_OBUF (Po<7>)

   ---------------------------------------

   Total                 4.310ns (3.863ns logic, 0.447ns route)

                         (89.6% logic, 10.4% route)



==============================================================================
```

Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 3.55 secs

-->

Total memory usage is 254764 kilobytes

Number of errors   :   0 (0 filtered)

Number of warnings :   0 (0 filtered)

Number of infos   :   0 (0 filtered)