

Introduction to process Architecture

SEQ & PIPE– Architecture

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Sequential Architecture:

- We need to design a Y86-64 Processor using verilog by implementing the sequential design.
- Our Y86-64 processor is capable of running following instructions :
halt, nop, rrmovq, vmovle, cmovl, cmovle, cmovge, cmovg, irmovq, rmmovq, mrmovq, addq, subq, andq, xorq, jmp, jle, jl, je, jne, jge, jg, call, ret, pushq, popq.
- Now let's discuss the various stages involved in our SEQ design.

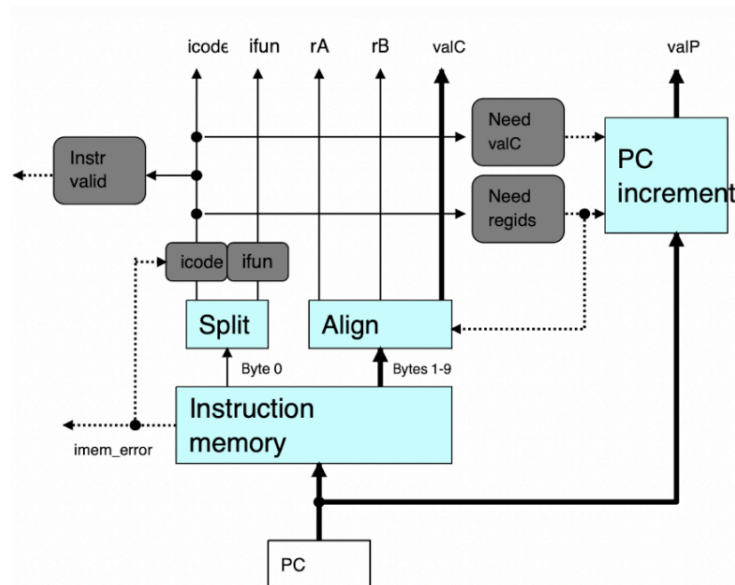
Fetch Stage :

- The main purpose of the fetch stage is to fetch data from the instruction memory based on the Program Counter (PC) value and updating the PC to the next instruction's address.
- In the fetch stage, we typically take inputs on the negative edge of the clock, and after processing within the module, the outputs are ready on the positive edge of the clock. This process ensures proper synchronization and smooth operation.
- To do this, we split the instruction memory at the byte where the PC points, dividing it into two parts: the most significant 4 bits (MSB) and the least significant 4 bits (LSB). The MSB represents the icode, while the LSB represents the instruction function (Ifun).

1st Byte	i_code (MSB 4bits)	i_fun (LSB 4bits)
2nd Byte	r_A (MSB 4bits)	r_B (LSB 4bits)
3rd Byte	Val C	
4th Byte	Val C	
5th Byte	Val C	
6th Byte	Val C	
7th Byte	Val C	
8th Byte	Val C	
9th Byte	Val C	
10th Byte	Val C	

Our instruction set implementaion diagram. In our implementation we are using PC+8 bits instead of PC+1 Byte. So in report for simplicity we are using PC+1 or PC+x bytes everywhere instead of PC+8 bits.

- The fetch stage reads the bytes of an instruction from memory, using the program counter (PC) as the memory address. From the instruction it extracts the two 4-bit portions of the instruction specifier byte, referred to as `icode` (the instruction code) and `ifun` (the instruction function). It possibly fetches a register specifier byte, giving one or both of the register operand specifiers `rA` and `rB`. It also possibly fetches a 4-byte constant word `valC`. It computes `valP` to be the address of the instruction following the current one in sequential order. That is, `valP` equals the value of the PC plus the length of the fetched instruction.
- The inputs to the fetch module include the instruction memory itself and the PC value. From these inputs, we derive various outputs such as register encodings (`rA` and `rB`), `icode`, `Ifun`, the value to be stored in the Constant (`valC`), the next PC value (`valP`), instruction validity (`instr_valid`), and any errors that may occur during instruction memory access (`imem_error`).



block digram showing fetch operations

Brief expalanation of each instruction:

Halt :

- To implement this, the fetch stage checks the instruction memory at the PC address. If the icode is 0000(Ifun is anything), it sets the halt flag to 1 and increments the next PC value (valP) to PC+8 (In our case as we have taken it in bits so we do PC+8 bits). This stops the iterations as no changes occur in the execute, decode, or memory blocks due to the halt flag being set.

```
1      /// HALT
2      if(Ins_Code == 0 && Ins_fun == 0)begin
3          // Do not do anything
4          // to write something such that the code
           stops executing
5      end
```

Nop :

- After checking the PC value to locate the instruction, if the icode is 0001, fetch stage encounters a "nop" (no operation) instruction, with any Ifun value. Then we increment the PC value (valP) to PC+1(In our implementation PC+8 bits). No other operations occur, and the processor moves directly to the next iteration since the PC is updated after each instruction execution.

```
1      /// No operation nop
2      if(Ins_Code == 1 && Ins_fun == 0)begin
3          // skip this instruction
4          need_regids = 0;
5          need_Val_C = 0;
6          //PC_increment_bytes = 8 + need_regids * 8
           + need_Val_C * 64;
7          Val_P =
           memory_for_instructions[$unsigned(PC_adress)
           + 8 + need_regids * 8 + need_Val_C *
           64][63 : 0];
8      end
```

CMOVXX :

- For the cmovxx instruction, the fetch stage begins by looking at the instruction code (icode), which is 00010, and the function code (ifun), represented as xxxx(ranging from 0 to 6). Since the icode is 0010, the fetch stage knows it needs to fetch data from the instruction memory at addresses PC and PC+1(PC+8 bits in our implementation) to get both the icode, ifun and r_A , r_B encodings.
- After retrieving this data, it increments the Program Counter (PC) to PC+2 since it has processed instructions from addresses PC and PC+1.

```
1      /// conditional move cmovXX
2      if(Ins_Code == 2)begin
3          if(0 <= Ins_fun <= 6)begin
4              rA = instruction_set
5                  [($unsigned(PC_address)/8) + 1][7 :
6                  4];
7              rB = instruction_set
8                  [($unsigned(PC_address)/8) + 1][3 :
9                  0];
10             need_Val_C = 0;
11             // since Val_C not present and needed,
12             // we do not fetch val_C.
13             need_regids = 1;
14             // since regids needed, we fetched
15             // registers ra and rb
16             //PC_increment_bytes = 8 + need_regids
17                 * 8 + need_Val_C * 64;
18             Val_P =
19                 memory_for_instructions[$unsigned(PC_address)
20                     + 8 + need_regids * 8 + need_Val_C *
21                     64][63:0];
22         end
23     end
24     if(Ins_fun >6)begin
25         $display("For cmovXX the function code
26             range between 0 to 6");
27     end
28 end
```

IRMOVQ :

- As the name implies, the fetch stage immediately moves data from the constant value (valC) to the specified register (rA or rB).
- In decoding the instruction memory from PC to PC+9, the PC provides the instruction code (ICode), which is 0011, along with the function code (IFun). The next memory location, PC+1, provides values for rA and rB. Finally, the memory locations from PC+2 to PC+9 provide the constant value (valC).
- Since it fetches all 10 PC instructions, it increments the PC by 10 (PC+10) after processing.
- So, in brief: PC provides ICode and IFun, PC+1 provides rA and rB, and PC+2 to PC+9 provide valC. After processing, the next PC value (valP) is set to PC+10.

```
1  /// immediate Register move irmovq
2      if(Ins_Code == 3)begin
3          if(Ins_fun != 0)begin
4              $display("ERROR:  for  irmovq:  function
5                  code  is  0,  but  not  entered  0");
6          end
7          if(Ins_fun == 0)begin
8              // immediate register move.
9              need_Val_C = 1;
10             need_regids = 1;
11 rA = instruction_set [($unsigned(PC_adress)/8)+1][7:4];
12 rB = instruction_set [($unsigned(PC_adress)/8)+1][3:0];
13 Val_C = {instruction_set [($unsigned(PC_adress)/8)+2],
14 instruction_set [($unsigned(PC_adress)/8)+3],
15 instruction_set [($unsigned(PC_adress)/8)+4],
16 instruction_set [($unsigned(PC_adress)/8)+5],
17 instruction_set [($unsigned(PC_adress)/8)+6],
18 instruction_set [($unsigned(PC_adress)/8)+7],
19 instruction_set [($unsigned(PC_adress)/8)+8],
20 instruction_set [($unsigned(PC_adress)/8)+9]};
21 Val_P = memory_for_instructions [$unsigned(PC_adress) +
22     8 + need_regids * 8 + need_Val_C * 64][63 : 0];
23
24     end
25 end
```

RMMOVQ :

- As the name implies, this stage moves data from registers to memory, based on the values of rA and rB.
- In decoding the instruction memory from PC to PC+9, the PC provides the instruction code (ICode), which is 0100, along with the function code (IFun). The next memory location, PC+1, provides values for rA and rB. The subsequent memory locations from PC+2 to PC+9 provide the constant value (valC).
- Since it processes all 10 PC instructions, it increments the PC by 10 (PC+10) after completion. So, in brief: PC provides ICode and IFun, PC+1 provides rA and rB, and PC+2 to PC+9 provide valC. After processing, the next PC value (valP) is set to PC+10.

```
1 if(Ins_Code == 4)begin
2 if(Ins_fun != 0)begin
3 $display("ERROR: for rmmovq: function code is 0, but
   not entered 0");
4     end
5 if(Ins_fun == 0)begin
6 need_Val_C = 1;
7 need_regids = 1;
8 rA = instruction_set[($unsigned(PC_adress)/8) + 1][7:4];
9 rB = instruction_set[($unsigned(PC_adress)/8) + 1][3:0];
10 Val_C = same as of previous operation updation
11 Val_P = memory_for_instructions [$unsigned(PC_adress) +
   8 + need_regids * 8 + need_Val_C * 64][63 : 0];
12     end
13 end
```

MRMOVQ :

- As the name implies, this stage moves data from memory to registers, based on the values of rA and rB.
- When decoding the instruction memory from PC to PC+9, the PC provides the instruction code (ICode), which is 0100, along with the function code (IFun). At PC+1, the values for rA and rB are found, while the values from memory locations PC+2 to PC+9 provide the constant value (valC).

- After processing all 10 PC instructions, the PC is incremented by 10 (PC+10). So, to brief: PC provides ICode and IFun, PC+1 provides rA and rB, and PC+2 to PC+9 provide valC. After processing, the next PC value (valP) is set to PC+10.

```

1  /// memory to register move mrmovq
2  if(Ins_Code == 5)begin
3  if(Ins_fun == 0)begin
4  need_Val_C = 1;
5  need_regids = 1;
6  rA = instruction_set[($unsigned(PC_adress)/8) + 1][7:4];
7  rB = instruction_set[($unsigned(PC_adress)/8) + 1][3:0];
8  Val_C = same as of previous operation updation
9  Val_P = memory_for_instructions [$unsigned(PC_adress) +
    8 + need_regids * 8 + need_Val_C * 64][63 : 0];
10      end
11  end

```

FETCH FOR OPQ :

- As the name suggests, this instruction performs addition, subtraction, and logical operations (AND, XOR) on the register addresses rA and rB, depending on the function code (ifun).
- For the OPQ instruction, the instruction code (Icode) must be 0110, and the function code (ifun) determines the specific operation to execute.
- To fetch the instruction, it reads the memory locations from PC to PC+1, extracting the Icode and ifun from PC, and rA and rB from PC+1. Then, it increments the PC value by 2, setting valP to PC+2.

```

1  /// Arithmetic memory operations: OPq
2  if(Ins_Code == 6)begin
3      if(Ins_fun >3)begin
4          $display("For OPq the i_fun code range is 0 to 3");
5      end
6  if(Ins_fun >=0 && Ins_fun <=3)begin
7  need_Val_C = 0;
8  need_regids = 1;
9  rA = instruction_set[($unsigned(PC_adress)/8) + 1][7:4];
10 rB = instruction_set[($unsigned(PC_adress)/8) + 1][3:0];

```



```

11 Val_P = memory_for_instructions [$unsigned(PC_address) +
    8 + need_regids * 8 + need_Val_C * 64][63 : 0];
12 end
13 end

```

FETCH FOR JXX :

- This instruction, as the name implies, facilitates jumping from one instruction to another based on certain conditions.
- For the JXX instruction, the instruction code (Icode) must be 0111, while the function code (Ifun) doesn't affect the execution or PC update.
- To fetch this instruction, it reads memory locations from PC to PC+8. It extracts Icode and Ifun from PC, and valC from PC+1 to PC+8. Then, it increments the PC value by 9, setting valP to PC+9.
- So, in short: the instruction code must be 0111, Ifun doesn't matter, PC provides Icode, and valC comes from PC+1 to PC+8. After processing, the next PC value (valP) is set to PC+9.

```

1      /// JUMP operations
2  if(Ins_Code == 7)begin
3      if(Ins_fun > 6)begin
4          $display("Error: for JUMP operations, the function
5              codes between 0 and 6");
6      end
7  if(Ins_fun >= 0 && Ins_fun <= 6)begin
8      need_regids = 0;
9      need_Val_C = 1;
10     Val_C = {instruction_set [($unsigned(PC_address)/8) + 1],
11         instruction_set [($unsigned(PC_address)/8) + 2],
12         instruction_set [($unsigned(PC_address)/8) + 3],
13         instruction_set [($unsigned(PC_address)/8) + 4],
14         instruction_set [($unsigned(PC_address)/8) + 5],
15         instruction_set [($unsigned(PC_address)/8) + 6],
16         instruction_set [($unsigned(PC_address)/8) + 7],
17         instruction_set [($unsigned(PC_address)/8) + 8]};
18     Val_P = memory_for_instructions [$unsigned(PC_address) +
19         8 + need_regids * 8 + need_Val_C * 64][63 : 0];
20 end
21 end

```

FETCH FOR CALL :

- This instruction, as indicated by its name, retrieves a value from the register pointed to by the stack within the storage of the Y86-64 architecture.
- For the Call instruction, the instruction code (icode) should be 1000, while the function code (ifun) can be any value (xxxx).
- During the fetch stage, instructions are fetched from the instruction memory ranging from PC to PC+8. PC provides the Icode and Ifun, and from PC to PC+8 provides the valC. Therefore, the PC needs to be incremented by 9, resulting in valP=PC+9.

```
1      /// CALL operations : call
2  if(Ins_Code == 8)begin
3      if(Ins_fun != 0)begin
4  $display("ERROR: for call the function code is 0");
5      end
6  if(Ins_fun == 0)begin
7      need_regids = 0;
8      need_Val_C = 1;
9      Val_C = {instruction_set [($unsigned(PC_address)/8) + 1],
10 instruction_set [($unsigned(PC_address)/8) + 2],
11 instruction_set [($unsigned(PC_address)/8) + 3],
12 instruction_set [($unsigned(PC_address)/8) + 4],
13 instruction_set [($unsigned(PC_address)/8) + 5],
14 instruction_set [($unsigned(PC_address)/8) + 6],
15 instruction_set [($unsigned(PC_address)/8) + 7],
16 instruction_set [($unsigned(PC_address)/8) + 8]};
17 Val_P = memory_for_instructions [$unsigned(PC_address) +
    8 + need_regids * 8 + need_Val_C * 64][63 : 0];
18 end
19 end
```

FETCH FOR RETURN :

- This instruction, as its name implies, returns the value pointed to by the stack. For the Return instruction, the instruction code (Icode) is 1001, and the function code (Ifun) is considered.
- During the fetch stage, only one instruction is fetched from PC, providing the Icode and Ifun. Therefore, the PC is incremented only once, resulting in valP=PC+1.

```

1      /// Return operation : ret
2      if(Ins_Code == 9)begin
3          if(Ins_fun != 0)begin
4              $display("Function code for return is
5                  0");
6          end
7
8          if(Ins_fun == 0)begin
9              //no need to fetch anything, we just
10             need to update pc to the next
11             instruction after the call
12
13             need_regids = 0;
14             need_Val_C = 0;
15         end
16     end
17 end

```

Pushq :

- This instruction, pushes data to a lower memory location, typically decremented by 8. Therefore, it's usually stored at the initial memory minus 8. For Push instruction, the instruction code (Icode) is 1010, and the function code (Ifun) is considered.
- During the fetch stage, it retrieves instructions from the instruction memory at PC and PC+1. PC provides the Icode (1010) and Ifun, while PC+1 provides the values for rA and rB. After this, the PC is incremented by 2, resulting in valP=PC+2.

```

1      /// Pushq
2      if(Ins_Code == 10)begin
3          if(Ins_fun != 0)begin
4              $display("Function code for pushq is 0");
5          end
6      if(Ins_fun == 0)begin
7          need_regids = 1;
8          need_Val_C = 0;
9          rA = instruction_set[($unsigned(PC_address)/8) + 1][7:4];
10         rB = instruction_set[($unsigned(PC_address)/8) + 1][3:0];
11         Val_P = memory_for_instructions [$unsigned(PC_address) +
12             8 + need_regids * 8 + need_Val_C * 64][63 : 0];
13     end
14 end

```

Popq :

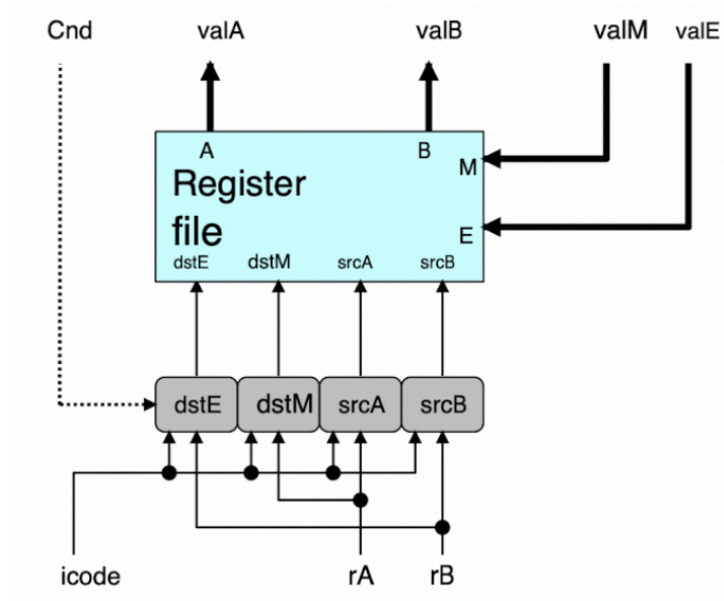
- This instruction, pops data from a higher memory location, typically incremented by 8. Therefore, it's usually stored at the initial memory plus 8. For the Pop instruction, the instruction code (Icode) is 1011, and the function code (Ifun) is considered.
- During the fetch stage, it retrieves instructions from the instruction memory at PC and PC+1. PC provides the Icode (1011) and Ifun, while PC+1 provides the values for rA and rB. After this, the PC is incremented by 2, resulting in valP=PC+2.

```
1  /// Popq
2  if(Ins_Code == 11)begin
3      if(Ins_fun != 0)begin
4          $display("Function code for popq is 0");
5      end
6  if(Ins_fun == 0)begin
7      need_Val_C = 0;
8      need_regids = 1;
9      rA = instruction_set[($unsigned(PC_adress)/8) + 1][7:4];
10     rB = instruction_set[($unsigned(PC_adress)/8) + 1][3:0];
11     Val_P = memory_for_instructions [$unsigned(PC_adress) +
        8 + need_regids * 8 + need_Val_C * 64][63 : 0];
12     end
13 end
```

.....

Decode and Write Back Stage :

- This block provides either the values of valA and valB, or just valA or just valB, depending on the case being used.



block digram showing decode operations

Brief expalanation of each instruction :

CMOV_{xx}:

Decode: Only the value of A is needed, which will be fetched from the register memory rA.

Writeback: If the condition is true (1), the value of register memory rB is stored as valE.

IRMOVQ:

Decode: No decoding is required for IRMOVQ.

Writeback: The value of valE is assigned to the register memory rB.

MRMOVQ:

Decode: The value of valB is fetched from the register memory rB.

Writeback: The value of valM is stored in the register memory rB.

OPQ instruction:

Decode: Fetch valA and valB from the register memory rA and rB respectively.

Writeback: Store the value of valE in the register memory of rB.

CALL instruction:

Decode: Fetch valB from the stack pointer rsp.

Writeback: Update the stack pointer rsp with the value of valE.

RETURN :

Decode: Retrieve valA and valB from the register memory of rsp.

Writeback: Update the stack pointer rsp with the executed value valE.

PUSHQ:

Decode: Obtain valA from register memory rA and valB from rsp.

Writeback: Update the stack pointer register rsp with the value of valE.

POPQ :

Decode: Fetch valA and valB from the register memory of rsp.

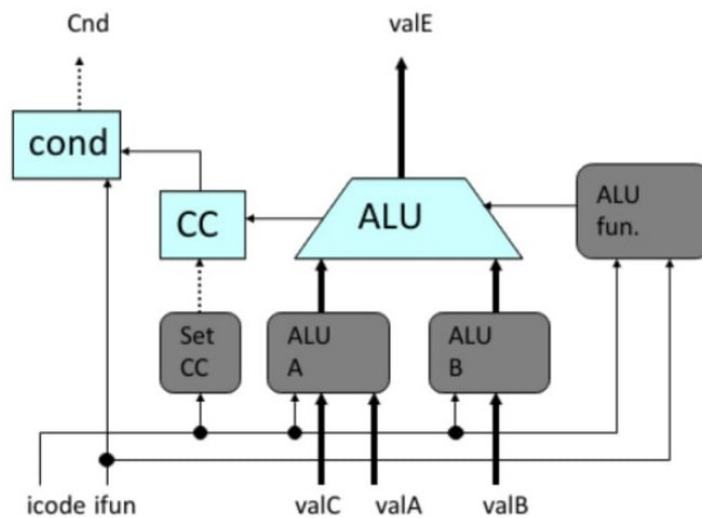
Writeback: Update the rsp with valE and R[rA] with valM.

- Other instructions won't require any additional decoding or writeback steps.
- Code for decode and write back stage is already uploaded.

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Execute Stage :

- During the execute stage, the main focus is on the operations of the Arithmetic Logic Unit (ALU). It performs operations based on the values of valA and valB obtained during the decode stage. The outputs typically include Zf (zero flag), Sf (sign flag), Of (overflow flag), and valE (result of the operation). These outputs are crucial for determining the status and outcome of the operation being executed.
- The Inputs to this module are clk, icode, ifun, valA, valB, valC and outputs are cnd signal, valE, cc.



block digram showing execute stage

Brief expalanation of each instruction :

- For the HALT instruction, no execution occurs.
- Similarly, for the NOP (No Operation) instruction, there are no executions as implied by the name.

CMOV :

- For the CMOVxx instruction, execution primarily involves evaluating the condition control using the provided flags (such as Sf, Zf, and Of) based on the Ifun parameter. This determines whether the operation specified by the instruction should be performed.

Instruction	Synonym	Move condition	Description
<code>cmove S, R</code>	<code>cmovz</code>	ZF	Equal / zero
<code>cmovne S, R</code>	<code>cmovnz</code>	\sim ZF	Not equal / not zero
<code>cmovs S, R</code>		SF	Negative
<code>cmovns S, R</code>		\sim SF	Nonnegative
<code>cmovg S, R</code>	<code>cmovnle</code>	\sim (SF \wedge OF) & \sim ZF	Greater (signed >)
<code>cmovge S, R</code>	<code>cmovnl</code>	\sim (SF \wedge OF)	Greater or equal (signed >=)
<code>cmovl S, R</code>	<code>cmovnge</code>	SF \wedge OF	Less (signed <)
<code>cmovle S, R</code>	<code>cmovng</code>	(SF \wedge OF) ZF	Less or equal (signed <=)
<code>cmova S, R</code>	<code>cmovnbe</code>	\sim CF & \sim ZF	Above (unsigned >)
<code>cmovae S, R</code>	<code>cmovnb</code>	\sim CF	Above or equal (Unsigned >=)
<code>cmovb S, R</code>	<code>cmovnae</code>	CF	Below (unsigned <)
<code>cmovbe S, R</code>	<code>cmovna</code>	CF ZF	below or equal (unsigned <=)

Based on the condition provided, `cnd` is set to 1 if the move condition specified in the above instruction is satisfied.

IRMOVQ :

- For the IRMOVQ instruction, the execution involves a single operation: setting `valE` to the immediate value `valC` \implies `valE` = `valC`

RMMOVQ AND MRMOVQ :

- For both RMMOVQ and MRMOVQ instructions, the execution is similar since they involve moving data between registers and memory. In both cases, the execution calculates the memory address as `valE` = `valC` + `valB`.

EXECUTE FOR OPQ :

- For the OPQ instruction, various operations are performed on `valA` and `valB` based on the value of `ifun`. For example, if `ifun` is 0000, addition is performed; if `ifun` represents subtraction, multiplication, or any other operation, the corresponding operation is executed accordingly.

EXECUTE FOR JXX :

- In this stage, the execution primarily involves carrying out conditional jumps based on the flags provided, such as `Sf`, `Zf`, and `Of`, depending on the value of `ifun`.

Instruction	Synonym	Jump condition	Description
jmp <i>Label</i>		1	Direct jump
jmp <i>*Operand</i>		1	Indirect jump
j _e <i>Label</i>	j _z	ZF	Equal / zero
j _{ne} <i>Label</i>	j _{nz}	~ZF	Not equal / not zero
j _s <i>Label</i>		SF	Negative
j _{ns} <i>Label</i>		~SF	Nonnegative
j _g <i>Label</i>	j _{nle}	~(SF ^ OF) & ~ZF	Greater (signed >)
j _{ge} <i>Label</i>	j _{nl}	~(SF ^ OF)	Greater or equal (signed >=)
j _l <i>Label</i>	j _{nge}	SF ^ OF	Less (signed <)
j _{le} <i>Label</i>	j _{ng}	(SF ^ OF) ZF	Less or equal (signed <=)
j _a <i>Label</i>	j _{nbe}	~CF & ~ZF	Above (unsigned >)
j _{ae} <i>Label</i>	j _{nb}	~CF	Above or equal (unsigned >=)
j _b <i>Label</i>	j _{nae}	CF	Below (unsigned <)
j _{be} <i>Label</i>	j _{na}	CF ZF	Below or equal (unsigned <=)

CALL :

- Execution involves simply decreasing valC by 8 and assigning it to valE.

RETURN :

- Execution involves simply increasing valC by 8 and assigning it to valE.

PUSH :

- Execution requires decrementing valB by 8, as valE is determined by subtracting 8 from valB (valE = -64'd8 +valB).

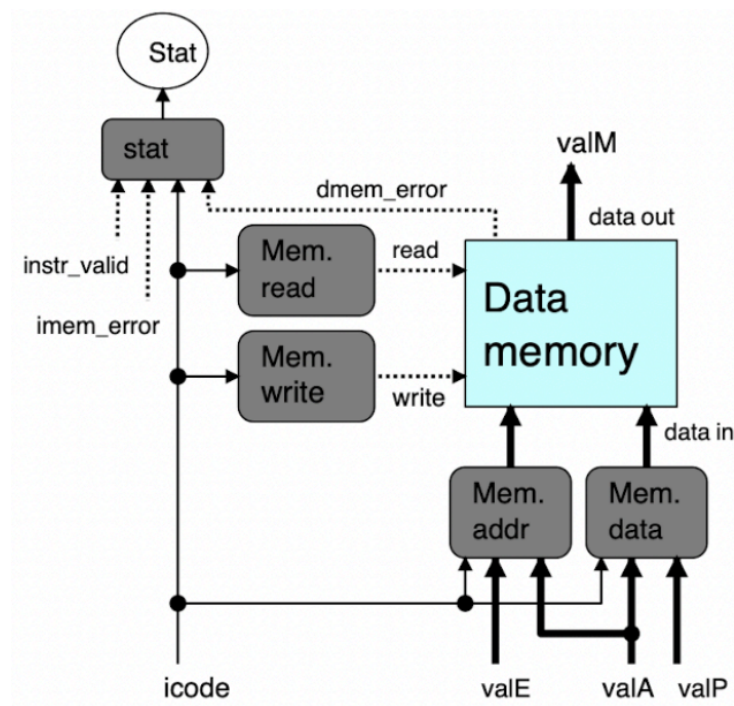
POP :

- Here execution involves incrementing valB by 8, as valE is determined by adding 8 to valB. (valE = 64'd8 +valB).

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Memory Block :

- The memory module is responsible for storing bits of memory data and can be accessed or utilized whenever necessary. It requires an address to fetch or store data in memory. This module is primarily utilized in instructions such as rmmovq, mrmovq, pop, push, and others, where data needs to be transferred to or from memory.
- We determine the memory address using valE, and based on the instruction, we either write data to or read data from memory. The data memory primarily stores the processor's data.



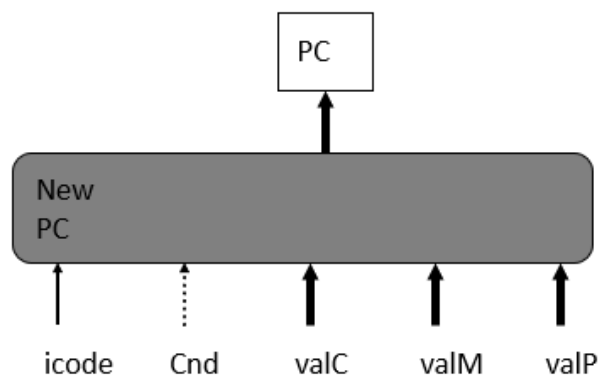
- In this module, the inputs are clk, icode, valA, valE, and valP. The outputs are valM and data_memory_error
- The primary operations performed in this stage are reading from memory or writing to memory, depending on the type of instruction being executed also checking instruction status, Select address, Select data.
- We've implemented a memory module, which is essentially an array of 64-bit registers used for storing, reading, and writing data. If an invalid memory address is provided as input, it will result in the generation of a data_memory_error

- **rmmovq** : $M8[valE] \leftarrow valA$ (Writing value to memory)
- **popq** : $valM \leftarrow M8[valA]$ (Read from old stack pointer)
- **Conditional moves**: Do nothing.
- **Jumps** : Do nothing.
- **Call** : $M8[valE] \leftarrow valP$ (Write incremented PC to new value of stack pointer or Writing return value on stack.)
- **ret** : $valM \leftarrow M8[valA]$ (Read return address from old stack pointer)

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PC Update Block :

- In this module, the primary task is to update the Program Counter (PC) with the respective valP under normal conditions. However, for instructions like CMOVxx, Jxx, and some others, the PC update might involve using valM or valC instead of the typical valP.
- The inputs to this module are clk, icode, cnd, valC, valM, and valP. The module outputs a signal called new_PC_address, indicating the updated PC value. Firstly we are doing a `mem_invalid_check == 0` and then `instruction_invalid_check == 0` then updating PC.



	OPq rA, rB	
PC update	PC \leftarrow valP	Update PC
	rmmovq rA, D(rB)	
PC update	PC \leftarrow valP	Update PC
	popq rA	
PC update	PC \leftarrow valP	Update PC
	jXX Dest	
PC update	PC \leftarrow Cnd ? valC : valP	Update PC
	call Dest	
PC update	PC \leftarrow valC	Set PC to destination
	ret	
PC update	PC \leftarrow valM	Set PC to return address

PC updation in different operations

Now explaining each stage of SEQ briefly in pictorial form as mentioned in class :

	OPq rA, rB	
Fetch	icode:ifun \leftarrow M ₁ [PC]	Read instruction byte
	rA:rB \leftarrow M ₁ [PC+1]	Read register byte
	valP \leftarrow PC+2	Compute next PC
Decode	valA \leftarrow R[rA]	Read operand A
	valB \leftarrow R[rB]	Read operand B
Execute	valE \leftarrow valB OP valA	Perform ALU operation
	Set CC	Set condition code register
Memory		
Write back	R[rB] \leftarrow valE	Write back result
PC update	PC \leftarrow valP	Update PC

OPQ Operation

	rmmovq rA, D(rB)	
Fetch	icode:ifun \leftarrow M ₁ [PC]	Read instruction byte
	rA:rB \leftarrow M ₁ [PC+1]	Read register byte
	valC \leftarrow M ₈ [PC+2]	Read displacement D
	valP \leftarrow PC+10	Compute next PC
Decode	valA \leftarrow R[rA]	Read operand A
	valB \leftarrow R[rB]	Read operand B
Execute	valE \leftarrow valB + valC	Compute effective address
Memory	M ₈ [valE] \leftarrow valA	Write value to memory
Write back		
PC update	PC \leftarrow valP	Update PC

rmmovq Operation

popq rA		
Fetch	$\text{icode:ifun} \leftarrow M_1[\text{PC}]$ $\text{rA:rB} \leftarrow M_1[\text{PC}+1]$ $\text{valP} \leftarrow \text{PC}+2$	Read instruction byte Read register byte Compute next PC
Decode	$\text{valA} \leftarrow R[\%rsp]$ $\text{valB} \leftarrow R[\%rsp]$	Read stack pointer Read stack pointer
Execute	$\text{valE} \leftarrow \text{valB} + 8$	Increment stack pointer
Memory	$\text{valM} \leftarrow M_8[\text{valA}]$	Read from stack
Write back	$R[\%rsp] \leftarrow \text{valE}$ $R[\text{rA}] \leftarrow \text{valM}$	Update stack pointer Write back result
PC update	$\text{PC} \leftarrow \text{valP}$	Update PC

- Use ALU to increment stack pointer
- Must update two registers
 - Popped value
 - New stack pointer

popq Operation

cmovXX rA, rB		
Fetch	$\text{icode:ifun} \leftarrow M_1[\text{PC}]$ $\text{rA:rB} \leftarrow M_1[\text{PC}+1]$ $\text{valP} \leftarrow \text{PC}+2$	Read instruction byte Read register byte Compute next PC
Decode	$\text{valA} \leftarrow R[\text{rA}]$ $\text{valB} \leftarrow 0$	Read operand A
Execute	$\text{valE} \leftarrow \text{valB} + \text{valA}$ If ! Cond(CC,ifun) $\text{rB} \leftarrow 0xF$	Pass valA through ALU (Disable register update)
Memory		
Write back	$R[\text{rB}] \leftarrow \text{valE}$	Write back result
PC update	$\text{PC} \leftarrow \text{valP}$	Update PC

- Read register rA and pass through ALU
- Cancel move by setting destination register to 0xF
 - If condition codes & move condition indicate no move

cmovxx Operation

	jXX Dest	
Fetch	$\text{icode:ifun} \leftarrow M_1[\text{PC}]$	Read instruction byte
	$\text{valC} \leftarrow M_8[\text{PC}+1]$	Read destination address
	$\text{valP} \leftarrow \text{PC}+9$	Fall through address
Decode		
Execute	$\text{Cnd} \leftarrow \text{Cond}(\text{CC}, \text{ifun})$	Take branch?
Memory		
Write back		
PC update	$\text{PC} \leftarrow \text{Cnd} ? \text{valC} : \text{valP}$	Update PC

- Compute both addresses
- Choose based on setting of condition codes and branch condition

jump Operation

	call Dest	
Fetch	$\text{icode:ifun} \leftarrow M_1[\text{PC}]$	Read instruction byte
	$\text{valC} \leftarrow M_8[\text{PC}+1]$	Read destination address
	$\text{valP} \leftarrow \text{PC}+9$	Compute return point
Decode	$\text{valB} \leftarrow R[\%rsp]$	Read stack pointer
Execute	$\text{valE} \leftarrow \text{valB} + -8$	Decrement stack pointer
Memory	$M_8[\text{valE}] \leftarrow \text{valP}$	Write return value on stack
Write back	$R[\%rsp] \leftarrow \text{valE}$	Update stack pointer
PC update	$\text{PC} \leftarrow \text{valC}$	Set PC to destination

- Use ALU to decrement stack pointer
- Store incremented PC

CALL Operation

	ret	
Fetch	$\text{icode:ifun} \leftarrow M_1[\text{PC}]$	Read instruction byte
Decode	$\text{valA} \leftarrow R[\%rsp]$ $\text{valB} \leftarrow R[\%rsp]$	Read operand stack pointer Read operand stack pointer
Execute	$\text{valE} \leftarrow \text{valB} + 8$	Increment stack pointer
Memory	$\text{valM} \leftarrow M_8[\text{valA}]$	Read return address
Write back	$R[\%rsp] \leftarrow \text{valE}$	Update stack pointer
PC update	$\text{PC} \leftarrow \text{valM}$	Set PC to return address

- Use ALU to increment stack pointer
- Read return address from memory

RET Operation

Now showing inputs and outputs for SEQ:

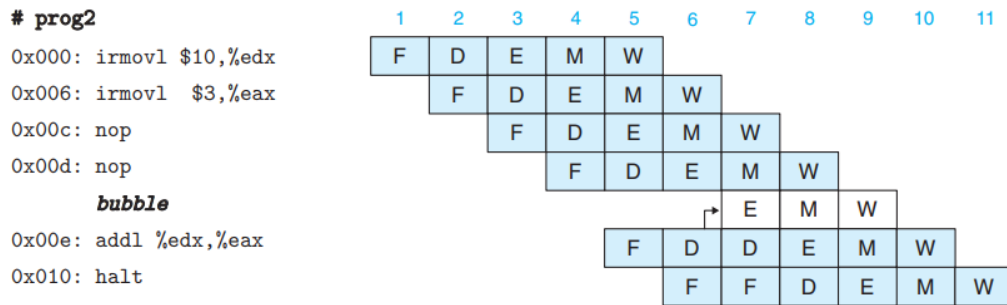
AT LAST i have kept:

Pipeline Architecture :

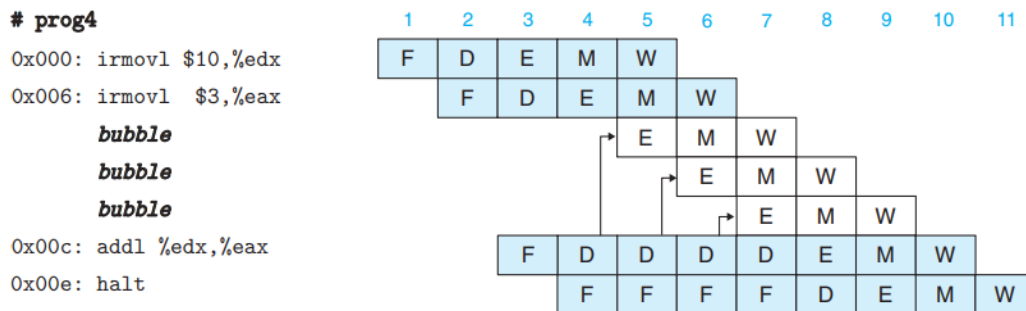
- We've developed a 5-stage pipelined architecture for designing a processor compatible with the Y-86 instruction set.
- The Fetch, Decode, Execute, Memory, and Writeback stages are separated by pipeline registers. These registers update at each positive edge of the clock.
- Instructions enter the pipeline starting from the Fetch stage. Once an instruction completes execution, the next instruction in sequence is fed into the pipeline at the positive edge of the next clock cycle e i.e the first instruction which is in fetch stage will go to decode stage and the 2nd instruction will go into fetch stage. This process continues until all instructions have been executed.
- **Data hazards** occur when an instruction that needs a register as a source follows closely after an instruction that writes to the same register. This is a common issue that we want to avoid as it can slow down the pipeline.
- **Control hazards** arise when there's a misprediction of a conditional branch. For instance, our design may predict all branches as taken, leading to the execution of extra instructions unnecessarily. Additionally, getting the return address for the "ret" instruction might require executing three extra instructions in a naive pipeline design.
- Ensuring the pipeline works effectively also involves considering scenarios where multiple special cases happen simultaneously. This requires careful design and testing to handle such situations appropriately.

Avoiding Data Hazards using stalls :

- In below execution, after decoding the addl instruction in cycle 6, the stall control logic detects a data hazard due to the pending write to register stage. It injects a bubble into execute stage and repeats the decoding of the addl instruction in cycle 7. In effect, the machine has dynamically inserted a nop instruction, giving a flow similar to that shown for prog1



- In another execution below, after decoding the addl instruction in cycle 4, the stall control logic detects data hazards for both source registers. It injects a bubble into the execute stage and repeats the decoding of the addl instruction on cycle 5. It again detects hazards for both source registers, injects a bubble into the execute stage, and repeats the decoding of the addl instruction on cycle 6. Still, it detects a hazard for source register of the addl instruction on cycle 7. In effect, the machine has dynamically inserted three nop instructions,



Avoiding Data Hazards by Forwarding :

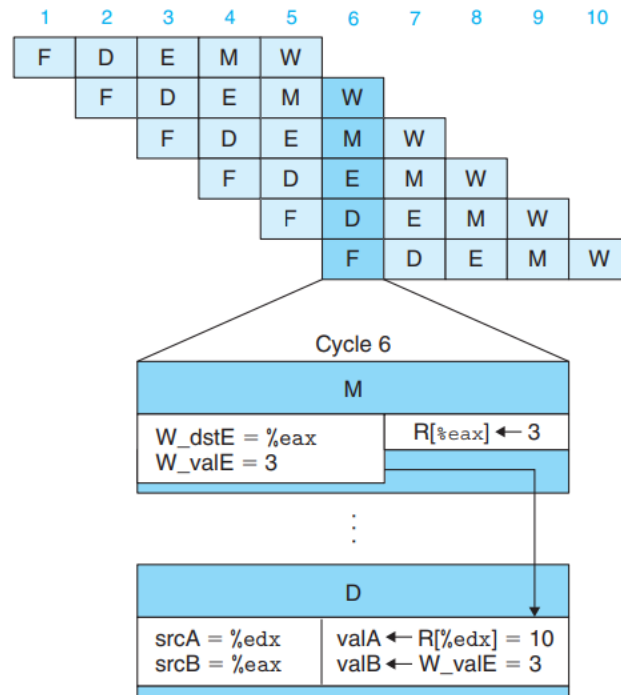
- The technique of passing a result value directly from one pipeline stage to an earlier one is commonly known as data forwarding (or simply forwarding, and sometimes bypassing).
- In cycle 6, the decode stage logic detects the presence of a pending write to register eax in the write-back stage. It uses this value for source operand valB rather than the value read from the register file.

prog2

```

0x000: irmovl $10,%edx
0x006: irmovl $3,%eax
0x00c: nop
0x00d: nop
0x00e: addl %edx,%eax
0x010: halt

```



Pipeline registers :

Fetch register : The Fetch register stores the predicted value of the Program Counter (PC), denoted as F_pred_PC. It takes this predicted PC value and stores it as F_predPC, which serves as an input for the fetch block.

Decode registers : The Decode register stores the values of D_iCode, D_iFun, D_stat, D_rA, D_rB, D_valC, and D_valP. These values correspond to the signals icode, ifun, stat, rA, rB, valC, and valP of the instruction currently present in the decode stage. These values are essential for the functioning of the decode stage.

Execute register : The Execute register stores the values of E_stat, E_icode, E_ifun, E_valC, E_valA, E_valB, E_rA, E_rB, and E_valP. These values correspond to the signals stat, icode, ifun, valC, valA, valB, rA, rB, and valP of the instruction currently present in the execute stage. This register facilitates the passing of all outputs, including the values passed on from the previous stage register, to subsequent stages.

Memory register : The Memory register stores the values of M_stat, M_icode, M_Cnd, M_valE, M_valA, M_rB, M_rA, M_valP, M_valC, and

M_valB. These values represent the signals stat, icode, Cnd, valE, valA, rB, rA, valP, valC, and valB of the instruction currently in the memory stage.

Writeback register :The Writeback register contains the values of W_Cnd, M_valE, M_valM, W_stat, W_iCode, W_valE, W_valM, W_rB, W_rA, W_valC, W_valA, W_valB, and W_valP. These values represent the signals of the instruction currently in the writeback stage.

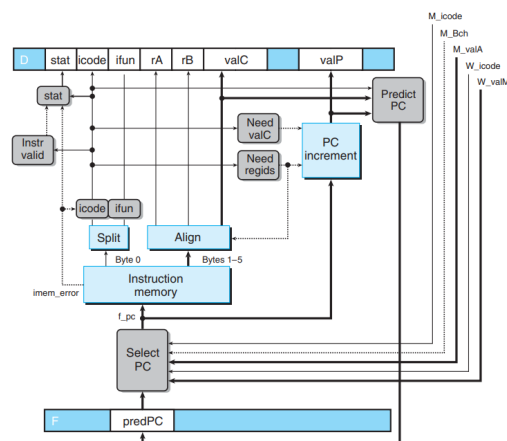
- The signals stored in these registers are utilized by combinational logic circuits in their corresponding stages (fetch, decode, execute, memory, and writeback). This design ensures that each instruction can be executed independently, without relying on previous stages in the pipeline.

Combinational Logics :

Fetch :

The combinational logic in the Fetch stage is responsible for several tasks:

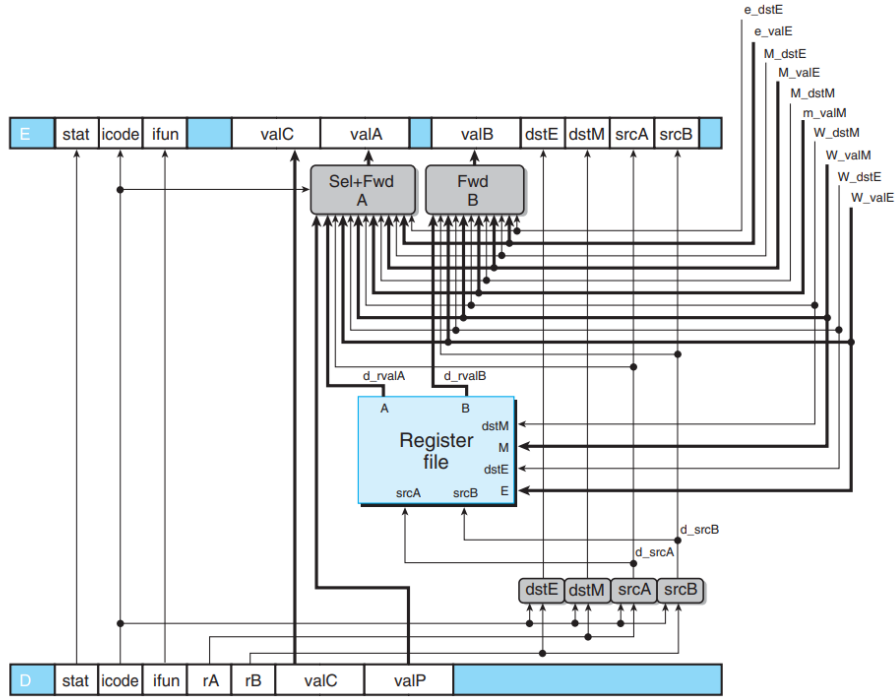
1. Selecting the current Program Counter (PC).
2. Reading the instruction from memory.
3. Calculating various signals including `f_stat`, `f_lcode`, `f_ifun`, `rA`, `rB`, `f_valC`, `f_valP`, `f_instr_Validity`, `f_imem_error`, and `f_HF`.



Within the one cycle time limit, the processor can only predict the address of the next instruction

Decode Writeback :

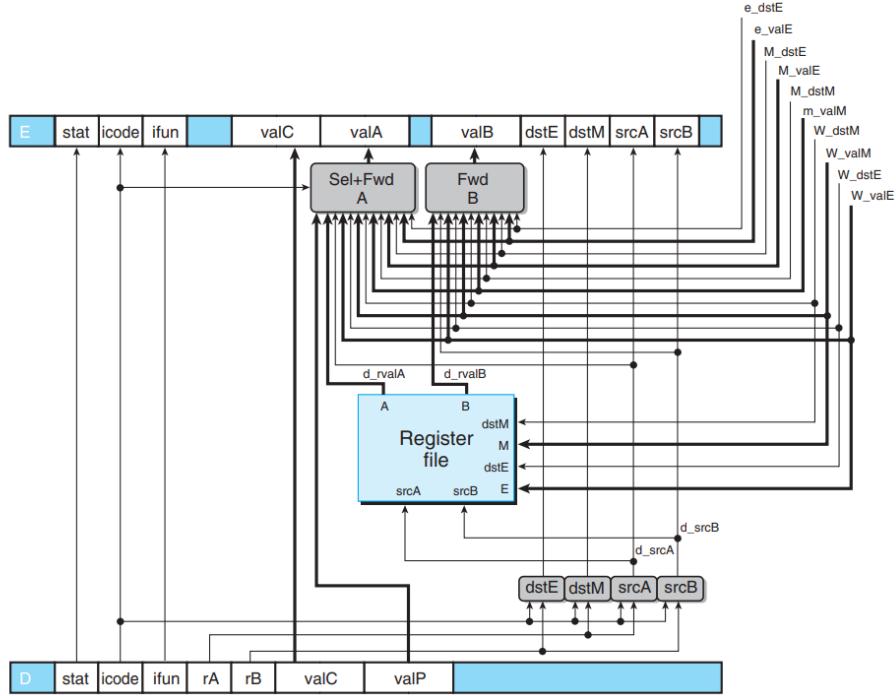
1. In the Decode stage, the logic extracts valA and valB from the inputs rA and rB. Additionally, this stage plays a critical role in data forwarding, crucial for handling data dependencies. It determines whether to obtain data from subsequent pipeline stages or directly from the register file, based on these dependencies.
2. Similarly, in the Writeback stage, the logic updates or writes back the result into the register, whether it's valE or valM.
3. The logic blocks labeled “Instr valid,” “Need regids,” and “Need valC” are the same as for SEQ.



PIPE decode and write-back stage logic. No instruction requires both valP and the value read from register port A, and so these two can be merged to form the signal valA for later stages. The block labeled “Sel+Fwd A” performs this task and also implements the forwarding logic for source operand valA. The block labeled “Fwd B” implements the forwarding logic for source operand valB. The register write locations are specified by the dstE and dstM signals from the write-back stage rather than from the decode stage, since it is writing the results of the instruction currently in the write-back stage.

Execute :

- In the Execute stage, the logic computes e_valE and the condition signal e_Cnd using the Arithmetic Logic Unit (ALU). This block remains largely unchanged from the sequential implementation.



This part of the design is very similar to the logic in the SEQ implementation.

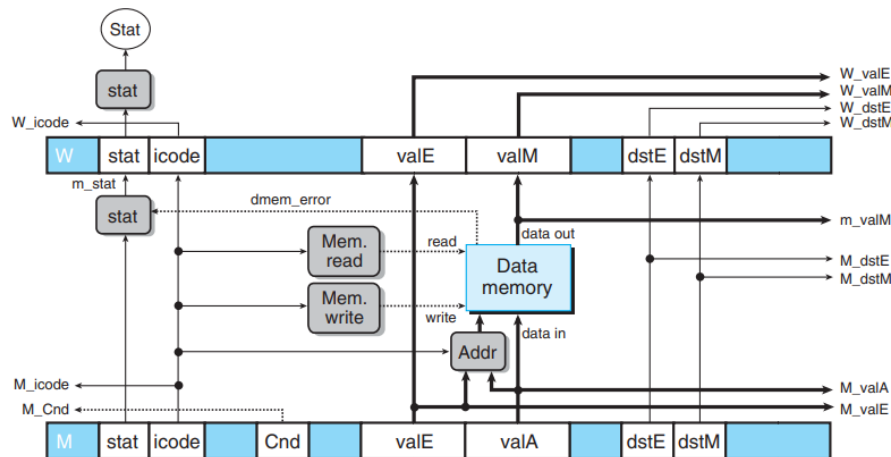
- The logic labeled “Set CC,” which determines whether or not update the condition codes, has signals m_stat and W_stat as inputs. These signals are used to detect cases where an instruction causing an exception is passing through later pipeline stages, and therefore any updating of the condition codes should be suppressed.

Memory :

- In the Memory stage, the processor reads from or writes to the data memory. It calculates the signals $valM$ and $data_memory_error$, obtaining its input from the memory register.
- The block labeled “Data” in SEQ is not present in PIPE. This block served to select between data sources $valP$ (for call instructions) and

valA, but this selection is now performed by the block labeled “Sel+Fwd A” in the decode stage. Most other blocks in this stage are identical to their counterparts in SEQ, with an appropriate renaming of the signals.

- In below figure, we can also see that many of the values in pipeline registers M and W are supplied to other parts of the circuit as part of the forwarding and pipeline control logic.



Many of the signals from pipeline registers M and W are passed down to earlier stages to provide write-back results, instruction addresses, and forwarded results.

Pipeline Control Logic:

This logic must handle the following four control cases for which other mechanisms, such as data forwarding and branch prediction, do not suffice:

- **Processing ret:** The pipeline must stall until the ret instruction reaches the write-back stage.
- **Load/use hazards:** The pipeline must stall for one cycle between an instruction that reads a value from memory and an instruction that uses this value.
- **Mispredicted branches:** By the time the branch logic detects that a jump should not have been taken, several instructions at the branch

target will have started down the pipeline. These instructions must be removed from the pipeline.

- **Exceptions:** When an instruction causes an exception, we want to disable the updating of the programmer-visible state by later instructions and halt execution once the excepting instruction reaches the write-back stage.

Detection conditions for pipeline control logic :

- Four different conditions require altering the pipeline flow by either stalling the pipeline or canceling partially executed instructions.

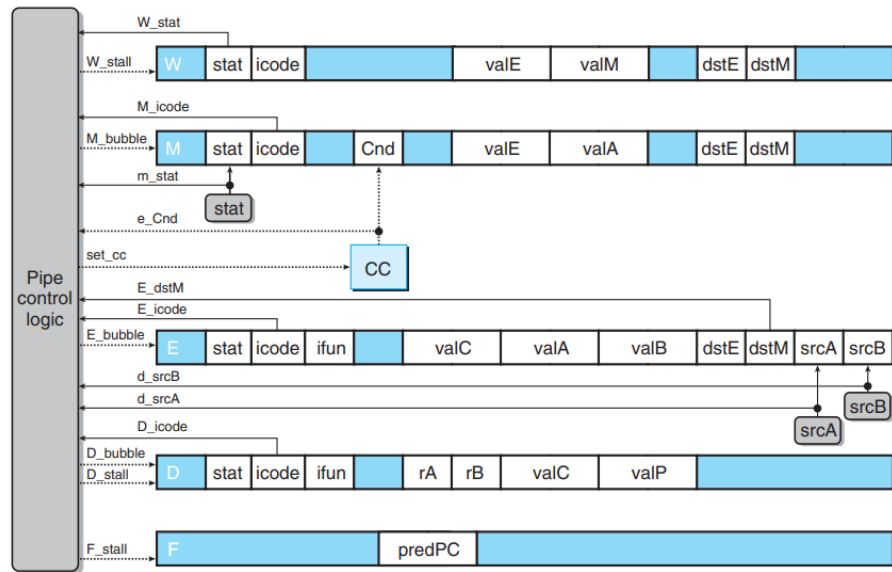
Condition	Trigger
Processing ret	$I_{RET} \in \{D_icode, E_icode, M_icode\}$
Load/use hazard	$E_icode \in \{IMRMOVL, IPOPL\} \ \&\& \ E_dstM \in \{d_srcA, d_srcB\}$
Mispredicted branch	$E_icode = IJXX \ \&\& \ !e_Cnd$
Exception	$m_stat \in \{SADR, SINS, SHLT\} \ \ W_stat \in \{SADR, SINS, SHLT\}$

Actions for pipeline control logic:

- The different conditions require altering the pipeline flow by either stalling the pipeline or by canceling partially executed instructions.

Condition	Pipeline register				
	F	D	E	M	W
Processing ret	stall	bubble	normal	normal	normal
Load/use hazard	stall	stall	bubble	normal	normal
Mispredicted branch	normal	bubble	bubble	normal	normal

- Based on signals from the pipeline registers and pipeline stages, the control logic generates stall and bubble control signals for the pipeline registers, and also determines whether the condition code registers should be updated.



This logic overrides the normal flow of instructions through the pipeline to handle special conditions such as procedure returns, mispredicted branches, load/use hazards, and program exceptions.

Now showing inputs and outputs :

Our input :

```
instruction_set[0] = 8'b00010000; // 1 0 : no operation

instruction_set[1] = 8'b01100011; //2 fn : OPq
instruction_set[2] = 8'b01100111; //rA rB

instruction_set[3] = 8'b00110000; //3 fn : irmovq
instruction_set[4] = 8'b01100111; //rA rB
instruction_set[5] = 8'b00000000;
instruction_set[6] = 8'b00000000;
instruction_set[7] = 8'b00000000;
instruction_set[8] = 8'b00000000;
instruction_set[9] = 8'b00000000;
instruction_set[10] = 8'b00000000;
instruction_set[11] = 8'b00000000;
instruction_set[12] = 8'b00000111;
```

```

instruction_set[13] = 8'b01000000; //4 fn : rmmovq
instruction_set[14] = 8'b01100111; //rA rB
instruction_set[15] = 8'b00000000;
instruction_set[16] = 8'b00000000;
instruction_set[17] = 8'b00000000;
instruction_set[18] = 8'b00000000;
instruction_set[19] = 8'b00000000;
instruction_set[20] = 8'b00000000;
instruction_set[21] = 8'b00000000;
instruction_set[22] = 8'b00000011;

```

```

instruction_set[23] = 8'b01010000; //5 fn : mromvq
instruction_set[24] = 8'b10000111; //rA rB
instruction_set[25] = 8'b00000000;
instruction_set[26] = 8'b00000000;
instruction_set[27] = 8'b00000000;
instruction_set[28] = 8'b00000000;
instruction_set[29] = 8'b00000000;
instruction_set[30] = 8'b00000000;
instruction_set[31] = 8'b00000000;
instruction_set[32] = 8'b00000011;

```

```

instruction_set[33] = 8'b01100000; //6 fn : OPq
instruction_set[34] = 8'b01100111; //rA rB

```

```

instruction_set[35] = 8'b01110001; //7 fn : jXX
instruction_set[36] = 8'b00000000;
instruction_set[37] = 8'b00000000;
instruction_set[38] = 8'b00000000;
instruction_set[39] = 8'b00000000;
instruction_set[40] = 8'b00000000;
instruction_set[41] = 8'b00000000;
instruction_set[42] = 8'b00000000;
instruction_set[43] = 8'b00011000;

```

```

instruction_set[44] = 8'b10000000; //8 fn : Call
instruction_set[45] = 8'b00000000;
instruction_set[46] = 8'b00000000;
instruction_set[47] = 8'b00000000;
instruction_set[48] = 8'b00000000;
instruction_set[49] = 8'b00000000;

```



```
rsi : x
rdi : x
r8 : x
r9 : x
r10 : x
r11 : x
r12 : x
r13 : x
r14 : x
```

```
Value_E : x
Value_M : x
```

Condition satisfy check : 0

Overflow flag : 0

```
address memory error : x
```

```
status of memory : x
```

————STATUS FLAGS : ————

Memory Address flag : x

Instruction code flag : x

```
clk : 0
```

PC Address : x

Instruction invalid Check : x

Need for Val_C : x

[illegible]
$$\text{Val } P = \quad \quad \quad x$$

```

register A : xxxx
register B : xxxx
PROGRAM REGISTER VALUES:

```

```

rax  :          x
rcx  :          x
rdx  :          x
rbx  :          x
rsp  :          x
rbp  :          x
rsi  :          x
rdi  :          x
r8   :          x
r9   :          x
r10  :          x
r11  :          x
r12  :          x
r13  :          x
r14  :          x

```

```

Value_A :          x
Value_B :          x

```

```

Value_E :          x
Value_M :          x

```

```
No. of valid instructions :          300
```

```
Condition satisfy check : 0
```

```
signed flag : 0
```

```
Overflow flag : 0
```

```
Zero Flag : 0
```

```
address memory error : x
```

```
instruction invalid address : x
```

```
status of memory : x
```

```
new pc address :          x
```

```
————STATUS FLAGS : —————
```

```
ALL OK FLAG : x
```

```
Memory Address flag : x
```

```
Halt Flag : x
```

```
Instruction code flag : x
```

```
TIME INSTANT :          2
```



```
Value_B : x
-----
Value_E : x
Value_M : x
No. of valid instructions : 300
Condition satisfy check : 0
signed flag : 0
Overflow flag : 0
Zero Flag : 0
address memory error : x
instruction invalid address : x
status of memory : x
new pc address : x
-----STATUS FLAGS : -----
ALL OK FLAG : x
Memory Address flag : x
Halt Flag : x
Instruction code flag : x

TIME INSTANT : 10
clk : 1
Memory invalid check : 0
PC Adress : 0
Instrction code : 0001
Instruction invalid Check : 0
Function code : 0000
Need for Val_C : 0
Need for registers : 0
Val_C = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Val P = 8
register A : xxxx
register B : xxxx
PROGRAM REGISTER VALUES:
-----
rax : 1
rcx : 2
rdx : 4
rbx : 8
rsp : 256
rbp : 32
rsi : 64
```


rdi :	128
r8 :	256
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

```
Value_A : x
Value_B : x
```

```
Value_E : x
Value_M : x
```

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

```
address memory error : x
```

```
instruction invalid adress : x
```

```
status of memory : x
```

```
new pc adress :      x
```

————STATUS FLAGS : ————

ALL OK FLAG : x

Memory Address flag : x

Halt Flag : x

Instruction code flag : x

TIME INSTANT : 14

clk : 1

Memory invalid check : 0

PC Address : 0

Instruction code : 0001

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 0

Need for registers : 0

[illegible]

Val P = 8

```
register A : xxxx
```

register B : xxxx

PROGRAM REGISTER VALUES:

rax :	1
rcx :	2
rdx :	4
rbx :	8
rsp :	256
rbp :	32
rsi :	64
rdi :	128
r8 :	256
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

Value_A :	x
Value_B :	x

Value_E :	x
Value_M :	x

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

address memory error : x

instruction invalid address : x

status of memory : x

new pc address : x

——STATUS FLAGS : ——

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 20

clk : 0


```
Value_E : x
Value_M : x
No. of valid instructions : 300
Condition satisfy check : 0
signed flag : 0
Overflow flag : 0
Zero Flag : 0
address memory error : x
instruction invalid address : x
status of memory : x
new pc address : 8
-----STATUS FLAGS : -----
ALL OK FLAG : 1
Memory Adress flag : 0
Halt Flag : 0
Instruction code flag : 0

TIME INSTANT : 29
clk : 0
Memory invalid check : 0
PC Address : 8
Instrection code : 0001
Instruction invalid Check : 0
Function code : 0000
Need for Val_C : 0
Need for registers : 0
Val_C = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Val P = 8
register A : xxxx
register B : xxxx
PROGRAM REGISTER VALUES:
-----
rax : 1
rcx : 2
rdx : 4
rbx : 8
rsp : 256
rbp : 32
rsi : 64
rdi : 128
```

r8 :	256
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

```
Value_E : x
Value_M : x
```

Condition satisfy check : 0

Overflow flag : 0

```
address memory error : x
```

```
status of memory : x
```

————STATUS FLAGS : ————

Memory Address flag : 0

Instruction code flag : 0

TIME INSTANT : 30

Memory invalid check : 0

Instruction code : 0110

Function code : 0011

Need for registers : 1

Val P = 24

register B : 0111

PROGRAM REGISTER VALUES:

rax :	1
rcx :	2
rdx :	4
rbx :	8
rsp :	256
rbp :	32
rsi :	64
rdi :	128
r8 :	256
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

Value_A :	x
Value_B :	x

Value_E :	x
Value_M :	x

No. of valid instructions :	300
-----------------------------	-----

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

address memory error : x

instruction invalid address : x

status of memory : x

new pc address :	8
------------------	---

STATUS FLAGS : —————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT :	31
----------------	----

clk : 1

Memory invalid check : 0

PC Address : 8

Instruction code : 0110

Instruction invalid Check : 0

Function code : 0011

Need for Val_C : 0

Need for registers : 1

[illegible]

Val P = 24

register A : 0110

```

register B : 0111

```

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

$$\text{rcx} : 2$$

rdx : 4

rbx : 8

```
rsp    : 256
```

32

rsi : 64

```
rdi : 128
```

r8 : 256

r9 : 512

r10	:	1024
-----	---	------

r11	:	2048
-----	---	------

```

r12  : 4096

```

r13	:	8192
-----	---	------

r14	:	16384
-----	---	-------

Value_A : 64

Value_B : 128

Value_E : x

Value_M : x

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

```

address memory error : x

```

```
instruction invalid adress : x
```

```
status of memory : x
```



```
new pc adress : 8
```

————STATUS FLAGS : ————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

```
-----in_xnor1  : 0-----
```

```

-----in_xnor2  : 0-----

```

```
-----in_xor11  : 0-----
```

```
-----in_xor12  : 0-----
```

_____in_and21 : x_____

————in_and22 : x————

————out_and2 : x —————

SIGNED FLAG = 0

OVERFLOW FLAG = x

ZERO FLAG = 0

TIME INSTANT : 38

clk : 1

Memory invalid check : 0

PC Address : 8

Instruction code : 0110

Instruction invalid Check : 0

Function code : 0011

Need for Val_C : 0

Need for registers : 1

[illegible]
$$\text{Val P} = 24$$

register A : 0110

register B : 0111

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx : 2

rdx : 4

rbx : 8

```
rsp      : 256
```

rbp : 32

rsi : 64

```
rdi : 128
```

r8	:	256
----	---	-----

<hr/>		
rax :	1	
rcx :	2	
rdx :	4	
rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	128	
r8 :	256	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	64	
Value_B :	128	
<hr/>		
Value_E :	192	
Value_M :	x	
No. of valid instructions :		300
Condition satisfy check :	0	
signed flag :	0	
Overflow flag :	x	
Zero Flag :	0	
address memory error :	x	
instruction invalid address :	x	
status of memory :	x	
new pc address :		8
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Address flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
TIME INSTANT :		42
clk :	0	
Memory invalid check :	0	
PC Address :		8


```
Value_M : x
No. of valid instructions : 300
Condition satisfy check : 0
signed flag : 0
Overflow flag : x
Zero Flag : 0
address memory error : x
instruction invalid address : x
status of memory : x
new pc address : 24
-----STATUS FLAGS : -----
ALL OK FLAG : 1
Memory Address flag : 0
Halt Flag : 0
Instruction code flag : 0

TIME INSTANT : 49
clk : 0
Memory invalid check : 0
PC Address : 24
Instrection code : 0110
Instruction invalid Check : 0
Function code : 0011
Need for Val_C : 0
Need for registers : 1
Val_C = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Val P = 24
register A : 0110
register B : 0111
PROGRAM REGISTER VALUES:
```

```
rax : 1
rcx : 2
rdx : 4
rbx : 8
rsp : 256
rbp : 32
rsi : 64
rdi : 192
r8 : 256
r9 : 512
```

```
Value_A : 64
Value_B : 128
```

No. of valid instructions : 300

signed flag : 0

Zero Flag : 0

```
instruction invalid adress : x
```

```
new pc address : 24
```

ALL OK FLAG : 1

Halt Flag : 0

TIME INSTANT : 50

Memory invalid check : 0

Instruction code : 0011

Function code : 0000

Need for registers : 1

[illegible]

register A : 0110

```

      8
register B : 0111

```

PROGRAM REGISTER VALUES:

rax :	1	
rcx :	2	
rdx :	4	
rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	192	
r8 :	256	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	x	
Value_B :	x	
<hr/>		
Value_E :	x	
Value_M :	x	
No. of valid instructions :		300
Condition satisfy check :	0	
signed flag :	0	
Overflow flag :	x	
Zero Flag :	0	
address memory error :	x	
instruction invalid address :	x	
status of memory :	x	
new pc address :		24
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Adress flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
TIME INSTANT :		53
clk :	1	
Memory invalid check :	0	
PC Address :		24
Instrection code :	0011	

No. of valid instructions : 300

TIME INSTANT : 62

```

rax   : 1
rcx   : 2
rdx   : 4
rbx   : 8
rsp   : 256
rbp   : 32
rsi   : 64
rdi   : 7
r8    : 256
r9    : 512
r10   : 1024

```

r11	:	2048
r12	:	4096
r13	:	8192
r14	:	16384

```
Value_E : 7
Value_M : x
```

Condition satisfy check : x

Overflow flag : x

```
address memory error : x
```

```
status of memory : x
```

————STATUS FLAGS : ————

Memory Address flag : 0

Instruction code flag : 0

```
clk : 0
```

PC Address : 24

Instruction invalid Check : 0

Need for Val_C : 1

```
Val_C = 0000000000000000000000000000000000000000000000000000000
```

Val P = 104

register B : 0111

PROGRAM REGISTER VALUES:

```

rcx :          2
rdx :          4
rbx :          8
rsp :        256
rbp :         32
rsi :         64
rdi :          7
r8  :        256
r9  :        512
r10 :       1024
r11 :       2048
r12 :       4096
r13 :       8192
r14 :      16384

```

```

Value_A :          x
Value_B :          x

```

```

Value_E :          7
Value_M :          x

```

```
No. of valid instructions :          300
```

```
Condition satisfy check : x
```

```
signed flag : 0
```

```
Overflow flag : x
```

```
Zero Flag : 0
```

```
address memory error : x
```

```
instruction invalid address : x
```

```
status of memory : x
```

```
new pc address :          104
```

```
-----STATUS FLAGS : -----
```

```
ALL OK FLAG : 1
```

```
Memory Address flag : 0
```

```
Halt Flag : 0
```

```
Instruction code flag : 0
```

```
TIME INSTANT :          69
```

```
clk : 0
```

```
Memory invalid check : 0
```

```
PC Address :          104
```

```
Instruction code : 0011
```

```
Instruction invalid Check : 0
```



```

Condition satisfy check : x
signed flag : 0
Overflow flag : x
Zero Flag : 0
address memory error : x
instruction invalid address : x
status of memory : x
new pc address :
-----STATUS FLAGS : -----
ALL OK FLAG : 1
Memory Address flag : 0
Halt Flag : 0
Instruction code flag : 0

```

ALL OK FLAG : 1

Halt Flag : 0

TIME INSTANT : 71

Memory invalid check : 0

Instruction code : 0100

Function code : 0000

Need for registers : 1

Val P = 184

register B : 0111

```
rax    :                               1
```

rdx : 4

```
rsp      : 256
```

rsi : 64

r8 : 256

r9 : 512

```
r10 : 1024
```

r11 : 2048


```
Value_A : 64
Value_B : 7
```

No. of valid instructions : 300

signed flag : 0

Zero Flag : 0

```
instruction invalid adress : x
```

```
new pc address : 104
```

ALL OK FLAG : 1

Halt Flag : 0

Instruction code flag : 0

clk : 1

PC Address : 104

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 1

Need for registers : 1

[illegible]

Val P = 184

register A : 0110

```

      8
register B : 0111

```

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx : 2

```

rdx :          4
rbx :          8
rsp :        256
rbp :         32
rsi :         64
rdi :          7
r8  :        256
r9  :        512
r10 :       1024
r11 :       2048
r12 :       4096
r13 :       8192
r14 :      16384

```

```

Value_A :          64
Value_B :           7

```

```

Value_E :          10
Value_M :           x

```

```
No. of valid instructions :          300
```

```
Condition satisfy check : x
```

```
signed flag : 0
```

```
Overflow flag : x
```

```
Zero Flag : 0
```

```
address memory error : x
```

```
instruction invalid address : x
```

```
status of memory : x
```

```
new pc address :          104
```

```
———STATUS FLAGS : ——
```

```
ALL OK FLAG : 1
```

```
Memory Address flag : 0
```

```
Halt Flag : 0
```

```
Instruction code flag : 0
```

```
——— Memory data value =          64———
```

```
——— Memory Status : Data pushed from register to memory ——
```

```
TIME INSTANT :          79
```

```
clk : 1
```

```
Memory invalid check : 0
```

```
PC Address :          104
```

```
Instrection code : 0100
```



```
ALL OK FLAG      : 1
Memory Address flag : 0
Halt Flag       : 0
Instruction code flag : 0
```

TIME INSTANT : 80

clk : 0

```
Memory invalid check : 0
```

PC Address : 104

Instruction code : 0100

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 1

Need for registers : 1

```
Val_C =   0000000000000000000000000000000000000000000000000000000
```

Val P = 184

register A : 0110

register B : 0111

PROGRAM REGISTER VALUES:

rax	:	1
rcx	:	2
rdx	:	4
rbx	:	8
rsp	:	256
rbp	:	32
rsi	:	64
rdi	:	7
r8	:	256
r9	:	512
r10	:	1024
r11	:	2048
r12	:	4096
r13	:	8192
r14	:	16384

```
Value_A : 64
Value_B : 7
```

```
Value_E : 10
Value_M : x
```

No. of valid instructions : 300

TIME INSTANT : 83

```
rax    :                               1
```

r11	:	2048
r12	:	4096
r13	:	8192
r14	:	16384

```
Value_A : 64
Value_B : 7
```

```
Value_E : 10
Value_M : x
```

No. of valid instructions : 300

Condition satisfy check : x

signed flag : 0

Overflow flag : x

Zero Flag : 0

```
address memory error : 0
```

```
instruction invalid adress : x
```

```
status of memory : 1
```

```
new pc address : 184
```

————STATUS FLAGS : ————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 89

```
clk : 0
```

Memory invalid check : 0

PC Address : 184

Instruction code : 0100

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 1

Need for registers : 1

[illegible]

Val P = 184

register A : 0110

register B : 0111

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx :	2	
rdx :	4	
rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	7	
r8 :	256	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	64	
Value_B :	7	
<hr/>		
Value_E :	10	
Value_M :	x	
No. of valid instructions :		300
Condition satisfy check :	x	
signed flag :	0	
Overflow flag :	x	
Zero Flag :	0	
address memory error :	0	
instruction invalid address :	x	
status of memory :	1	
new pc adress :		184
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Adress flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
TIME INSTANT :		90
clk :	1	
Memory invalid check :	0	
PC Adress :		184
Instrection code :	0101	
Instruction invalid Check :	0	


```
TIME INSTANT : 91
clk : 1
```

PC Address : 184

Instruction invalid Check : 0

Need for Val_C : 1

[illegible]

register A : 1000

```

      8
register B : 0111

```

```

rax      :      1
rcx      :      2
rdx      :      4
rbx      :      8
rsp      :     256
rbp      :     32
rsi      :     64
rdi      :      7
r8       :    256
r9       :    512
r10      :   1024
r11      :   2048
r12      :   4096
r13      :   8192
r14      :  16384

```

```
Value_A : x
Value_B : 7
```

```
Value_E : x
Value_M : x
```

No. of valid instructions : 300

```

Condition satisfy check : x
signed flag : 0
Overflow flag : x
Zero Flag : 0
address memory error : x
instruction invalid address : x
status of memory : x
new pc address :
-----STATUS FLAGS : -----
ALL OK FLAG : 1
Memory Address flag : 0
Halt Flag : 0
Instruction code flag : 0

```

ALL OK FLAG : 1

Halt Flag : 0

TIME INSTANT : 98

Memory invalid check : 0

Instruction code : 0101

Function code : 0000

Need for registers : 1

Val P = 264

```
register A : 1000
```

PROGRAM REGISTER

```
rax    :                               1
```

rdx : 4

rSD : 256

```

rsi : 64

```

r8 : 256

r8	:	256
r9	:	512

r0	:	512
r10	:	1024

r11	:	2048
-----	---	------

r12 :	4096
r13 :	8192
r14 :	16384

```
Value_E : 10
Value_M : x
```

Condition satisfy check : x

Overflow flag : x

```
address memory error : x
```

```
status of memory : x
```

————STATUS FLAGS : ————

Memory Address flag : 0

Instruction code flag : 0

64

TIME INSTANT : 99

Memory invalid check : 0

Instruction code : 0101

Function code : 0000

Need for registers : 1

Val P = 264

```

register B : 0111

```

rax :	1	
rcx :	2	
rdx :	4	
rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	7	
r8 :	256	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	

Value_A :	x	
Value_B :	7	

Value_E :	10	
Value_M :	64	
No. of valid instructions :		300
Condition satisfy check :	x	
signed flag :	0	
Overflow flag :	x	
Zero Flag :	0	
address memory error :	0	
instruction invalid address :	0	
status of memory :	1	
new pc address :		184

STATUS FLAGS :

ALL OK FLAG :	1	
Memory Address flag :	0	
Halt Flag :	0	
Instruction code flag :	0	

TIME INSTANT :	100	
clk :	0	
Memory invalid check :	0	
PC Address :		184

[illegible]

```
Value_A : x
Value_B : 7
```

No. of valid instructions : 300

signed flag : 0

Zero Flag : 0

```
instruction invalid adress : 0
```

```
new pc address : 264
```

ALL OK FLAG : 1

Halt Flag : 0

TIME INSTANT : 109

Memory invalid check : 0

Instruction code : 0101

Function code : 0000

Need for registers : 1

[illegible]

register A : 1000

```

      8
register B : 0111

```

80

rax :	1	
rcx :	2	
rdx :	4	
rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	7	
r8 :	64	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	x	
Value_B :	7	
<hr/>		
Value_E :	10	
Value_M :	64	
No. of valid instructions :		300
Condition satisfy check :	x	
signed flag :	0	
Overflow flag :	x	
Zero Flag :	0	
address memory error :	0	
instruction invalid address :	0	
status of memory :	1	
new pc address :		264
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Address flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
TIME INSTANT :		110
clk :	1	
Memory invalid check :	0	
PC Address :		264
Instrection code :	0110	

rcx :	2	
rdx :	4	
rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	7	
r8 :	64	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	64	
Value_B :	7	
<hr/>		
Value_E :	71	
Value_M :	64	
No. of valid instructions :		300
Condition satisfy check :	x	
signed flag :	0	
Overflow flag :	0	
Zero Flag :	0	
address memory error :	x	
instruction invalid address :	x	
status of memory :	x	
new pc address :		264
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Address flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
TIME INSTANT :		120
clk :	0	
Memory invalid check :	0	
PC Address :		264
Instrection code :	0110	
Instruction invalid Check :	0	


```

Condition satisfy check : x
signed flag : 0
Overflow flag : 0
Zero Flag : 0
address memory error : x
instruction invalid address : x
status of memory : x
new pc address :
-----STATUS FLAGS : -----
ALL OK FLAG : 1
Memory Address flag : 0
Halt Flag : 0
Instruction code flag : 0

```

ALL OK FLAG : 1

Halt Flag : 0

TIME INSTANT : 123

Memory invalid check : 0

Instruction code : 0110

Function code : 0000

Need for registers : 1

Val P = 280

```

      8
register B : 0111

```

```

rax   : 1
rcx   : 2
rdx   : 4
rbx   : 8
rsp   : 256
rbp   : 32
rsi   : 64
rdi   : 71
r8     : 64
r9     : 512
r10    : 1024
r11    : 2048

```



```
Value_A : 64
Value_B : 7
```

No. of valid instructions : 300

signed flag : 0

Zero Flag : 0

```
instruction invalid adress : x
```

```
new pc address : 280
```

ALL OK FLAG : 1

Halt Flag : 0

Instruction code flag : 0

```
clk : 0
```

PC Address : 280

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 0

Need for registers : 1

[illegible]

Val P = 280

register A : 0110

register B : 0111

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx : 2

rdx :	4	
rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	71	
r8 :	64	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	64	
Value_B :	7	
<hr/>		
Value_E :	71	
Value_M :	64	
No. of valid instructions :		300
Condition satisfy check :	x	
signed flag :	0	
Overflow flag :	0	
Zero Flag :	0	
address memory error :	x	
instruction invalid address :	x	
status of memory :	x	
new pc address :		280
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Address flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
<hr/>		
TIME INSTANT :		130
clk :	1	
Memory invalid check :	0	
PC Address :		280
Instrection code :	0111	
Instruction invalid Check :	0	
Function code :	0001	


```
Halt Flag : 0
Instruction code flag : 0
```

TIME INSTANT : 133

clk : 1

```
Memory invalid check : 0
```

PC Address : 280

Instruction code : 0111

Instruction invalid Check : 0

Function code : 0001

Need for Val_C : 1

Need for registers : 0

[illegible]

Val P = 352

register A : 0110

```

register B : 0111

```

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

$$\Gamma_{CX} : \quad 2$$
$$\text{rdx} : 4$$

rbx : 8

rsp : 256

32

rsi : 64

rdi : 71

r8 : 64

r9 : 512

r10	:	1024
-----	---	------

r10	:	1024
r11	:	2048

r11	:	2018
r12	:	4096

r12	:	1999
r13	:	8192

r13	:	5192
r14	:	16384

Value_A : x

Value_B : x

Value_E : x

Value_M : 64

No. of valid instructions :	300
-----------------------------	-----

Condition satisfy check : 0

```
signed flag : 0
Overflow flag : 0
Zero Flag : 0
address memory error : x
instruction invalid adress : x
status of memory : x
new pc address : 280
```

TIME INSTANT : 140

Memory invalid check : 0

Instruction code : 0111

Function code : 0001

Need for registers : 0

Val P = 352

register B : 0111

rcx : 2

rbx : 8

rbp : 32

rdi : 71

r9 : 512

```
r11 : 2048
```

r13 :	8192
r14 :	16384

```
Value_A : x
Value_B : x
```

```
Value_E : x
Value_M : 64
```

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

```
address memory error : x
```

```
instruction invalid adress : x
```

```
status of memory : x
```

```
new pc address : 280
```

————STATUS FLAGS : ————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 143

```
clk : 0
```

```
Memory invalid check : 0
```

PC Address : 280

Instruction code : 0111

Instruction invalid Check : 0

Function code : 0001

Need for Val_C : 1

Need for registers : 0

[illegible]

Val P = 352

register A : 0110

register B : 0111

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

$$\mathrm{rcx} \quad : \quad 2$$

rdx : 4

rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	71	
r8 :	64	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	x	
Value_B :	x	
<hr/>		
Value_E :	x	
Value_M :	64	
No. of valid instructions :		300
Condition satisfy check :	0	
signed flag :	0	
Overflow flag :	0	
Zero Flag :	0	
address memory error :	x	
instruction invalid address :	x	
status of memory :	x	
new pc address :		352
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Address flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
TIME INSTANT :		149
clk :	0	
Memory invalid check :	0	
PC Adress :		352
Instrction code :	0111	
Instruction invalid Check :	0	
Function code :	0001	
Need for Val_C :	1	

[illegible]

register A : 0110

PROGRAM REGISTER VALUES:

Halt Flag : 0


```
Value_A : x
Value_B : 256
```

Instruction code flag : 0

PROGRAM REGISTER VALUES:

99

```

rsp :          256
rbp :          32
rsi :          64
rdi :          71
r8 :           64
r9 :          512
r10 :         1024
r11 :         2048
r12 :         4096
r13 :         8192
r14 :        16384

```

```

Value_A :          x
Value_B :         256

```

```

Value_E :         192
Value_M :          64

```

```
No. of valid instructions :          300
```

```
Condition satisfy check : 0
```

```
signed flag : 0
```

```
Overflow flag : 0
```

```
Zero Flag : 0
```

```
address memory error : x
```

```
instruction invalid address : x
```

```
status of memory : x
```

```
new pc address :          352
```

```
STATUS FLAGS : 
```

```
ALL OK FLAG : 1
```

```
Memory Address flag : 0
```

```
Halt Flag : 0
```

```
Instruction code flag : 0
```

```
Memory Status : Address of next unstruction pushed to memory
```

```
TIME INSTANT :          159
```

```
clk : 1
```

```
Memory invalid check : 0
```

```
PC Address :          352
```

```
Instruction code : 1000
```

```
Instruction invalid Check : 0
```

```
Function code : 0000
```

```
Need for Val_C : 1
```

[illegible]

register A : 0110

PROGRAM REGISTER VALUES:

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 160

```
clk : 0
```

```
Memory invalid check : 0
```

PC Address : 352

Instruction code : 1000

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 1

Need for registers : 0

[illegible]

Val P = 424

register A : 0110

```

register B : 0111

```

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx : 2

$$\text{rdx} : 4$$

rbx : 8

rsp : 256

rbp : 32

rsi : 64

rdi : 71

r8 : 64

r9 : 512

```
r10      :      1024
```

r11	:	2048
-----	---	------

r12	:	4096
-----	---	------

r13 : 8192

r14 : 16384

Value_A : x

Value_B : 256

Value_E : 192

Value_M : 64

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

```

Overflow flag : 0
Zero Flag : 0
address memory error : 0
instruction invalid address : x
status of memory : 1
new pc address :
-----STATUS FLAGS : -----
ALL OK FLAG : 1
Memory Address flag : 0
Halt Flag : 0
Instruction code flag : 0

```

TIME INSTANT : 162

```
clk : 0
```

Memory invalid check : 0

PC Address : 352

Instruction code : 1000

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 1

Need for registers : 0

[illegible]

Val P = 424

register A : 0110

```

register B : 0111

```

PROGRAM REGISTER VALUES:

```

rax    :    1
rcx    :    2
rdx    :    4
rbx    :    8
rsp    :   192
rbp    :   32
rsi    :   64
rdi    :   71
r8     :   64
r9     :  512
r10    : 1024
r11    : 2048
r12    : 4096
r13    : 8192

```

```
Value_A : x
Value_B : 256
```

Instruction code flag : 0

```

register A : 0110
register B : 0111

```

```

rax      :      1
rcx      :      2
rdx      :      4
rbx      :      8

```


rsp :	192	
rbp :	32	
rsi :	64	
rdi :	71	
r8 :	64	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	x	
Value_B :	256	
<hr/>		
Value_E :	192	
Value_M :	64	
No. of valid instructions :		300
Condition satisfy check :	0	
signed flag :	0	
Overflow flag :	0	
Zero Flag :	0	
address memory error :	0	
instruction invalid address :	x	
status of memory :	1	
new pc address :		440
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Address flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
TIME INSTANT :		169
clk :	0	
Memory invalid check :	0	
PC Address :		440
Instruction code :	1000	
Instruction invalid Check :	0	
Function code :	0000	
Need for Val_C :	1	
Need for registers :	0	

rbp :	32	
rsi :	64	
rdi :	71	
r8 :	64	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	

Value_A :	512	
Value_B :	192	

Value_E :	128	
Value_M :	64	
No. of valid instructions :		300
Condition satisfy check :	0	
signed flag :	0	
Overflow flag :	0	
Zero Flag :	0	
address memory error :	x	
instruction invalid address :	x	
status of memory :	x	
new pc address :		440

STATUS FLAGS : ————

ALL OK FLAG :	1
Memory Address flag :	0
Halt Flag :	0
Instruction code flag :	0

Memory Status : Address of pushed data instruction pushed to memory

TIME INSTANT :	179
clk :	1
Memory invalid check :	0
PC Address :	440
Instruction code :	1010
Instruction invalid Check :	0
Function code :	0000
Need for Val_C :	0
Need for registers :	1


```

Zero Flag : 0
address memory error : 0
instruction invalid address : x
status of memory : 1
new pc address : 440
-----STATUS FLAGS : -----

```

TIME INSTANT : 182

```
Instruction code : 1010
Instruction invalid Check : 0
```

[illegible]

PROGRAM REGISTER VALUES:

rbp :	32
rsi :	64
rdi :	71
r8 :	64
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

Value_E :	128
Value_M :	64

Condition satisfy check : 0

Overflow flag : 0

```
address memory error : 0
```

```
status of memory : 1
```

————STATUS FLAGS : ————

Memory Address flag : 0

Instruction code flag : 0

TIME INSTANT : 189

Memory invalid check : 0

Instruction code : 1010

Function code : 0000

Need for registers : 1

[illegible]

Val P = 456

register A : 1001

register B : 1111

PROGRAM REGISTER VALUES:

rax	:	1
rcx	:	2
rdx	:	4
rbx	:	8
rsp	:	128
rbp	:	32
rsi	:	64
rdi	:	71
r8	:	64
r9	:	512
r10	:	1024
r11	:	2048
r12	:	4096
r13	:	8192
r14	:	16384

Value_A : 512

Value_B : 192

Value_E : 128

Value_M : 64

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

address memory error : 0

instruction invalid address : x

status of memory : 1

new pc address : 456

STATUS FLAGS : _____

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0


```
Value_A : 128
Value_B : 128
```

```
Value_E : x
Value_M : 64
```

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

```
address memory error : x
```

```
instruction invalid adress : x
```

```
status of memory : x
```

```
new pc adress : 456
```

————STATUS FLAGS : ————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 198

clk : 1

Memory invalid check : 0

PC Address : 456

Instruction code : 1011

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 0

Need for registers : 1

[illegible]

Val P = 472

register A : 0111

```

      0
register B : 1111

```

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx : 2

rdx : 4

rbx : 8

```
rsp    : 128
```

rbp : 32

rsi :	64	
rdi :	71	
r8 :	64	
r9 :	512	
r10 :	1024	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	

Value_A :	128	
Value_B :	128	

Value_E :	192	
Value_M :	64	
No. of valid instructions :		300
Condition satisfy check :	0	
signed flag :	0	
Overflow flag :	0	
Zero Flag :	0	
address memory error :	x	
instruction invalid address :	x	
status of memory :	x	
new pc adress :		456

————STATUS FLAGS : ————

ALL OK FLAG :	1
Memory Adress flag :	0
Halt Flag :	0
Instruction code flag :	0

———— Memory Status : Data extracted from the memory ————

————Valid data taken from memory————

TIME INSTANT :	199
clk :	1
Memory invalid check :	0
PC Adress :	456
Instrection code :	1011
Instruction invalid Check :	0
Function code :	0000
Need for Val_C :	0
Need for registers :	1

[illegible]

```

Zero Flag : 0
address memory error : 0
instruction invalid address : 0
status of memory : 1
new pc address : 456
-----STATUS FLAGS : -----

```

TIME INSTANT : 202

```
Instruction code : 1011
Instruction invalid Check : 0
```

[illegible]

PROGRAM REGISTER VALUES:

rbp :	32
rsi :	64
rdi :	512
r8 :	64
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

Value_E :	192
Value_M :	512

Condition satisfy check : 0

Overflow flag : 0

```
address memory error : 0
```

status of memory : 1

————STATUS FLAGS : —————

Memory Address flag : 0

Instruction code flag : 0

```
clk : 0
```

PC Address : 472

Instruction invalid Check : 0

Need for Val_C : 0

[illegible]

Val P = 472

register A : 0111

register B : 1111

PROGRAM REGISTER VALUES:

rax :	1
rcx :	2
rdx :	4
rbx :	8
rsp :	192
rbp :	32
rsi :	64
rdi :	512
r8 :	64
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

Value_A : 128

Value_B : 128

Value_E : 192

Value_M : 512

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

address memory error : 0

instruction invalid address : 0

status of memory : 1

new pc address : 472

——STATUS FLAGS : ——

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

[illegible]


```
Value_A : 192
Value_B : 192
```

```
Value_E : x
Value_M : 512
```

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

```
address memory error : x
```

```
instruction invalid adress : x
```

```
status of memory : x
```

```
new pc adress : 472
```

————STATUS FLAGS : ————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 218

clk : 1

Memory invalid check : 0

PC Address : 472

Instruction code : 1001

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 0

Need for registers : 0

[illegible]

Val P = 472

register A : 0111

register B : 1111

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx : 2

rdx : 4

rbx : 8

rsp : 192

rbp : 32

```

rsi :          64
rdi :         512
r8  :          64
r9  :         512
r10 :         1024
r11 :         2048
r12 :         4096
r13 :         8192
r14 :        16384

```

Value_E :	256
Value_M :	512

Condition satisfy check : 0

Overflow flag : 0

```
address memory error : x
```

```
status of memory : x
```

STATUS FLAGS : _____

Memory Address flag : 0

Instruction code flag : 0

TIME INSTANT : 219

Memory invalid check : 0

Instruction code : 1001

Function code : 0000

Need for registers : 0

[illegible]

Val P = 472

register A : 0111

register B : 1111

PROGRAM REGISTER VALUES:

rax :	1
rcx :	2
rdx :	4
rbx :	8
rsp :	192
rbp :	32
rsi :	64
rdi :	512
r8 :	64
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

Value_A : 192

Value_B : 192

Value_E : 256

Value_M : 424

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

address memory error : 0

instruction invalid address : x

status of memory : x

new pc address : 472

————STATUS FLAGS : ————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

[illegible]


```
Value_A : 192
Value_B : 192
```

Value_E	:	256
Value_M	:	424

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

```
address memory error : 0
```

```
instruction invalid adress : x
```

```
status of memory : x
```

```
new pc adress : 472
```

————STATUS FLAGS : ————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 223

```
clk : 0
```

Memory invalid check : 0

PC Address : 472

Instruction code : 1001

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 0

Need for registers : 0

[illegible]

Val P = 472

register A : 0111

register B : 1111

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx : 2

rdx : 4

rbx : 8

```
rsp    : 256
```

rbp : 32

```

rsi :          64
rdi :         512
r8  :          64
r9  :         512
r10 :         1024
r11 :         2048
r12 :         4096
r13 :         8192
r14 :        16384

```

```
Value_A : 192
Value_B : 192
```

Value_E :	256
Value_M :	424

No. of valid instructions : 300

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

```
address memory error : 0
```

```
instruction invalid adress : x
```

```
status of memory : x
```

```
new pc address : 424
```

————STATUS FLAGS : —————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 229

```
clk : 0
```

Memory invalid check : 0

PC Address : 424

Instruction code : 1001

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 0

Need for registers : 0

[illegible]

Val P = 472

register A : 0111
 register B : 1111
 PROGRAM REGISTER VALUES:

rax :	1
rcx :	2
rdx :	4
rbx :	8
rsp :	256
rbp :	32
rsi :	64
rdi :	512
r8 :	64
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

Value_A :	192
Value_B :	192

Value_E :	256
Value_M :	424

No. of valid instructions :	300
-----------------------------	-----

Condition satisfy check : 0

signed flag : 0

Overflow flag : 0

Zero Flag : 0

address memory error : 0

instruction invalid adress : x

status of memory : x

new pc adress :	424
-----------------	-----

STATUS FLAGS :

ALL OK FLAG : 1

Memory Adress flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT :	230
----------------	-----

0

X

424

300

0

0

0

0

X

X

X

424

STATUS FLAGS :

1

0

0

0

238

1

0

424

0

0

10

0

1

01101110

440

0

0

 $S:$

1

2

1

3

256

32

64

r di :	512
r8 :	64
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

```
Value_A : 4
Value_B : 0
```

Value_E	:	4
Value_M	:	424

No. of valid instructions : 300

Condition satisfy check : 1

signed flag : 0

Overflow flag : 0

Zero Flag : 0

```
address memory error : x
```

```
instruction invalid adress : x
```

```
status of memory : x
```

```
new pc address : 424
```

————STATUS FLAGS : ————

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 240

$$\text{clk} : 0$$

Memory invalid check : 0

PC Address : 424

Instruction code : 0010

Instruction invalid Check : 0

Function code : 0110

Need for Val_C : 0

Need for registers : 1

Val P = 440

```

register A : 0010

```

register B : 1010

PROGRAM REGISTER VALUES:

rax :	1
rcx :	2
rdx :	4
rbx :	8
rsp :	256
rbp :	32
rsi :	64
rdi :	512
r8 :	64
r9 :	512
r10 :	1024
r11 :	2048
r12 :	4096
r13 :	8192
r14 :	16384

Value_A :	4
Value_B :	0

Value_E :	4
Value_M :	424

No. of valid instructions : 300

Condition satisfy check : 1

signed flag : 0

Overflow flag : 0

Zero Flag : 0

address memory error : x

instruction invalid address : x

status of memory : x

new pc address : 424

——STATUS FLAGS : ——

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 242

clk : 0


```
Value_A : 4
Value_B : 0
```

Instruction code flag : 0

```

      8
register B : 1111

```

PROGRAM REGISTER VALUES:

rax :	1	
rcx :	2	
rdx :	4	
rbx :	8	
rsp :	256	
rbp :	32	
rsi :	64	
rdi :	512	
r8 :	64	
r9 :	512	
r10 :	4	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	
<hr/>		
Value_A :	x	
Value_B :	x	
<hr/>		
Value_E :	x	
Value_M :	424	
No. of valid instructions :		300
Condition satisfy check :	1	
signed flag :	0	
Overflow flag :	0	
Zero Flag :	0	
address memory error :	x	
instruction invalid address :	x	
status of memory :	x	
new pc address :		440
<hr/>		
STATUS FLAGS : <hr/>		
ALL OK FLAG :	1	
Memory Address flag :	0	
Halt Flag :	0	
Instruction code flag :	0	
<hr/>		
TIME INSTANT :		251
clk :	1	
Memory invalid check :	0	


```
new pc adress : 440
```

ALL OK FLAG : 1

Memory Address flag : 0

Halt Flag : 0

Instruction code flag : 0

TIME INSTANT : 258

$$\text{clk} : 1$$

Memory invalid check : 0

PC Address : 440

Instruction code : 1010

Instruction invalid Check : 0

Function code : 0000

Need for Val_C : 0

Need for registers : 1

[illegible]

Val P = 456

register A : 1001

register B : 1111

PROGRAM REGISTER VALUES:

```
rax    :                               1
```

rcx : 2

rdx : 4

rbx : 8

rsp : 256

rbp : 32

rsi : 64

rdi : 512

r8 : 64

r9 : 512

r10 : 4

```

r11      :      2048

```

r12 : 4096

r13	:	8192
-----	---	------

r14	:	16384
-----	---	-------

Value_A : 512

Value_B :	256
-----------	-----

```

Value_E : 192
Value_M : 424
No. of valid instructions : 300
Condition satisfy check : 1
signed flag : 0
Overflow flag : 0
Zero Flag : 0
address memory error : x
instruction invalid address : x
status of memory : x
new pc address : 440
-----STATUS FLAGS : -----
ALL OK FLAG : 1
Memory Address flag : 0
Halt Flag : 0
Instruction code flag : 0

```

[illegible]

```

rax   :      1
rcx   :      2
rdx   :      4
rbx   :      8
rsp   :    256
rbp   :     32
rsi   :     64

```

rdi :	512	
r8 :	64	
r9 :	512	
r10 :	4	
r11 :	2048	
r12 :	4096	
r13 :	8192	
r14 :	16384	

Value_A :	512	
Value_B :	256	

Value_E :	192	
Value_M :	424	
No. of valid instructions :		300
Condition satisfy check :	1	
signed flag :	0	
Overflow flag :	0	
Zero Flag :	0	
address memory error :	0	
instruction invalid adress :	x	
status of memory :	x	
new pc adress :		440
——STATUS FLAGS : ——		
ALL OK FLAG :	1	
Memory Adress flag :	0	
Halt Flag :	0	
Instruction code flag :	0	