**ET3206: Digital Design**

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**Div: D Batch: D1**

**Date of performance: 19 / 01 / 2023**

**Experiment No.2**

**Title: Transient and DC analysis of CMOS inverter using SPICE**

**Description : CMOS Inverter DC analysis for varying threshold voltage and W/L ratio and Transient analysis for pulse input**

**Aim:** To understand the ngspice coding conventions for active and passive devices, voltage sources

**Learning objectives:**

1. To understand how to write NGSPICE code for a subcircuit.

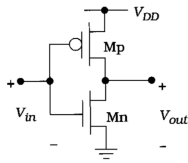
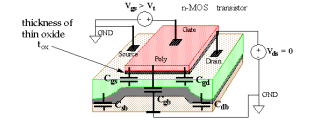
2. To demonstrate transient analysis of CMOS inverter circuit.

**Software used:** NGSPICE 28

**Theory:**

*Explain the effect of change in Width on the transfer curve*

**Circuit Diagram:**

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**Circuit Diagram**

(Circuit diagram with 4 terminal MOS and Labeled nodes )

**Part 1: DC Analysis of CMOS Inverter**

**Spice code: Voltage Transfer Curve analysis**

\*cmos invertor

.model n nmos vto=1.4v

.model p pmos vto=-1.4v

vdd 4 0 dc 5v

vin 1 0 dc 5v

vd 4 2 dc 0v

m1 3 1 0 0 n

m2 3 1 2 2 p

.dc vin 0 5 0.1

.control

run

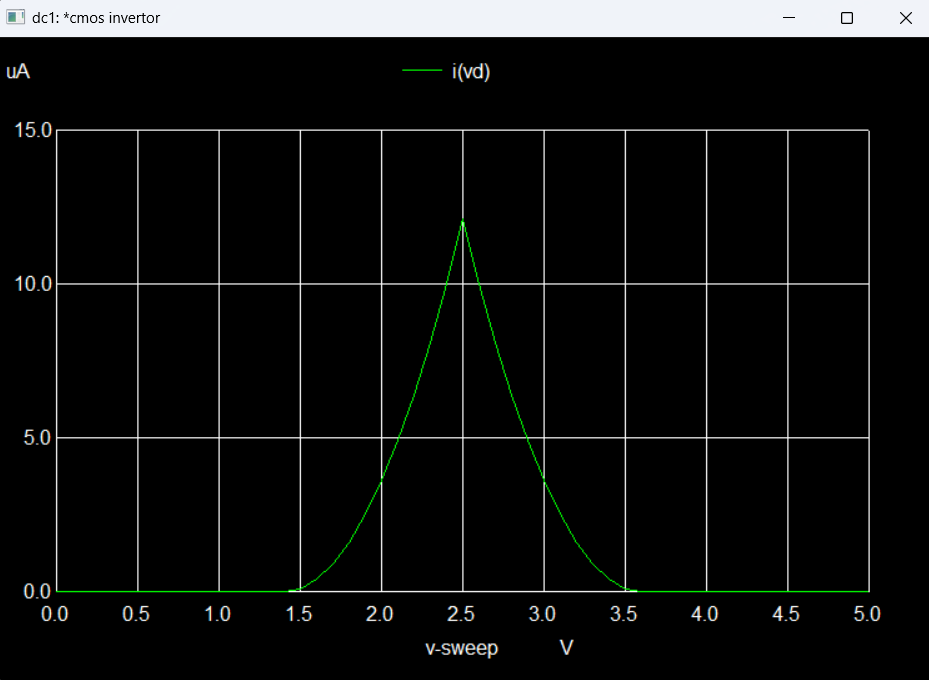
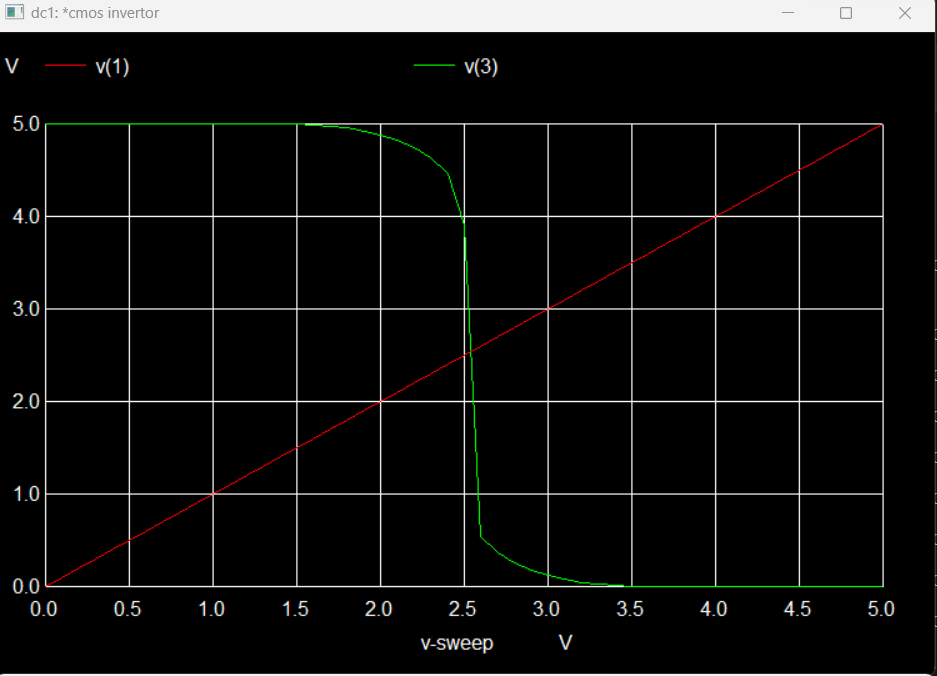
plot v(3) v(1)

plot i(vd)

.endc

.end

**When Vth = 1.4 V**

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**When Vth = 1.5 V**

\*cmos invertor

.model n nmos vto=1.5 v

.model p pmos vto=-1.5 v

vdd 4 0 dc 5v

vin 1 0 dc 5v

vd 4 2 dc 0v

m1 3 1 0 0 n

m2 3 1 2 2 p

.dc vin 0 5 0.1

.control

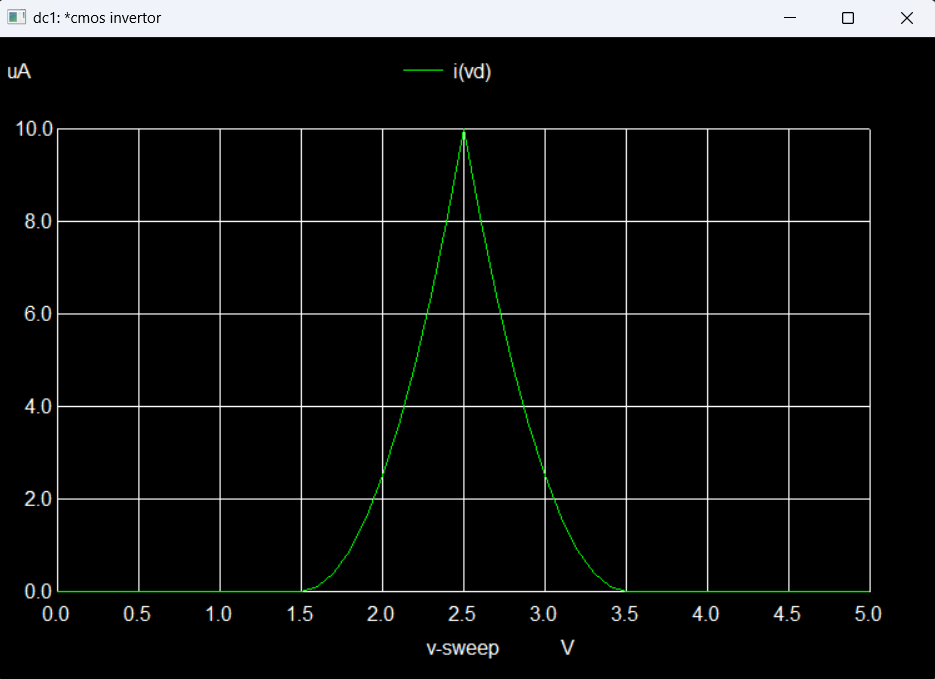
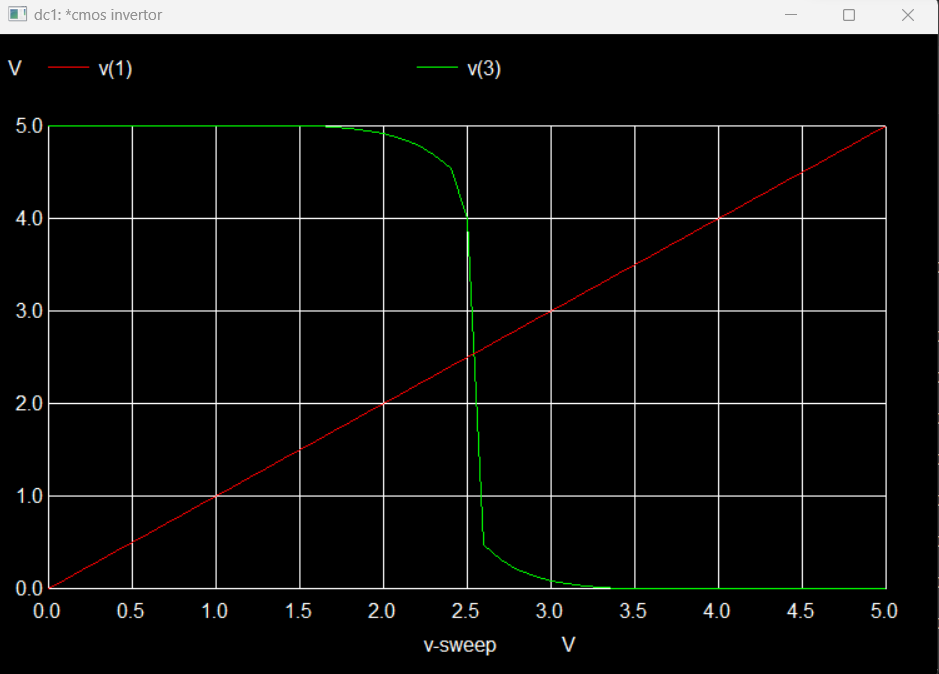
run

plot v(3) v(1)

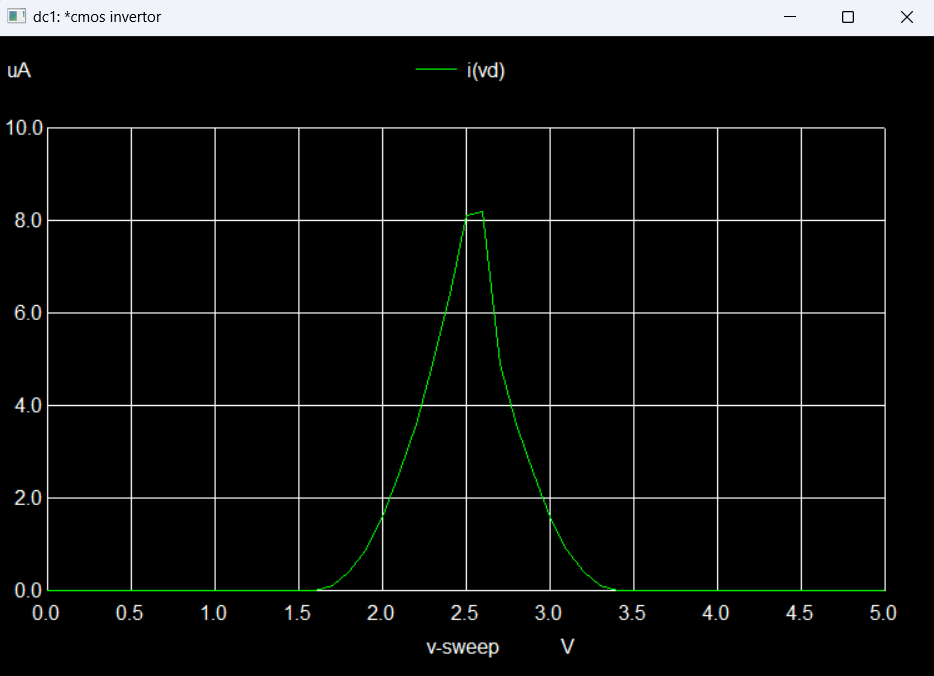
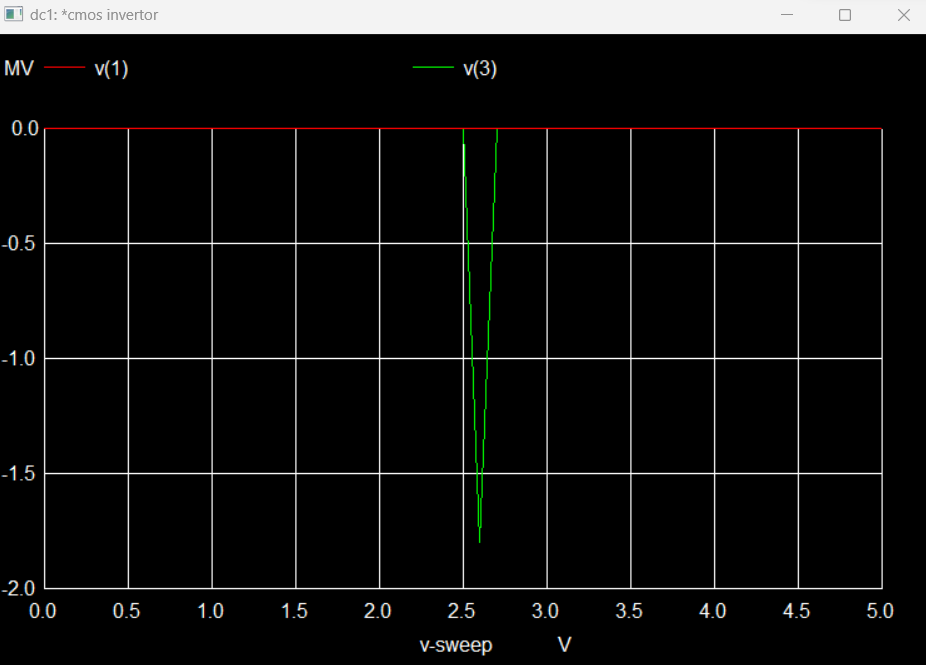
plot i(vd)

.endc

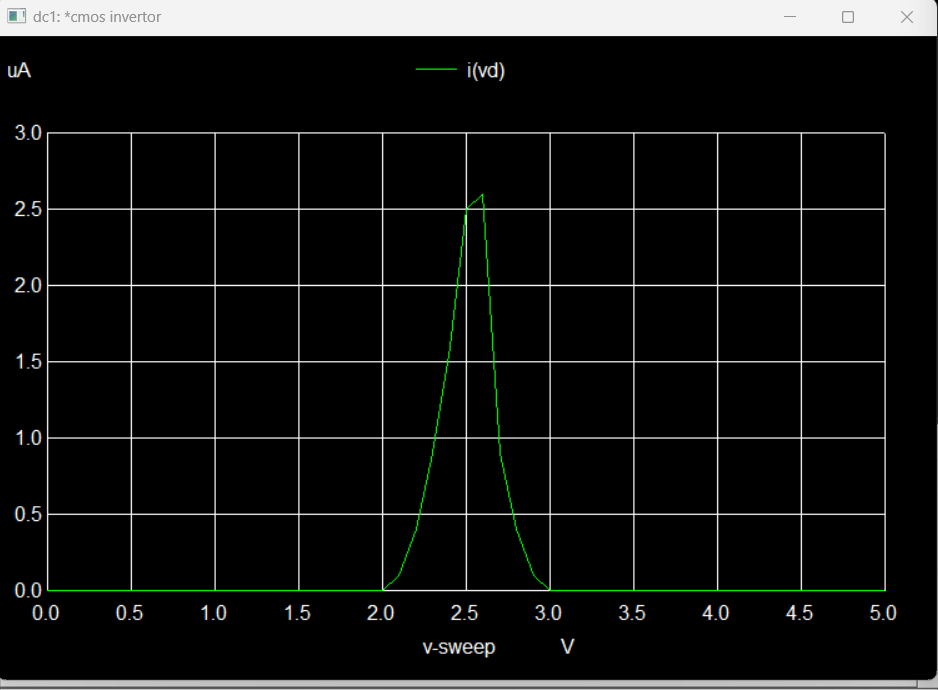
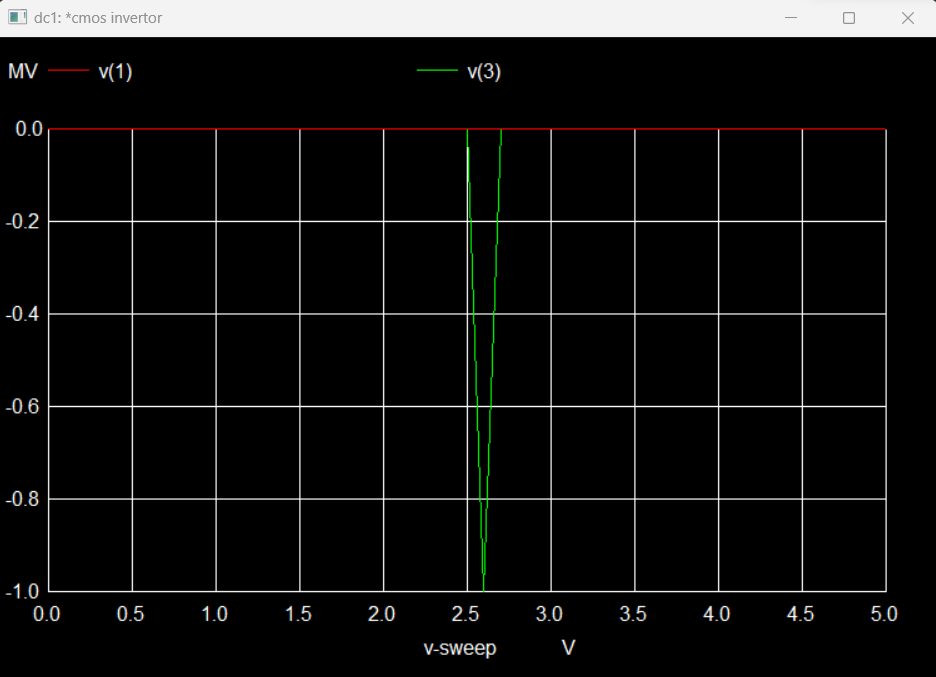
.end

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**When Vth = 1.8 V**

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**When Vth = 2V**

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**CMOS Characteristics Varying W/L ratio**

\*cmos invertor

.model n nmos vto=1.2v

.model p pmos vto=-1.2v

vdd 4 0 dc 5v

vin 1 0 dc 5v

vd 4 2 dc 0v

m1 3 1 0 0 n

m2 3 1 2 2 p L= 1.8U W=0.09U

.dc vin 0 5 0.1 L=0.18U W=0.09U

.control

run

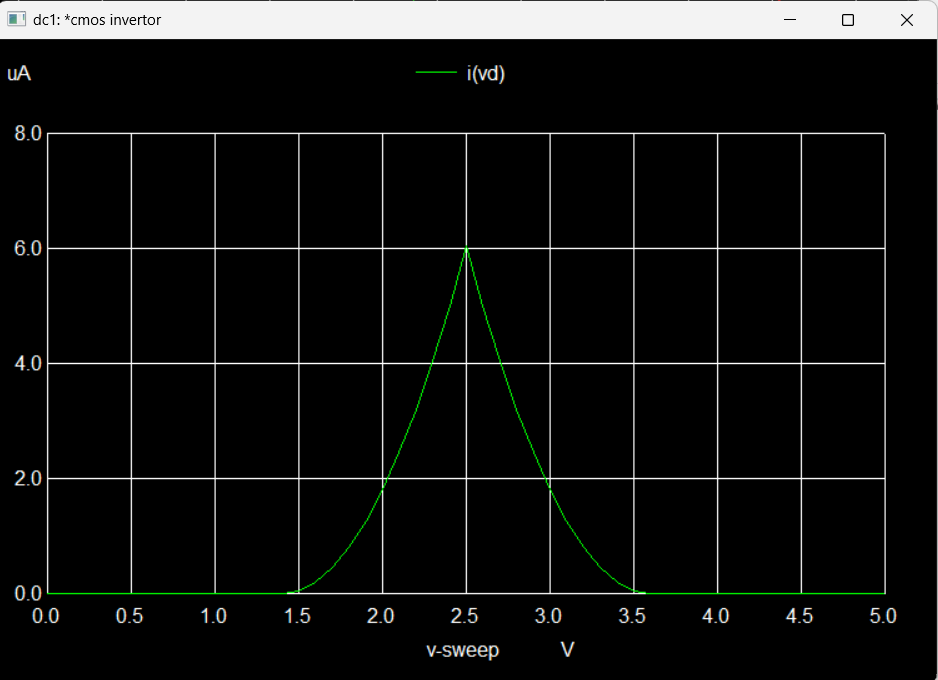
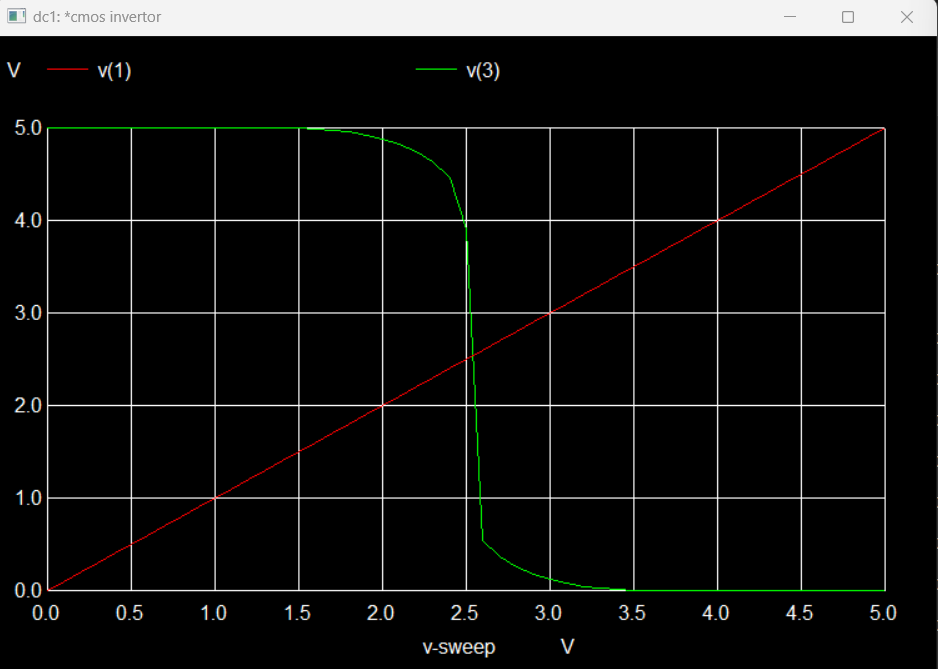
plot v(3) v(1)

plot i(vd)

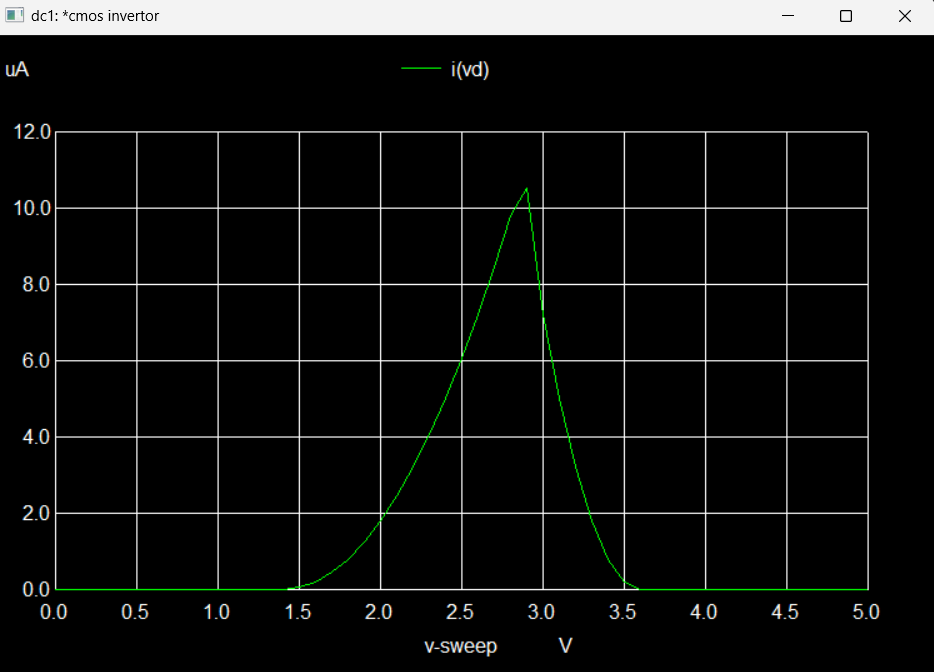
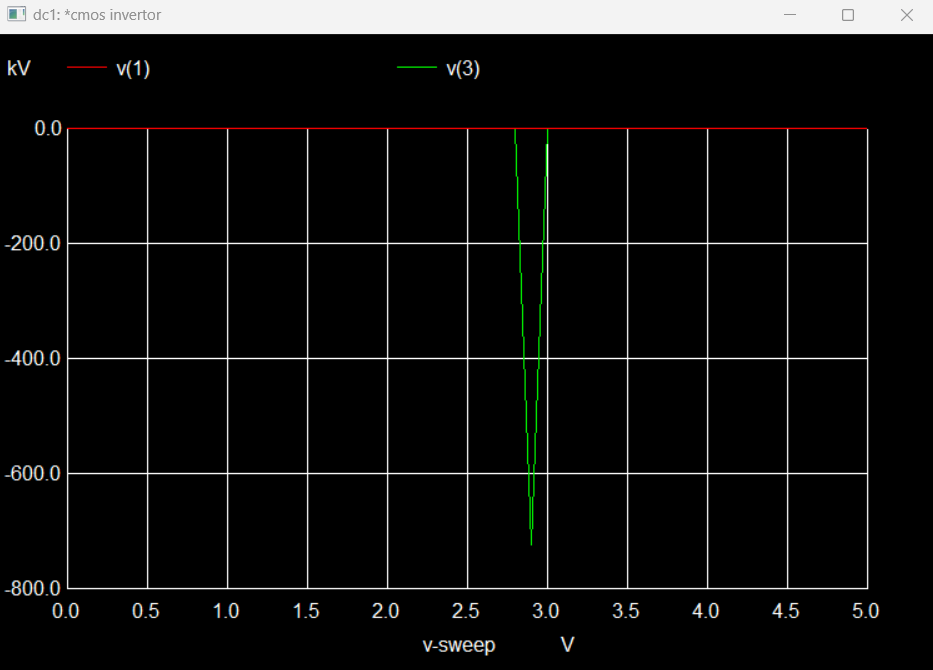
.endc

.end

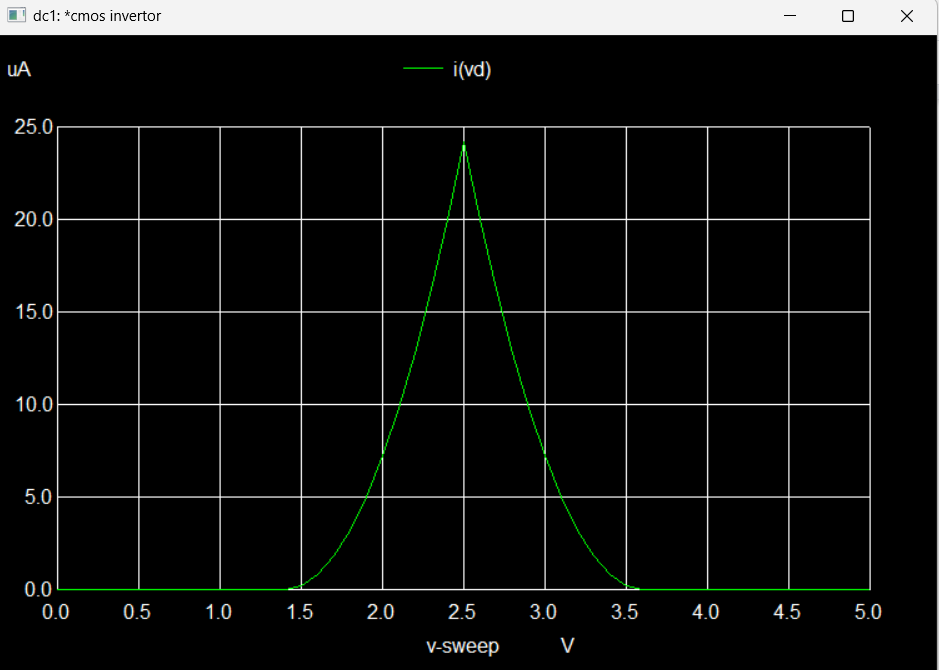
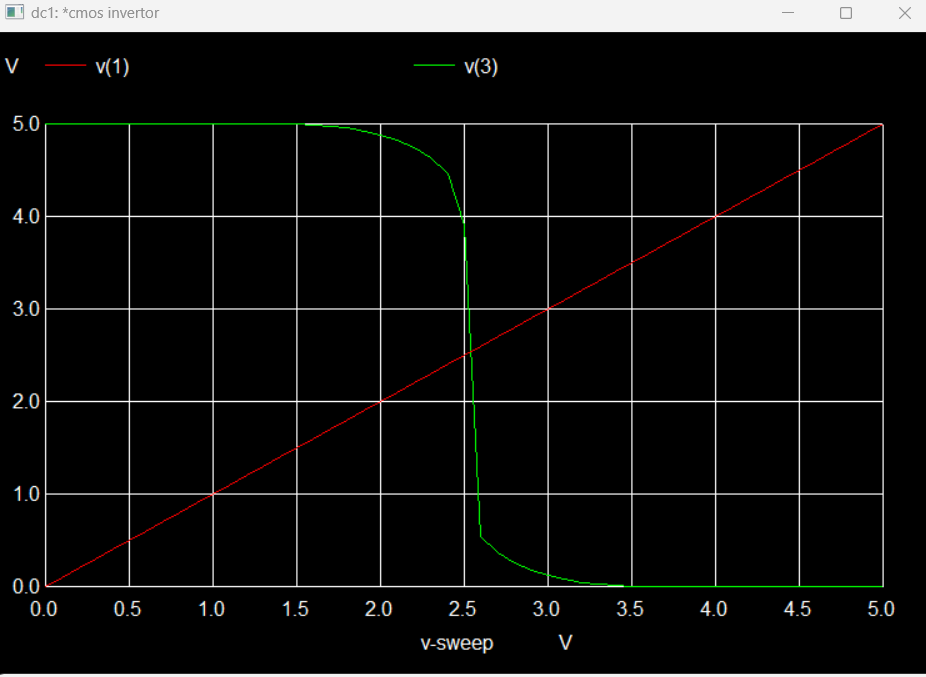
**When n L=0.18U W=0.09U p L=0.18U W=0.09U**

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**When n L=0.18U W=0.09U p L=0.09U W=0.18U**

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**When n L=0.09U W=0.18U p L=0.18U W=0.09U**

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**Part 2: Transient Analysis of CMOS Inverter**

\*cmos invertor

.model n nmos

.model p pmos

vdd 4 0 dc 5v

\*vin 1 0 dc 5v

vd 4 2 dc 0v

m1 3 1 0 0 n

m2 3 1 2 2 p

Vin 1 0 pulse(0 5 0 0.5ns 0.5ns 5ns 10ns)

.tran 0.01ns 50ns

\*.dc vin 0 5 0.1

.control

run

set color0=black

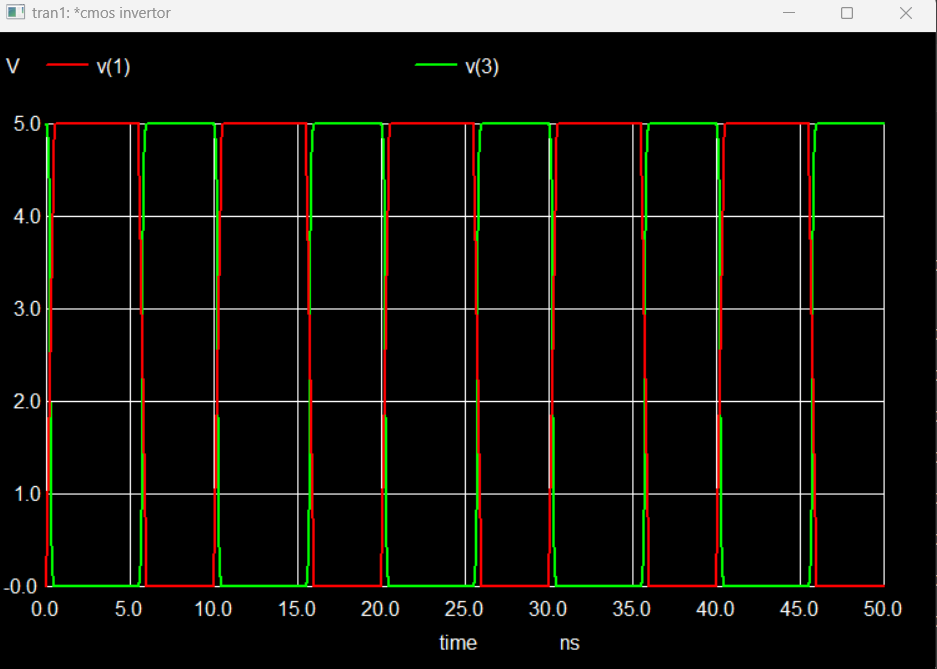
set xbrushwidth=2

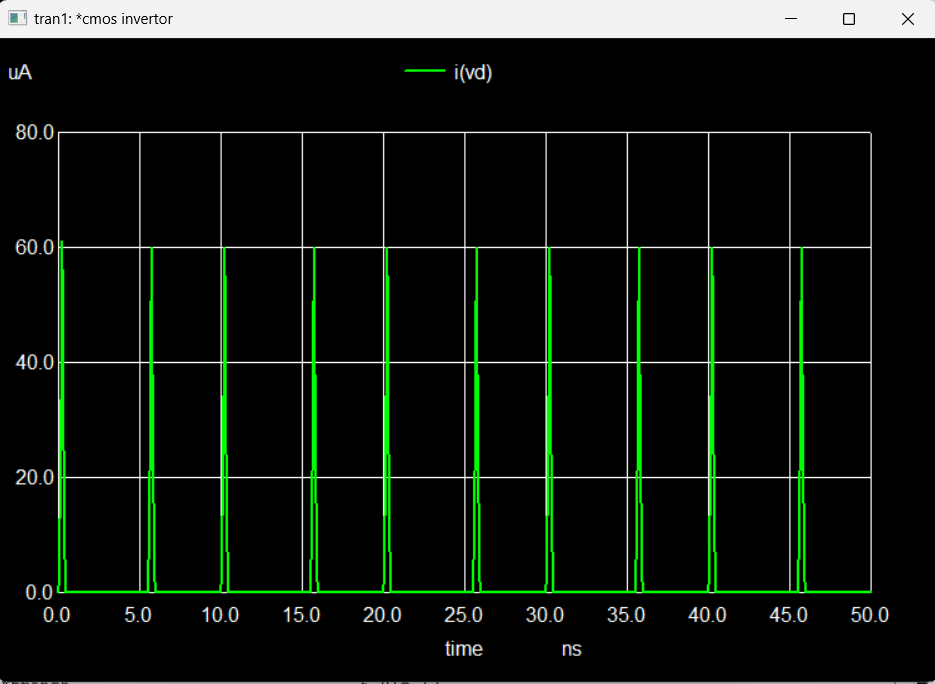
plot v(3) v(1)

plot i(vd)

.endc

.end

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**Conclusions:**

1. After plotting the graphs of different threshold voltages the peak value of i(vd) decreases.

|  |  |
| --- | --- |
| Threshold Voltage | Peak value |
| 1.4 | 12V |
| 1.5 | 10V |
| 1.8 | 8.2V |

1. As the length of p mos is increased the peak of i(vd) decreases.
2. As the length of p mos is decreases the peak of i(vd) increases by nearly 2x. The slop of graph was seen to be decrease than previous graph.