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Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.71 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.74 secs

--> Reading design: traffic_light.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "traffic_light.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "traffic_light"
Output Format                      : NGC
Target Device                      : xc3s400-5-pq208

---- Source Options
Top Module Name                    : traffic_light
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : Yes
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
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ROM Style                          : Auto
Mux Extraction                     : Yes
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : Auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 8
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Yes
Use Synchronous Set                : Yes
Use Synchronous Reset              : Yes
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
Verilog 2001                       : YES
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                           HDL Compilation                             *
=========================================================================
Compiling verilog file "traffic.v" in library work
Module <traffic_light> compiled
No errors in compilation
Analysis of file <"traffic_light.prj"> succeeded.


=========================================================================
*                     Design Hierarchy Analysis                         *
=========================================================================
Analyzing hierarchy for module <traffic_light> in library <work> with parameters.
        HGRE_FRED = "00"
        HRED_FGRE = "10"
        HRED_FYEL = "11"
        HYEL_FRED = "01"
```

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=========================================================================
*                            HDL Analysis                               *
=========================================================================
Analyzing top module <traffic_light>.
        HGRE_FRED = 2'b00
        HRED_FGRE = 2'b10
        HRED_FYEL = 2'b11
        HYEL_FRED = 2'b01
Module <traffic_light> is correct for synthesis.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <traffic_light>.
    Related source file is "traffic.v".
INFO:Xst:2117 - HDL ADVISOR - Mux Selector <state> of Case statement line 26 was
re-encoded using one-hot encoding. The case statement will be optimized (default statement
optimization), but this optimization may lead to design initialization problems. To ensure
the design works safely, you can:
        - add an 'INIT' attribute on signal <state> (optimization is then done without any
risk)
        - use the attribute 'signal_encoding user' to avoid onehot optimization
        - use the attribute 'safe_implementation yes' to force XST to perform a safe (but
less efficient) optimization
    Found finite state machine <FSM_0> for signal <state>.
    -----------------------------------------------------------------------
    | States             | 4                                              |
    | Transitions        | 8                                              |
    | Inputs             | 4                                              |
    | Outputs            | 6                                              |
    | Clock              | clk                       (rising_edge)        |
    | Reset              | rst_n                     (negative)           |
    | Reset type         | asynchronous                                   |
    | Reset State        | 00                                             |
    | Encoding           | automatic                                      |
    | Implementation     | LUT                                            |
    -----------------------------------------------------------------------
    Found 28-bit up counter for signal <count>.
    Found 28-bit up counter for signal <count_delay>.
    Found 1-bit register for signal <delay10s>.
    Found 1-bit register for signal <delay3s1>.
    Found 1-bit register for signal <delay3s2>.
    Summary:
        inferred   1 Finite State Machine(s).
        inferred   2 Counter(s).
        inferred   3 D-type flip-flop(s).
Unit <traffic_light> synthesized.


=========================================================================
HDL Synthesis Report

Macro Statistics
# Counters                                             : 2
 28-bit up counter                                     : 2
# Registers                                            : 3
 1-bit register                                        : 3
```

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=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================

Analyzing FSM <FSM_0> for best encoding.
Optimizing FSM <state/FSM> on signal <state[1:2]> with gray encoding.
-------------------
 State | Encoding
-------------------
 00    | 00
 01    | 01
 10    | 11
 11    | 10
-------------------

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# FSMs                                                 : 1
# Counters                                             : 2
 28-bit up counter                                     : 2
# Registers                                            : 3
 Flip-Flops                                            : 3

=========================================================================

=========================================================================
*                       Low Level Synthesis                             *
=========================================================================

Optimizing unit <traffic_light> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block traffic_light, actual ratio is 1.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 61
 Flip-Flops                                            : 61

=========================================================================

=========================================================================
*                         Partition Report                              *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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```

```
================================================================================
*                            Final Report                                      *
================================================================================
Final Results
RTL Top Level Output File Name     : traffic_light.ngr
Top Level Output File Name         : traffic_light
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 9

Cell Usage :
# BELS                             : 212
#      GND                         : 1
#      INV                         : 5
#      LUT1                        : 54
#      LUT2                        : 6
#      LUT3                        : 2
#      LUT4                        : 18
#      LUT4_D                      : 1
#      MUXCY                       : 68
#      VCC                         : 1
#      XORCY                       : 56
# FlipFlops/Latches                : 61
#      FDC                         : 2
#      FDE                         : 3
#      FDR                         : 28
#      FDRE                        : 28
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 8
#      IBUF                        : 2
#      OBUF                        : 6
================================================================================

Device utilization summary:
---------------------------

Selected Device : 3s400pq208-5

 Number of Slices:                       44  out of   3584     1%
 Number of Slice Flip Flops:             61  out of   7168     0%
 Number of 4 input LUTs:                 86  out of   7168     1%
 Number of IOs:                           9
 Number of bonded IOBs:                   9  out of    141     6%
 Number of GCLKs:                         1  out of      8    12%

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Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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================================================================================
TIMING REPORT
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```
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 61    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------------------------+------------------------+-------+
Control Signal                                       | Buffer(FF name)        | Load  |
-----------------------------------------------------+------------------------+-------+
state_FSM_Acst_FSM_inv(state_FSM_Acst_FSM_inv1_INV_0:O)| NONE(state_FSM_FFd1)   | 2     |
-----------------------------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 8.044ns (Maximum Frequency: 124.324MHz)
   Minimum input arrival time before clock: 2.221ns
   Maximum output required time after clock: 8.027ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 8.044ns (frequency: 124.324MHz)
  Total number of paths / destination ports: 5141 / 148
-------------------------------------------------------------------------
Delay:               8.044ns (Levels of Logic = 9)
  Source:            count_delay_17 (FF)
  Destination:       count_delay_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: count_delay_17 to count_delay_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             2   0.626   1.040  count_delay_17 (count_delay_17)
     LUT4:I0->O            1   0.479   0.000  delay10s_and00001_wg_lut<1>
(delay10s_and00001_wg_lut<1>)
     MUXCY:S->O            1   0.435   0.000  delay10s_and00001_wg_cy<1>
(delay10s_and00001_wg_cy<1>)
     MUXCY:CI->O           1   0.056   0.000  delay10s_and00001_wg_cy<2>
(delay10s_and00001_wg_cy<2>)
     MUXCY:CI->O           1   0.056   0.000  delay10s_and00001_wg_cy<3>
(delay10s_and00001_wg_cy<3>)
     MUXCY:CI->O           1   0.056   0.000  delay10s_and00001_wg_cy<4>
(delay10s_and00001_wg_cy<4>)
     MUXCY:CI->O           1   0.056   0.000  delay10s_and00001_wg_cy<5>
```

```
(delay10s_and00001_wg_cy<5>)
     MUXCY:CI->O           2   0.265   0.768  delay10s_and00001_wg_cy<6>
(delay10s_and00001_wg_cy<6>)
     LUT4:I3->O            4   0.479   0.802  delay10s_and0000 (delay10s_and0000)
     LUT4:I3->O           28   0.479   1.556  count_delay_and0000 (count_delay_and0000)
     FDRE:R                    0.892          count_delay_0
    ----------------------------------------
    Total                      8.044ns (3.877ns logic, 4.167ns route)
                                       (48.2% logic, 51.8% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              2.221ns (Levels of Logic = 2)
  Source:            C (PAD)
  Destination:       state_FSM_FFd2 (FF)
  Destination Clock: clk rising

  Data Path: C to state_FSM_FFd2
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   0.715   0.851  C_IBUF (C_IBUF)
     LUT4:I1->O            1   0.479   0.000  state_FSM_FFd2-In1 (state_FSM_FFd2-In)
     FDC:D                     0.176          state_FSM_FFd2
    ----------------------------------------
    Total                      2.221ns (1.370ns logic, 0.851ns route)
                                       (61.7% logic, 38.3% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 10 / 6
-------------------------------------------------------------------------
Offset:              8.027ns (Levels of Logic = 2)
  Source:            state_FSM_FFd1 (FF)
  Destination:       light_highway<1> (PAD)
  Source Clock:      clk rising

  Data Path: state_FSM_FFd1 to light_highway<1>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             11   0.626   1.267  state_FSM_FFd1 (state_FSM_FFd1)
     LUT2:I0->O            2   0.479   0.745  state_FSM_Out11 (light_highway_1_OBUF)
     OBUF:I->O                 4.909          light_highway_1_OBUF (light_highway<1>)
    ----------------------------------------
    Total                      8.027ns (6.014ns logic, 2.013ns route)
                                       (74.9% logic, 25.1% route)

=========================================================================


Total REAL time to Xst completion: 13.00 secs
Total CPU time to Xst completion: 13.24 secs

-->

Total memory usage is 4521500 kilobytes

Number of errors   :    0 (   0 filtered)
```

```
Number of warnings :    0 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```