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Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.19 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.19 secs

--> Reading design: fifo_memory.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "fifo_memory.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "fifo_memory"
Output Format                      : NGC
Target Device                      : xc3s400-5-pq208

---- Source Options
Top Module Name                    : fifo_memory
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
```

```
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : Yes
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : Yes
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : Auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 8
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Yes
Use Synchronous Set                : Yes
Use Synchronous Reset              : Yes
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
Verilog 2001                       : YES
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
```

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=========================================================================


=========================================================================
*                        HDL Compilation                                *
=========================================================================
Compiling verilog file "fifo_memory.v" in library work
Module <fifo_memory> compiled
Module <memory_array> compiled
Module <read_pointer> compiled
Module <status_signal> compiled
Module <write_pointer> compiled
No errors in compilation
Analysis of file <"fifo_memory.prj"> succeeded.


=========================================================================
*                     Design Hierarchy Analysis                         *
=========================================================================
Analyzing hierarchy for module <fifo_memory> in library <work>.

Analyzing hierarchy for module <write_pointer> in library <work>.

Analyzing hierarchy for module <read_pointer> in library <work>.

Analyzing hierarchy for module <memory_array> in library <work>.

Analyzing hierarchy for module <status_signal> in library <work>.


=========================================================================
*                          HDL Analysis                                 *
=========================================================================
Analyzing top module <fifo_memory>.
Module <fifo_memory> is correct for synthesis.

Analyzing module <write_pointer> in library <work>.
Module <write_pointer> is correct for synthesis.

Analyzing module <read_pointer> in library <work>.
Module <read_pointer> is correct for synthesis.

Analyzing module <memory_array> in library <work>.
Module <memory_array> is correct for synthesis.

Analyzing module <status_signal> in library <work>.
Module <status_signal> is correct for synthesis.


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```
*                            HDL Synthesis                                 *
================================================================================

Performing bidirectional port resolution...

Synthesizing Unit <write_pointer>.
    Related source file is "fifo_memory.v".
    Found 5-bit up counter for signal <wrptr>.
    Summary:
        inferred   1 Counter(s).
Unit <write_pointer> synthesized.


Synthesizing Unit <read_pointer>.
    Related source file is "fifo_memory.v".
    Found 5-bit up counter for signal <rdptr>.
    Summary:
        inferred   1 Counter(s).
Unit <read_pointer> synthesized.


Synthesizing Unit <memory_array>.
    Related source file is "fifo_memory.v".
WARNING:Xst:647 - Input <rdptr<4>> is never used. This port will be preserved and
left unconnected if it belongs to a top-level block or it belongs to a sub-block and
the hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <wrptr<4>> is never used. This port will be preserved and
left unconnected if it belongs to a top-level block or it belongs to a sub-block and
the hierarchy of this sub-block is preserved.
    Found 16x8-bit dual-port RAM <Mram_out2> for signal <out2>.
    Summary:
        inferred   1 RAM(s).
Unit <memory_array> synthesized.


Synthesizing Unit <status_signal>.
    Related source file is "fifo_memory.v".
WARNING:Xst:646 - Signal <pointer_result<2:0>> is assigned but never used. This
unconnected signal will be trimmed during the optimization process.
    Found 1-bit register for signal <fifo_underflow>.
    Found 1-bit register for signal <fifo_overflow>.
    Found 1-bit xor2 for signal <fbit_comp>.
    Found 4-bit subtractor for signal <pointer_equal$addsub0000> created at line 54.
    Found 5-bit subtractor for signal <pointer_result>.
    Summary:
        inferred   2 D-type flip-flop(s).
        inferred   2 Adder/Subtractor(s).
Unit <status_signal> synthesized.
```

```
Synthesizing Unit <fifo_memory>.
    Related source file is "fifo_memory.v".
Unit <fifo_memory> synthesized.


=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 1
 16x8-bit dual-port RAM                                : 1
# Adders/Subtractors                                   : 2
 4-bit subtractor                                      : 1
 5-bit subtractor                                      : 1
# Counters                                             : 2
 5-bit up counter                                      : 2
# Registers                                            : 2
 1-bit register                                        : 2
# Xors                                                 : 1
 1-bit xor2                                            : 1

=========================================================================

=========================================================================
*                        Advanced HDL Synthesis                         *
=========================================================================


Synthesizing (advanced) Unit <memory_array>.
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_out2> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it
synchronous would allow you to take advantage of available block RAM resources, for
optimized device usage and improved timings. Please refer to your documentation for
coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 16-word x 8-bit                     |          |
    |     clkA           | connected to signal <clk>           | rise     |
    |     weA            | connected to signal <fifo_we>       | high     |
    |     addrA          | connected to signal <wrptr>         |          |
    |     diA            | connected to signal <in>            |          |
    ----------------------------------------------------------------------
    | Port B                                                               |
    |     aspect ratio   | 16-word x 8-bit                     |          |
    |     addrB          | connected to signal <rdptr>         |          |
    |     doB            | connected to signal <out>           |          |
    ----------------------------------------------------------------------
```

```
Unit <memory_array> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 1
 16x8-bit dual-port distributed RAM                    : 1
# Adders/Subtractors                                   : 2
 4-bit subtractor                                      : 1
 5-bit subtractor                                      : 1
# Counters                                             : 2
 5-bit up counter                                      : 2
# Registers                                            : 2
 Flip-Flops                                            : 2
# Xors                                                 : 1
 1-bit xor2                                            : 1

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=========================================================================
*                           Low Level Synthesis                         *
=========================================================================

Optimizing unit <fifo_memory> ...

Optimizing unit <status_signal> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block fifo_memory, actual ratio is 0.
FlipFlop top1/wrptr_1 has been replicated 1 time(s)

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 13
 Flip-Flops                                            : 13

=========================================================================

=========================================================================
*                             Partition Report                          *
=========================================================================

Partition Implementation Status
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```

```
  No Partitions were found in this design.

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=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : fifo_memory.ngr
Top Level Output File Name         : fifo_memory
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 25

Cell Usage :
# BELS                             : 41
#      INV                         : 3
#      LUT2                        : 9
#      LUT3                        : 4
#      LUT3_L                      : 4
#      LUT4                        : 10
#      LUT4_D                      : 2
#      LUT4_L                      : 2
#      MUXCY                       : 4
#      VCC                         : 1
#      XORCY                       : 2
# FlipFlops/Latches                : 13
#      FDCE                        : 13
# RAMS                             : 8
#      RAM16X1D                    : 8
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 24
#      IBUF                        : 11
#      OBUF                        : 13
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s400pq208-5

 Number of Slices:                       25  out of   3584     0%
 Number of Slice Flip Flops:             13  out of   7168     0%
 Number of 4 input LUTs:                 50  out of   7168     0%
    Number used as logic:                34
```

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    Number used as RAMs:                16
 Number of IOs:                         25
 Number of bonded IOBs:                 25  out of    141    17%
 Number of GCLKs:                        1  out of      8    12%

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Partition Resource Summary:
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  No Partitions were found in this design.

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=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 21    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
rst_n_inv(top4/rst_n_inv1_INV_0:O) | NONE(top1/wrptr_0)     | 13    |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 5.661ns (Maximum Frequency: 176.656MHz)
   Minimum input arrival time before clock: 4.295ns
   Maximum output required time after clock: 11.402ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

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=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.661ns (frequency: 176.656MHz)
  Total number of paths / destination ports: 326 / 98
-------------------------------------------------------------------------
Delay:               5.661ns (Levels of Logic = 2)
  Source:            top1/wrptr_3 (FF)
  Destination:       top1/wrptr_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: top1/wrptr_3 to top1/wrptr_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q            28   0.626   1.615  top1/wrptr_3 (top1/wrptr_3)
     LUT4_D:I2->O          7   0.479   0.929  top4/fifo_overflow_and0000221
(top4/fifo_overflow_and0000221)
     LUT4:I3->O           14   0.479   1.009  top1/fifo_we1 (fifo_we)
     FDCE:CE                   0.524          top1/wrptr_0
    ----------------------------------------
    Total                      5.661ns (2.108ns logic, 3.553ns route)
                                       (37.2% logic, 62.8% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 37 / 31
-------------------------------------------------------------------------
Offset:              4.295ns (Levels of Logic = 3)
  Source:            rd (PAD)
  Destination:       top4/fifo_underflow (FF)
  Destination Clock: clk rising

  Data Path: rd to top4/fifo_underflow
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.715   1.148  rd_IBUF (rd_IBUF)
     LUT4_L:I0->LO         1   0.479   0.270  top4/fifo_underflow_not00011_SW0 (N8)
     LUT4:I1->O            1   0.479   0.681  top4/fifo_underflow_not00011
(top4/fifo_underflow_not0001)
     FDCE:CE                   0.524          top4/fifo_underflow
    ----------------------------------------
    Total                      4.295ns (2.197ns logic, 2.098ns route)
                                       (51.1% logic, 48.9% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 87 / 13
-------------------------------------------------------------------------
```

```
Offset:              11.402ns (Levels of Logic = 8)
  Source:            top1/wrptr_0 (FF)
  Destination:       fifo_threshold (PAD)
  Source Clock:      clk rising

  Data Path: top1/wrptr_0 to fifo_threshold
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q            31   0.626   1.865  top1/wrptr_0 (top1/wrptr_0)
     LUT2:I0->O            1   0.479   0.000  top4/Msub_pointer_result_lut<0>
(top4/Msub_pointer_result_lut<0>)
     MUXCY:S->O            1   0.435   0.000  top4/Msub_pointer_result_cy<0>
(top4/Msub_pointer_result_cy<0>)
     MUXCY:CI->O           1   0.056   0.000  top4/Msub_pointer_result_cy<1>
(top4/Msub_pointer_result_cy<1>)
     MUXCY:CI->O           1   0.056   0.000  top4/Msub_pointer_result_cy<2>
(top4/Msub_pointer_result_cy<2>)
     MUXCY:CI->O           0   0.056   0.000  top4/Msub_pointer_result_cy<3>
(top4/Msub_pointer_result_cy<3>)
     XORCY:CI->O           1   0.786   0.976  top4/Msub_pointer_result_xor<4>
(top4/pointer_result<4>)
     LUT2:I0->O            1   0.479   0.681  top4/fifo_threshold_or00001
(fifo_threshold_OBUF)
     OBUF:I->O                 4.909          fifo_threshold_OBUF (fifo_threshold)
    ----------------------------------------
    Total                     11.402ns (7.881ns logic, 3.522ns route)
                                       (69.1% logic, 30.9% route)

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Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.73 secs

-->

Total memory usage is 4521448 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    3 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```