Control Block PL	As													
L DI A	C. Lance J. L. Lance INC	T24 INCT20 INCT20 IN	ICTOO INICTOT	INICTOC										
ImmPLA	6 input bits: ins	5T31, INST30, INST29, IN	15128, INS127	, INS126										
Output bit:	501	Immi												
	se:	Imm: 00 1XXX												
	00 1000	1X XXXX												
	00 1000	17 7777												
	00 1001													
	00 1010													
	00 1011													
	00 1100													
	00 1101													
	00 1111													
pcPLA	16 Input hits: IN	16 Input bits: INST31, INST30, INST29, INST28, INST27, INST26, INST20, INST16, n, eq, INST5, INST4, INST3, INST2, INST1, INST												
PCFLA	10 mput bits. in	13131, 1143130, 1143123,	1143120, 114312	7, IIV3120	, 1143120, 11	43110, 11,	eq, 114313, 11431	4, IIVJ I	J, 114312, 11	1311, 11131				
Output bit:	s0:	s1:	retaddr:											
	00 0000 00 XX 01	.001 00 0000 00 XX 0100	X 00 0010 XX	XX XXXXX										
	00 0001 XX XX XX	XXX 00 0011 XX XX XXXX	Х											
	00 0011 XX XX XX	XXX												
	00 0100 XX X1 XX	XXX												
	00 0101 XX X0 XX	XXX												
	00 0110 00 1X XX	XXX												
	00 0110 00 X1 XX	XXX												
	00 0111 00 00 XX	XXX												
	00 0001 XX XX XX	XXX												
funcPLA	12 Input bits: INST31, INST30, INST29, INST28, INST27, INST26, INST5, INST4, INST3, INST2, INST1, INST0													
Output bit:	func0:	func1:	func2:		func3:		func4:		func5:					
	000000 XXXXX1	000000 XXXX1X	000000 XX	000000 XXX1XX		XX 1XXX	000000 X1XXXX		000000 1XXXXX					
	0010X1 XXXXXX	001010 XXXXXX	00110X XX	00110X XXXXXX		XXXXX			001XXX XXXXXX					
	001101 XXXXXX	001011 XXXXXX	001110 XXXXXX						10X011 X	XXXXX				
		001110 XXXXXX												

ShamtPLA	11 Input	bits: INST31	L, INST30,	INST29, INS	T28, INST	27, INST26,	INST10, II	NST9, INST8	, INST7, IN	IST6				
Output bit:	sa0:		sa1:		sa2:		sa3:		sa4:					
	000000 XXXX1		000000 XXX1X		000000 XX1XX		000000 X1XXX		000000 1XXXX					
									001111 X	01111 XXXXX				
CselPLA	16 Input	bits: INST31	L, INST30,	INST29, INS	T28, INST	27, INST26,	INST20, II	NST19, INST	18, INST1	7, INST16, I	NST15, IN	ST14, INST	13, INST12	2, INS
Output bit:	s0:		s1:		s2:		s3:		s4:					
RD VALUES	00 0000 X	XXXX XXXX1	00 0000 X	XXXX XXX1X	00 0000 X	XXXX XX1XX	00 0000 X	XXXX X1XXX	00 0000 XX	XXXX 1XXXX				
RT	00 1XXX X	XXXX1 XXXX	00 1XXX	XXX1X XXXX	00 1XXX >	XX1XX XXXX	00 1XXX X	(1XXX XXXX	00 1XXX 1	XXXX XXXX	X			
RT	10 XXXX X	XXX1X XXXX	10 XXXX	XXX1X XXXX	10 XXXX X	XX1XX XXXX	10 XXXX	(1XXX XXXX	10 XXXX 1	XXXX XXXX	X			
0x1f	00 0001 >	X0001 XXXX	00 0001	X0001 XXXX	00 0001 >	(0001 XXXX	00 0001 >	(0001 XXXX	00 0001 X	0001 XXXX	X			
0X1f	00 0011 >	XXXX XXXX	00 0011	XXXXX XXXX	00 0011 >	XXXX XXXX	00 0011 >	XXXX XXXX	00 0011 X	XXXX XXXX	X			
memPLA	6 Input bits: INST31, INST30, INST29, INST28, INST27, INST26													
Output bit:	dmen*:	dmwr*:	load:											
	10 0011		10 0011											
	10 1011	10 1011												
*Active Low!														