Control Block PLAs														
ImmPLA	**6 Input bits: INST31, INST30, INST29, INST28, INST27, INST26**													
Output bit:	se:		Imm:											
	1X XXXX		00 1XXX											
	00 1000		1X XXXX											
	00 1001													
	00 1010													
	00 1011													
	00 1100													
	00 1101													
	00 1111													
pcPLA	**16 Input bits: INST31, INST30, INST29, INST28, INST27, INST26, INST20, INST16, n, eq, INST5, INST4, INST3, INST2, INST1, INST**													
Output bit:	s0:		s1:		retaddr:									
	00 0000 00 XX 01001		00 0000 00 XX 0100X		00 0010 XX XX XXXXX									
	00 0001 XX XX XXXXX		00 0011 XX XX XXXXX											
	00 0011 XX XX XXXXX													
	00 0100 XX X1 XXXXX													
	00 0101 XX X0 XXXXX													
	00 0110 00 1X XXXXX													
	00 0110 00 X1 XXXXX													
	00 0111 00 00 XXXXX													
	00 0001 XX XX XXXXX													
funcPLA	**12 Input bits: INST31, INST30, INST29, INST28, INST27, INST26, INST5, INST4, INST3, INST2, INST1, INST0**													
Output bit:	func0:		func1:		func2:		func3:		func4:		func5:			
	000000 XXXXX1		000000 XXXX1X		000000 XXX1XX		00 0000 XX 1XXX		000000 X1XXXX		000000 1XXXXX			
	0010X1 XXXXXX		001010 XXXXXX		00110X XXXXXX		00101X XXXXXX				001XXX XXXXXX			
	001101 XXXXXX		001011 XXXXXX		001110 XXXXXX						10X011 XXXXXX			
			001110 XXXXXX											

ShamtPLA	**11 Input bits: INST31, INST30, INST29, INST28, INST27, INST26, INST10, INST9, INST8, INST7, INST6**													
Output bit:	sa0:		sa1:		sa2:		sa3:		sa4:					
	000000 XXXX1		000000 XXX1X		000000 XX1XX		000000 X1XXX		000000 1XXXX					
									001111 XXXXX					
CselPLA	**16 Input bits: INST31, INST30, INST29, INST28, INST27, INST26, INST20, INST19, INST18, INST17, INST16, INST15, INST14, INST13, INST12, INST11**													
Output bit:	s0:		s1:		s2:		s3:		s4:					
RD VALUES	00 0000 XXXXX XXXX1		00 0000 XXXXX XXX1X		00 0000 XXXXX XX1XX		00 0000 XXXXX X1XXX		00 0000 XXXXX 1XXXX					
RT	00 1XXX XXXX1 XXXX		00 1XXX XXX1X XXXX		00 1XXX XX1XX XXXX		00 1XXX X1XXX XXXX		00 1XXX 1XXXX XXXXX					
RT	10 XXXX XXX1X XXXX		10 XXXX XXX1X XXXX		10 XXXX XX1XX XXXX		10 XXXX X1XXX XXXX		10 XXXX 1XXXX XXXXX					
0x1f	00 0001 X0001 XXXX		00 0001 X0001 XXXX		00 0001 X0001 XXXX		00 0001 X0001 XXXX		00 0001 X0001 XXXXX					
0X1f	00 0011 XXXXX XXXX		00 0011 XXXXX XXXX		00 0011 XXXXX XXXX		00 0011 XXXXX XXXX		00 0011 XXXXX XXXXX					
memPLA	**6 Input bits: INST31, INST30, INST29, INST28, INST27, INST26**													
Output bit:	dmen*:	dmwr*:	load:											
	10 0011		10 0011											
	10 1011	10 1011												
*Active Low!														