EE517 ANALOG IC DESIGN LAB

Experiment 6

Design and analysis of a 2-stage op-amp.

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Contents

1 Objective

The objective of this project is to design and analyze a two-stage operational amplifier (op-amp) based on the given design specifications.

1.1 Design Specifications

- Voltage Gain (A_v): 1000 (or 60 dB)
- Unity gain frequency : 100 MHz
- Load Capacitance (C_L): 1 pF
- Common Mode Gain: 0.1V/V
- Slew Rate: 10 V/u
- MOSFET Channel Length: 180 nm
- Phase Margin: 60
- Output Voltage swing: 800m(atleast)
- Supply Voltage: 1.8V

2 Theoretical Background

2.1 Key Definitions

2.1.1 Transconductance (g_m)

Transconductance measures how effectively a MOSFET converts an input voltage variation into an output current variation. It is defined as:

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{1}$$

where I_{DS} is the drain current and V_{GS} is the gate-to-source voltage.

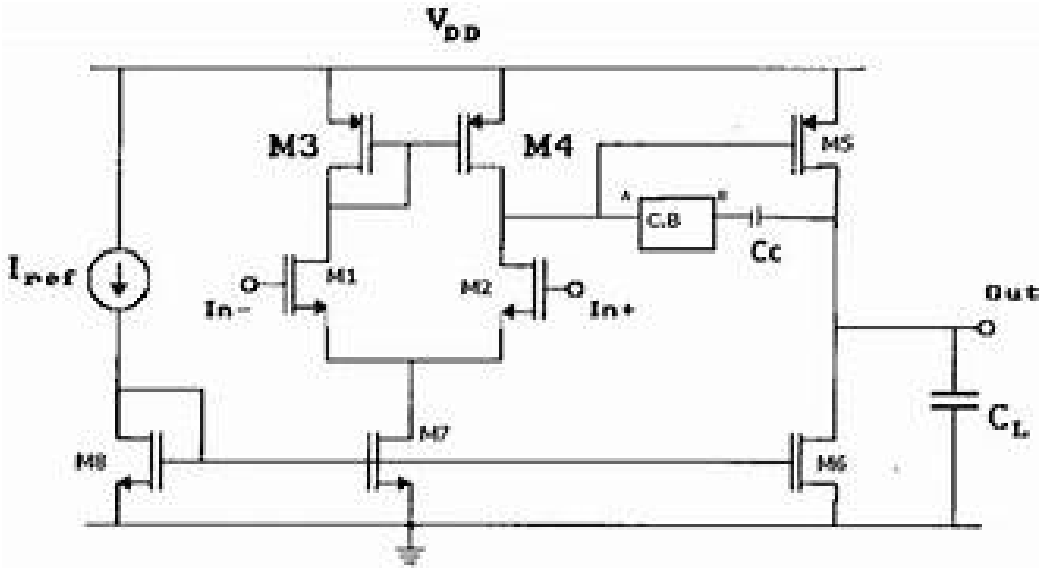

Figure 1: 2 stage opamp

2.1.2 Voltage Gain (A_v)

Voltage gain represents how much an input signal is amplified by the circuit:

$$A_v = \frac{V_{out}}{V_{in}} \tag{2}$$

2.1.3 Cutoff Frequency (f_c)

The cutoff frequency is the frequency at which the gain drops by 3 dB, defined as:

$$f_c = \frac{1}{2\pi R_{out} C_{out}} \tag{3}$$

where R_{out} is the output resistance and C_{out} is the output capacitance.

2.1.4 Output Resistance (R_{out})

The output resistance of a MOSFET determines how much of the amplified signal is delivered to the load. It is given by:

$$R_{out} = \frac{V_{test}}{I_{test}} \tag{4}$$

2.1.5 Slew Rate (SR)

The slew rate is the maximum rate of change of output voltage per unit time:

$$\text{SR} = \left(\frac{dV_{out}}{dt}\right)_{max} = \frac{I_5}{C_c} \tag{5}$$

where I_5 is the tail current and C_c is the Miller capacitance.

2.1.6 Input Common Mode Range (ICMR)

ICMR defines the range of input common-mode voltages where all transistors remain in saturation.

2.1.7 Gain Bandwidth Product (GBWP)

The GBWP is the product of open-loop gain and the frequency at which the amplifier gain drops by 20 dB.

3 Two-Stage Op-Amp Design

A two-stage op-amp consists of:

1. A differential amplifier for amplification.
2. A second stage common-source amplifier to boost gain.
3. A compensation capacitor to ensure stability.

3.1 Design Procedure

3.1.1 Step 1: Compensation Capacitor (C_c)

To ensure stability with a phase margin of 60°, the Miller capacitance is calculated as:

$$C_c > 0.22 C_L = 2.2 \text{ pF} \tag{6}$$

Thus, we select $C_c = 300$ fF.

3.1.2 Step 2: Slew Rate Consideration

$$I_5 = C_c \times \text{SR} = 20 \ \mu A \tag{7}$$

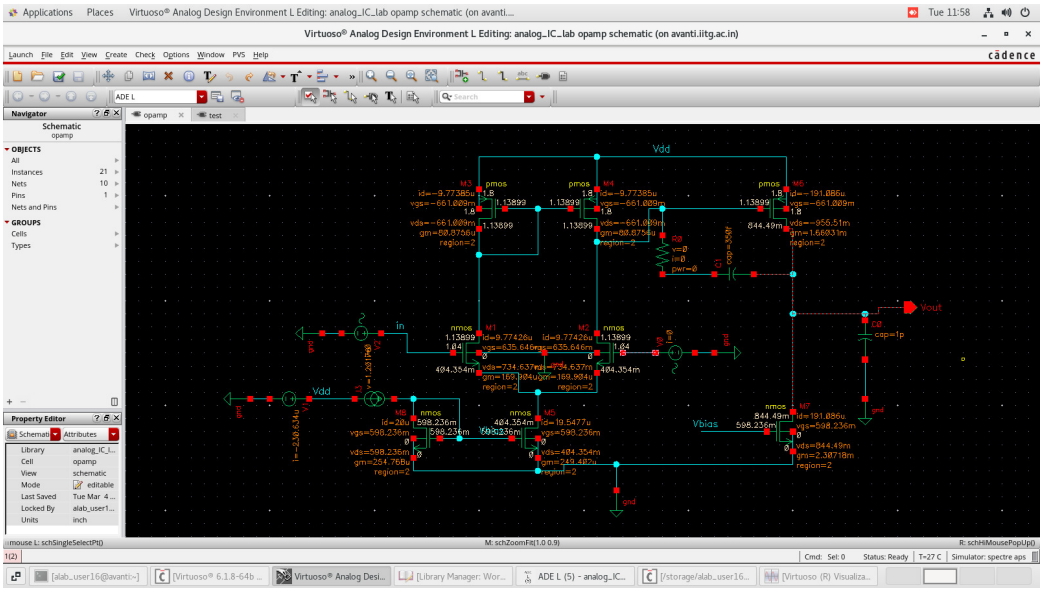

Figure 2: two stage opamp

3.1.3 Step 3: Gain Bandwidth Product (GBW)

$$g_{m1} = \text{GBW} \times 2\pi C_c \tag{8}$$

Substituting values,

$$g_{m1} = 160\ \mu A/V \tag{9}$$

Using the transconductance equation:

$$g_{m1} = 2I_D \mu_n C_{ox} \frac{W}{L} \tag{10}$$

Solving for $\frac{W}{L}$:

$$\frac{W}{L}_1 = \frac{W}{L}_2 = 12 \tag{11}$$

3.2 Step 4: Current Source

Given the current source $I_5 = 10\,\mu A$, we use this current value for further calculations.

$$I_5 = 20\,\mu A \tag{10}$$

3.3 Step 5: Gain-Bandwidth Product

We calculate the gain-bandwidth product as the voltage unit gain frequency. The dominant pole causes a 20 dB decay at unit gain frequency.

$$g_{m1} = \frac{GBW}{2\pi C_C} \tag{11}$$

Substitute the given values for GBW and C_C to find the value of g_{m1}.

$$g_{m1} = 160\,\mu A \tag{12}$$

3.4 Step 6: MOSFET Transconductance Equation

We use the MOSFET transconductance equation:

$$g_{m1} = \sqrt{\frac{2I_D\mu_n C_{ox}}{\frac{W}{L}}} \tag{13}$$

Substitute the values to calculate the $\frac{W}{L}$ ratio:

$$\frac{W}{L} = 10.385 \tag{14}$$

Assuming symmetry between M_1 and M_2, we set:

$$\frac{W}{L}_1 = \frac{W}{L}_2 = 12 \tag{15}$$

3.5 Step 7: Input Common-Mode Range (ICMR)

Given the maximum ICMR value of 1.6 V, we calculate the maximum gate voltage V_G for M_1 to remain in saturation. Using the gate-to-source voltage equation, we derive the value for $\frac{W}{L}_3$ for transistor M_3.

$$V_G < (V_{DD} - (V_{tp} + \sqrt{2I_D\mu_p C_{ox}\frac{W}{L}3}) + Vth1) \tag{19}$$

After substituting all values, we find:

$$\frac{W}{L}_3 = 13.02 \tag{21}$$

Since M_3 and M_4 are symmetric, we set:

$$\frac{W}{L}_3 = \frac{W}{L}_4 = 14 \tag{22}$$

3.6 Step 8: Minimum ICMR

We calculate the minimum ICMR value by ensuring all transistors are in saturation. Using the saturation condition equation for V_{DS}, we find:

$$V_{DS_{sat}} = I_{CMR_{min}} - \sqrt{2I_D\mu_n C_{ox}\frac{W}{L}1} - Vthn \tag{23}$$

After substituting all the values:

$$V_{DS_{sat}} = 0.946 \tag{24}$$

We then use the current equation to calculate $\frac{W}{L}_5$:

$$\frac{W}{L}_5 = 12.09 \tag{25}$$

We set:

$$\frac{W}{L}_5 = 12 \tag{26}$$

3.7 Step 9: Transconductance of M6

We assume that the transconductance g_{m6} is at least 10 times the value of g_{m1}:

$$g_{m6} > 10 \cdot g_{m1} \tag{27}$$

Using the value of g_{m1}:

$$g_{m6} > 1600\,\mu A \tag{28}$$

From the current mirror relationship, we have:

$$\frac{W/L_6}{W/L_4} = \frac{I_6}{I_4} = \frac{g_{m6}}{g_{m4}} \tag{29}$$

Substitute the known values of I_4 and g_{m4}:

$$g_{m4} = 129.61\,\mu A \tag{30}$$

Thus, we calculate:

$$\frac{W}{L}_{6} = 172.82 \tag{31}$$

Also, we find:

$$I_6 = 125\,\mu A \tag{32}$$

3.8 Step 10: Transconductance of M7

Using the fact that M_6 and M_7 are in series and both currents are equal, we have:

$$\frac{W/L_7}{W/L_5} = \frac{I_7}{I_5} \tag{33}$$

From this, we calculate:

$$\frac{W}{L}_{7} = 75 \tag{34}$$

3.9 Step 11: Length Calculation

Now that we have the values of the W/L ratios, we need to calculate the lengths. We know the gain of the two-stage operational amplifier is:

$$\text{gain} = g_{m1}g_{m2}\left(r_{01}||r_{04}\right)\left(r_{06}||r_{07}\right) \tag{35}$$

Substitute the values of g_{m1}, g_{m2}, and the gain into the equation:

$$\left(r_{01}||r_{04}\right)\left(r_{06}||r_{07}\right) = 640 \times 10^9 \tag{36}$$

To achieve this, we increase the length of the transistors. After performing the calculations, we get the following values for the W/L ratios:

- M_1 and M_2: $W/L = 180\,\text{nm}$
- M_3, M_4 and M_8: $W/L = 500\,\text{nm}$

- M_5: 1 um
- M_6 and M_7: $W/L = 360\,\text{nm}$

4 DC Analysis

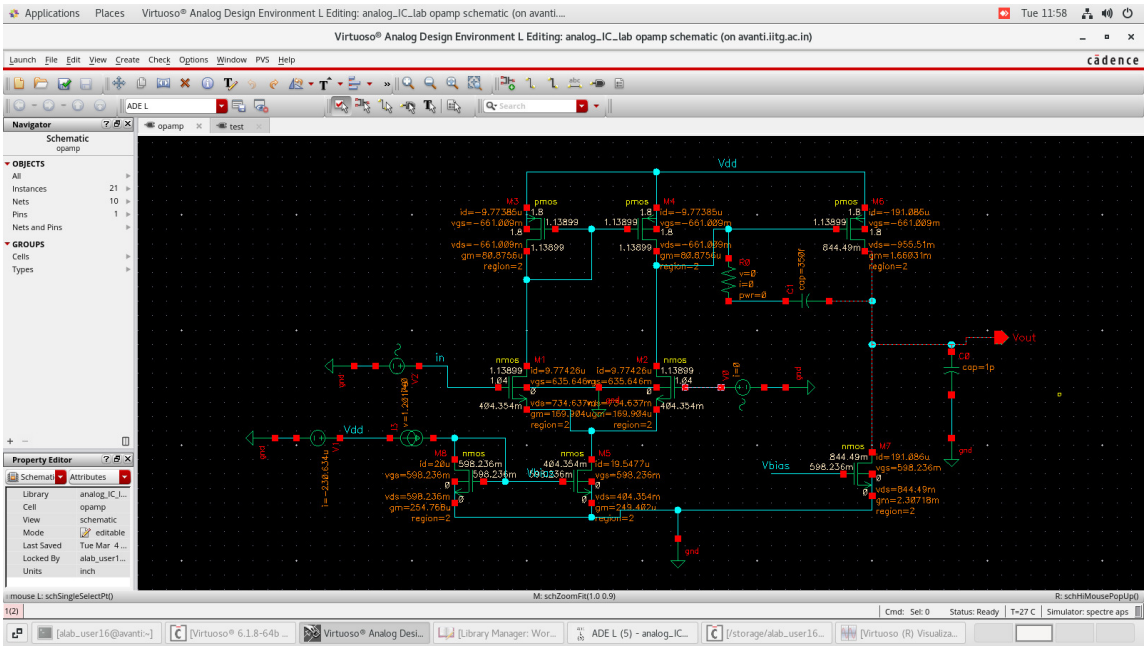

Figure 3: schematic

5 AC Analysis

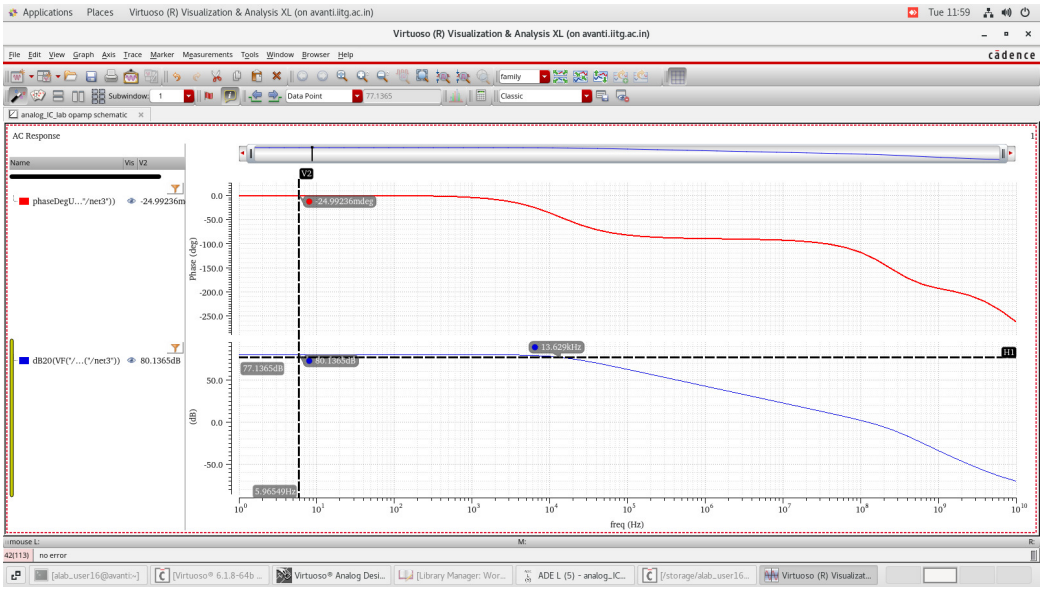

Figure 4: gain

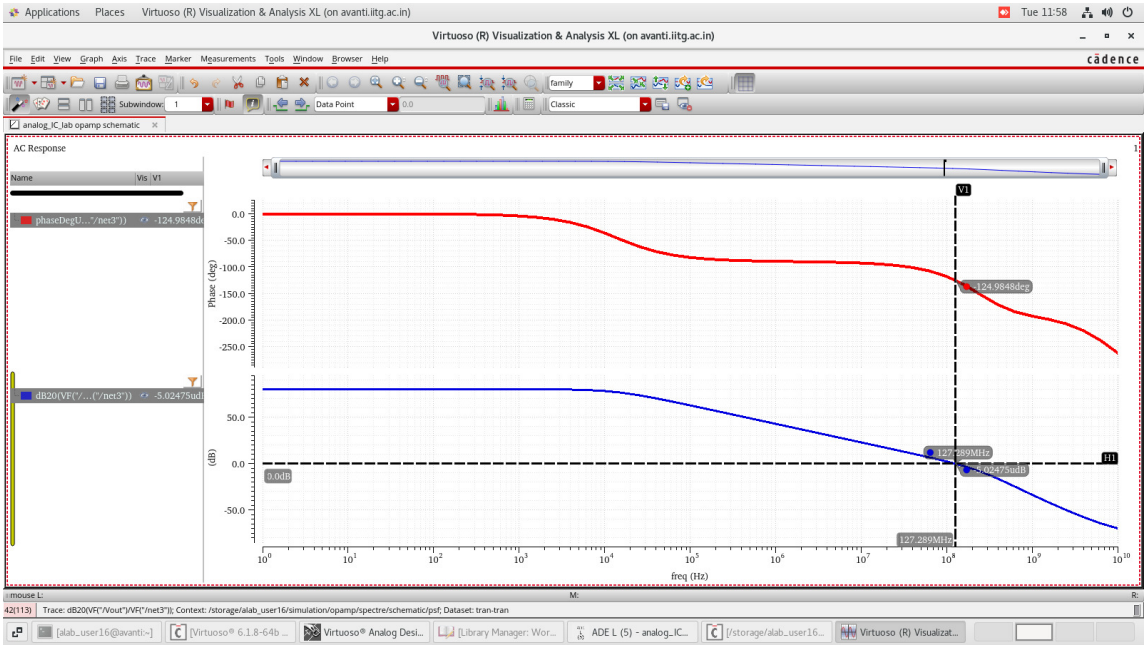

Figure 5: odb freq

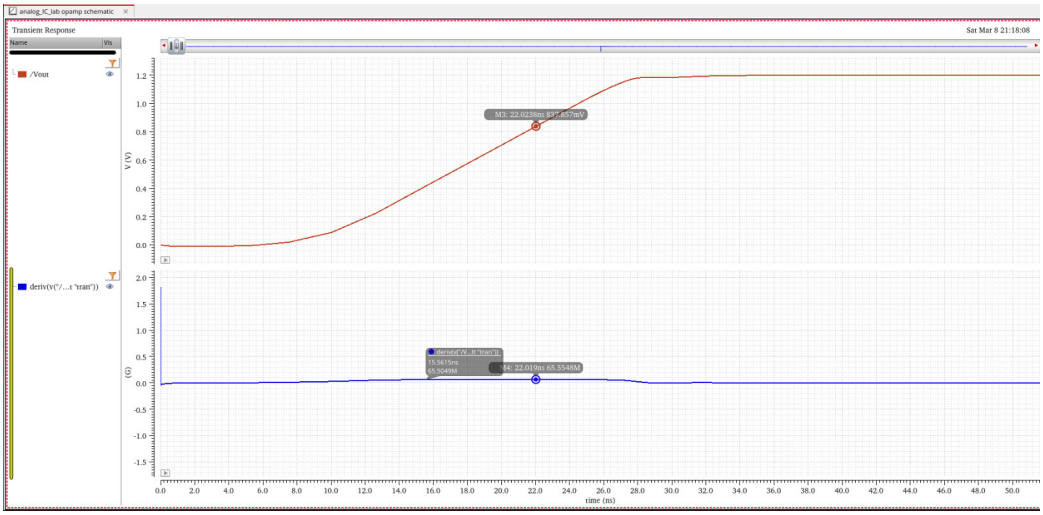

Figure 6: Common mode rejection ratio

6 Transient Anlysis

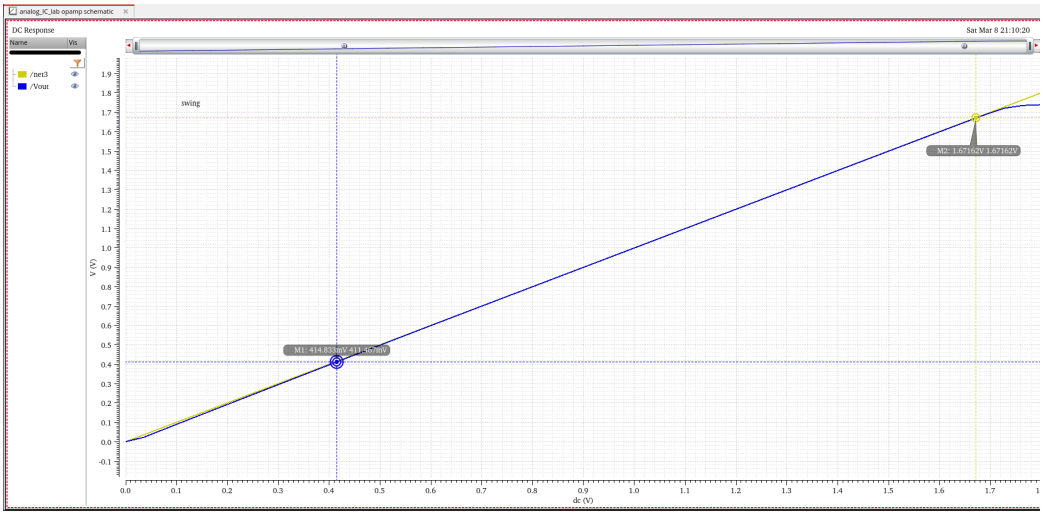

Figure 7: input and output swing

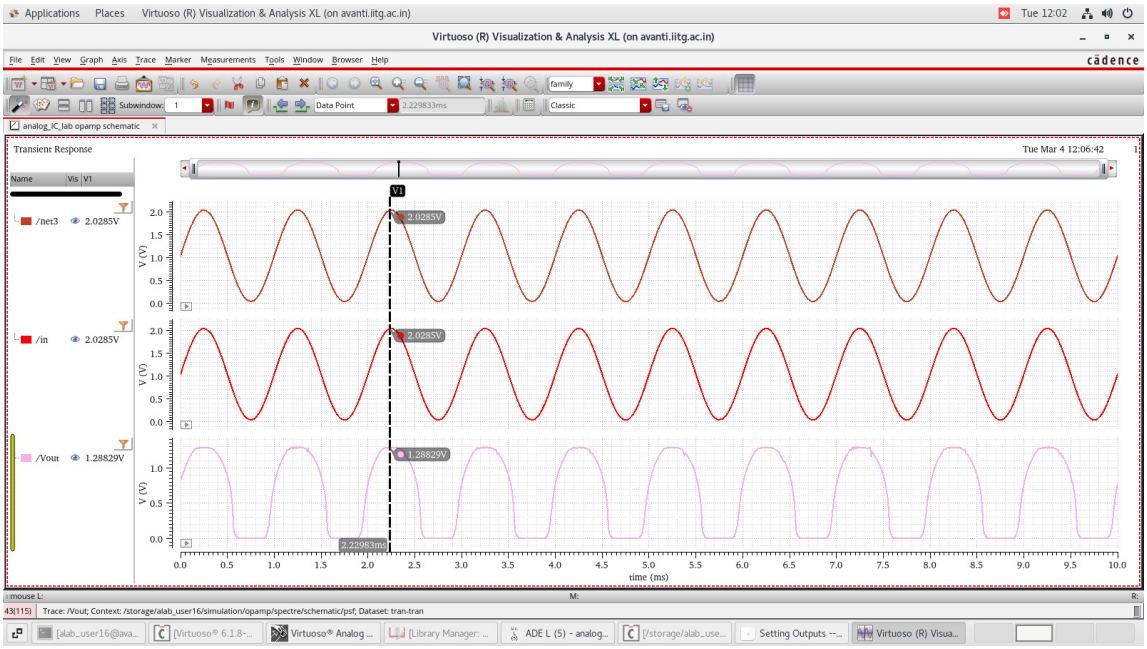

Figure 8: slew rate

7 Results

7.1 Transistor Dimensions

Transistor	Width (um)	Length (nm)
M1, M2	6	500
M3, M4	7	500
M5	12	1(u)
M6	174	1u
M7	75	1u
M8	same or less than M7	

Table 1: Transistor Widths and Lengths

Transistor	Width (um)	Length (nm)
M1, M2	6	500
M3, M4	3	180
M5	7	1(u)
M6	84	360
M7	13.5	360
M8	3.5	500

Table 2: practical value

7.2 Capacitance Values

Capacitor	Value (pF)
C_c	3
C_L	10

Table 3: Capacitor Values

7.3 Comparison of Theoretical and Practical Results

Parameter	Theoretical	Practical
Gain (dB)	66.6	60.9
phaseMargin	60	60.1
Slewrate	20	22

Table 4: Theoretical vs. Practical Results

Parameter	Practical	
inout swing	0.4148	1.6
CMR	-26.5db	

Table 5: Theoretical vs. Practical Results