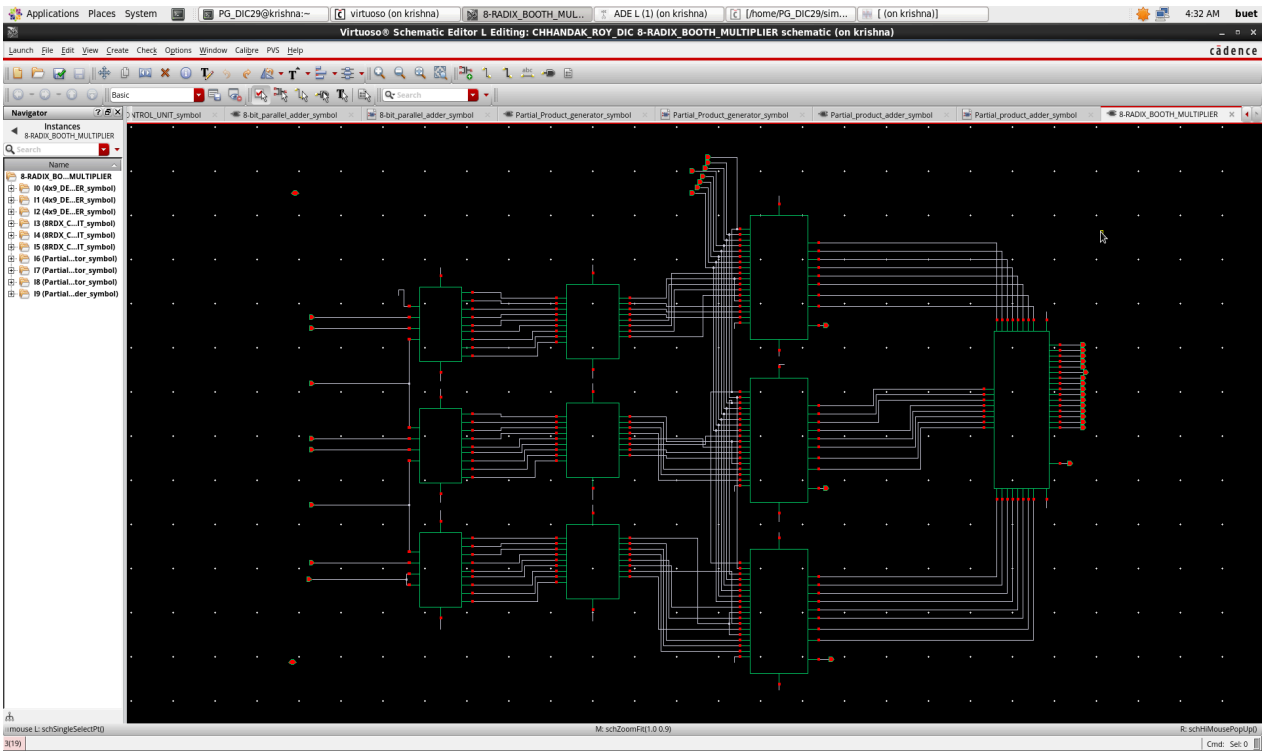
8-RADIX Booth Multiplier

Block Diagram & Overview



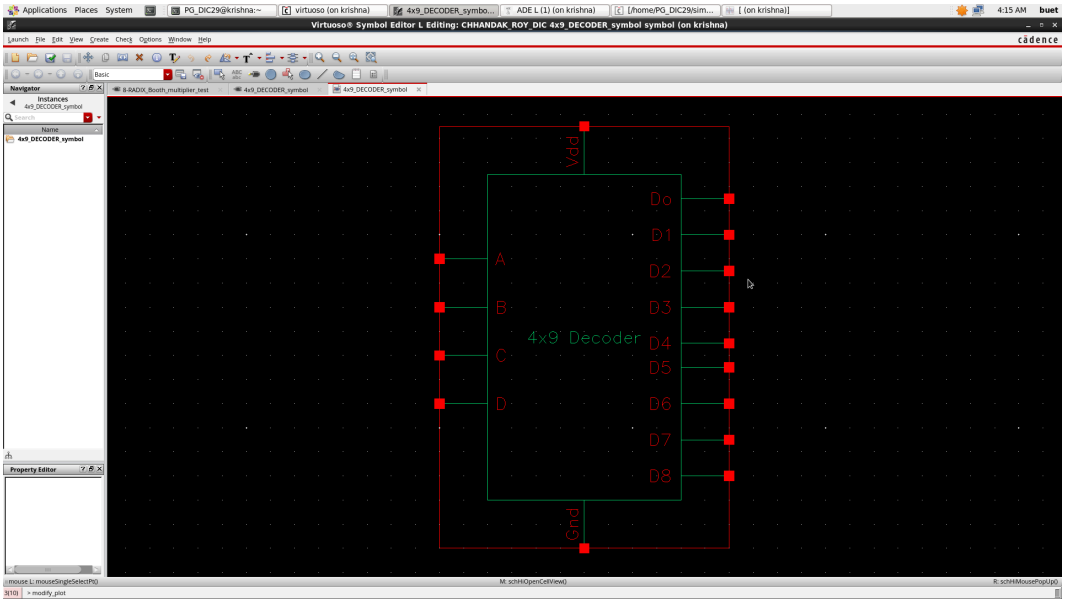
The 8-radix booth multiplier has been implemented using the 8 radix booth algorithm, which enables it to perform signed and unsigned 8-bit multiplication with the same architecture.
Following is the 8 radix Multiplication encoding rule:

Table 2. Radix-8 Booth Multiplier encoding table

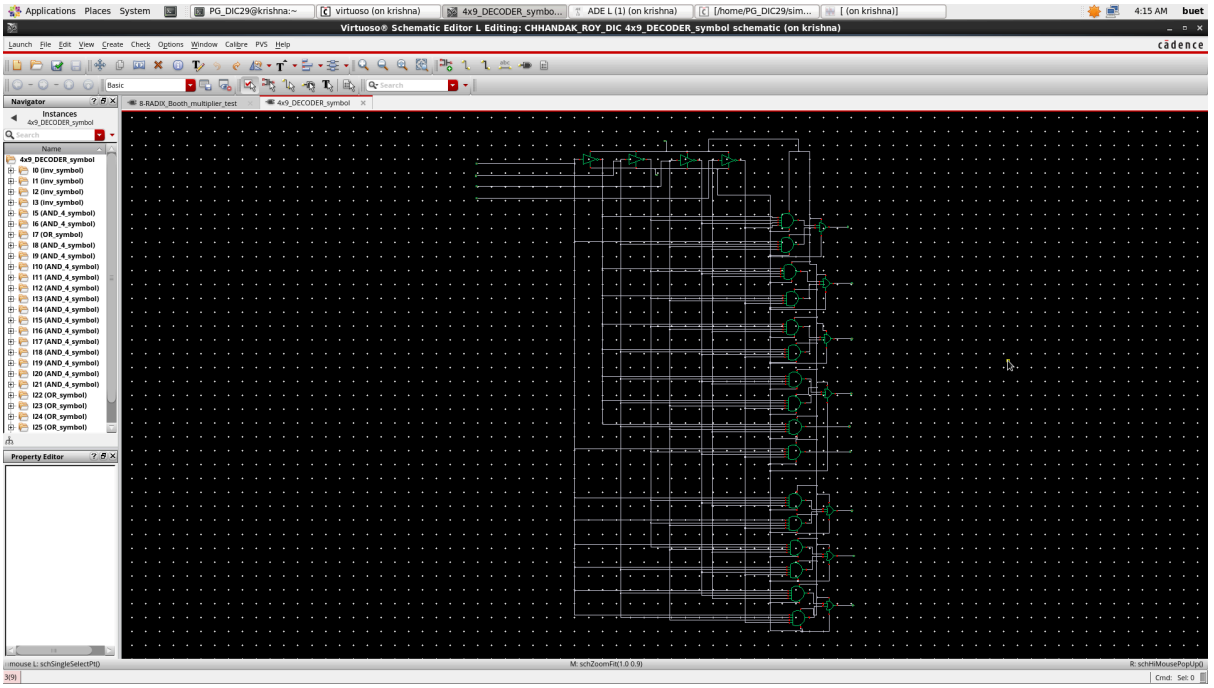
Multiplier Bits				Operation on Multiplicand
A	B	C	D	X
0	0	0	0	0X
0	0	0	1	+1X
0	0	1	0	+1X
0	0	1	1	+2X
0	1	0	0	+2X
0	1	0	1	+3X
0	1	1	0	+3X
0	1	1	1	+4X
1	0	0	0	-4X

The Multiplier has been made with the following stages:

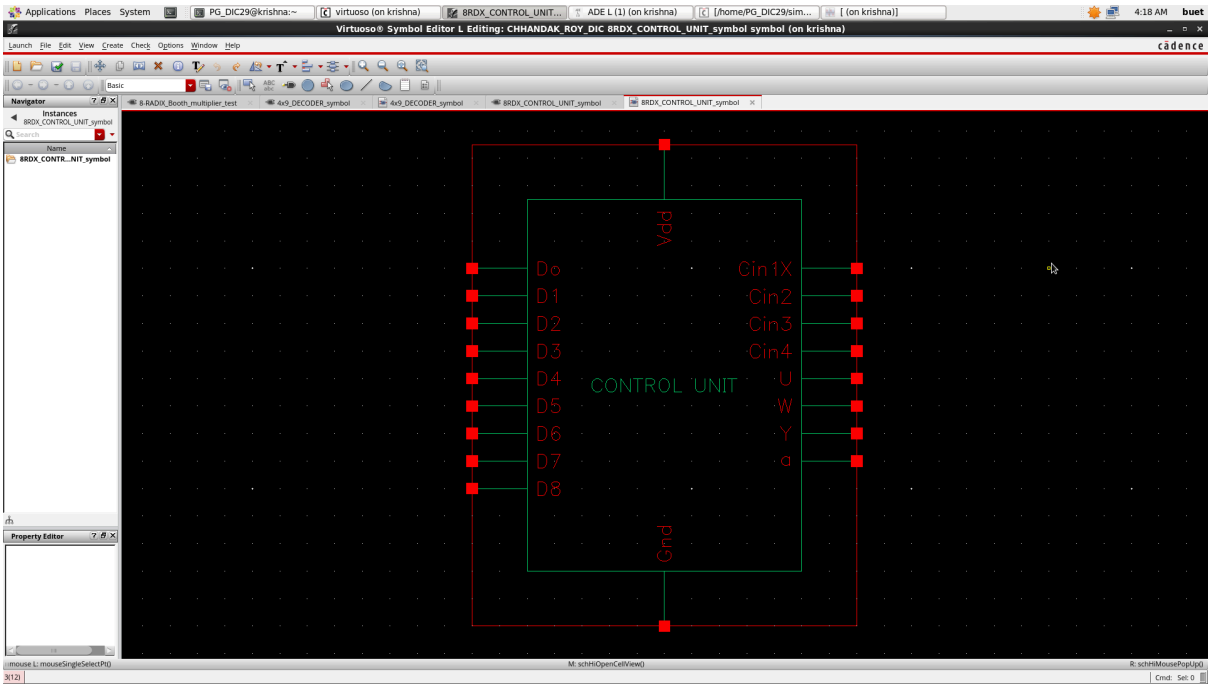
- **4:9 Decoder**
  A total of three 4:9 decoder has been used at the input of the multiplier, with the last input being shorted to the first input bit of the next coder because of overlapped grouping used in the 8-radix booth algorithm.



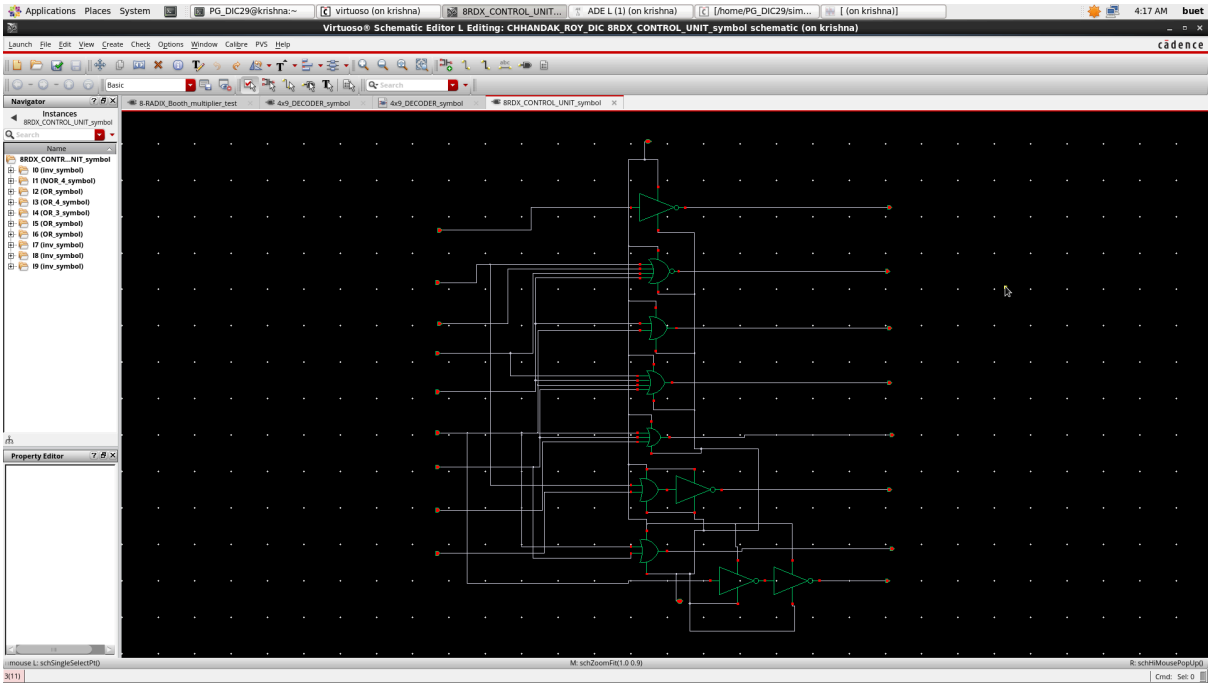
The Decoder tells the control unit about the bit combination received and the operation that should be done on the Multiplier(M) based on the bit grouping received.



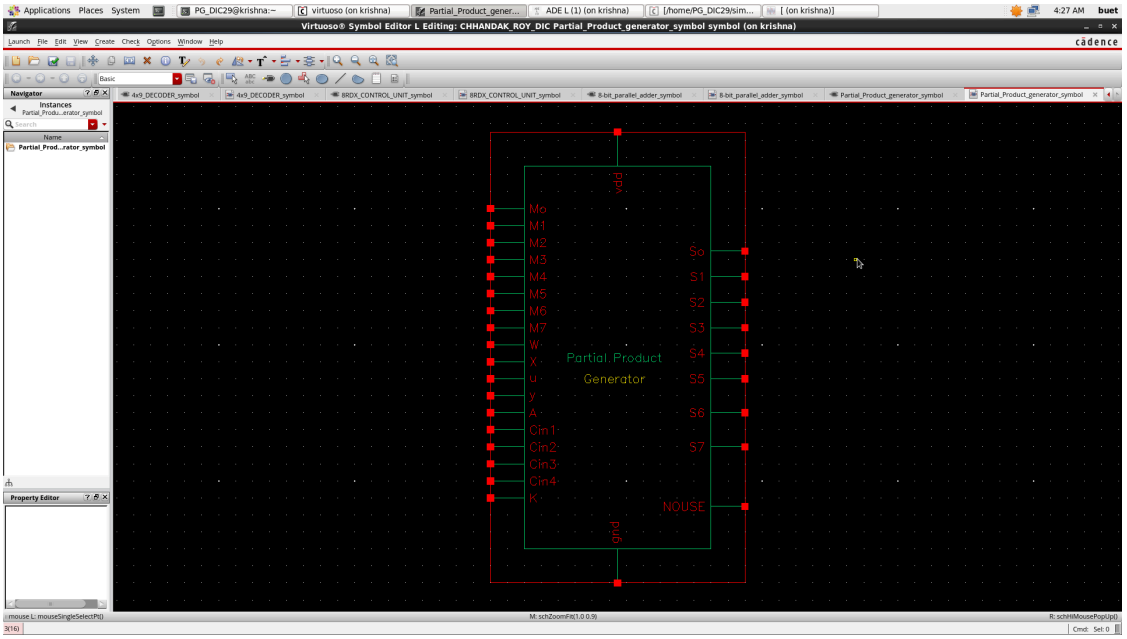
- **Control Unit**
  The output of the three decoders are fed to three Control Units which decide the operations to be done on the Multiplicand(M) based on the bit-combination in the grouping like 1M,2M,3M,-3M etc.(as shown in table 2)
  Thus the control has 9 input pins and controls the above operations using 8 control pins.

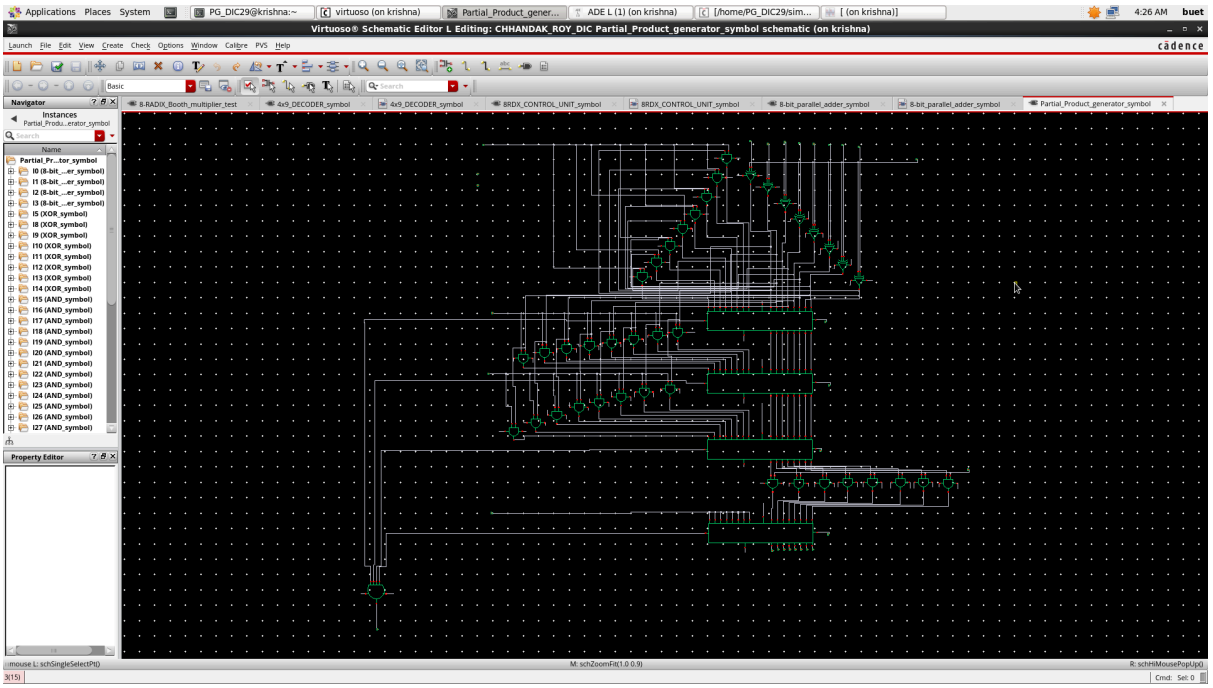


Control unit symbol & Scehmatic



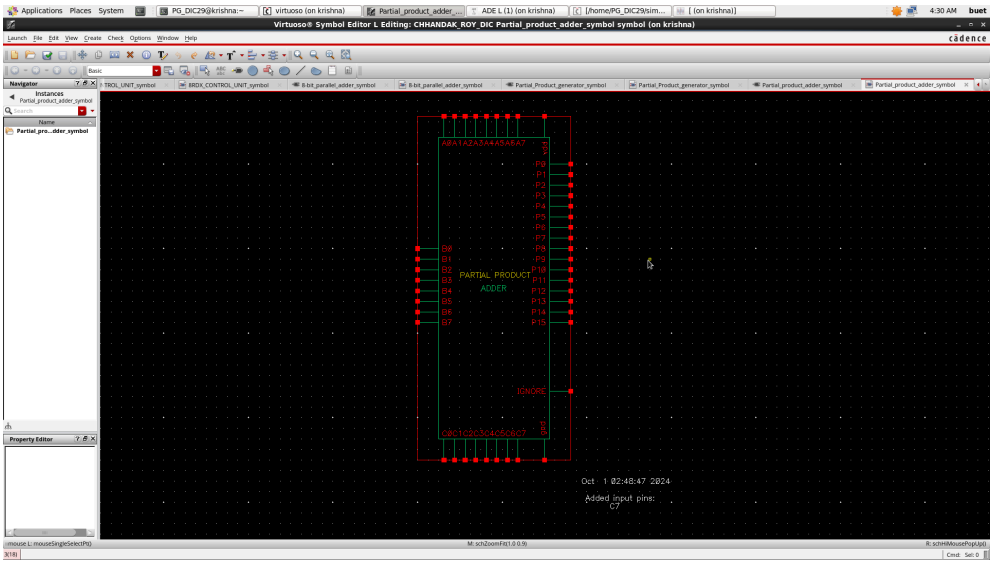
- **Partial Product Generator(PPG)**
  It consists of four 8-bit adder for performing operations on Multiplicand (M) as per the control signals received from the control unit. One PPG generates Partial product for the first bit grouping, similarly all of them together generates 3 PP which are added in the next stage i.e. PP adder.

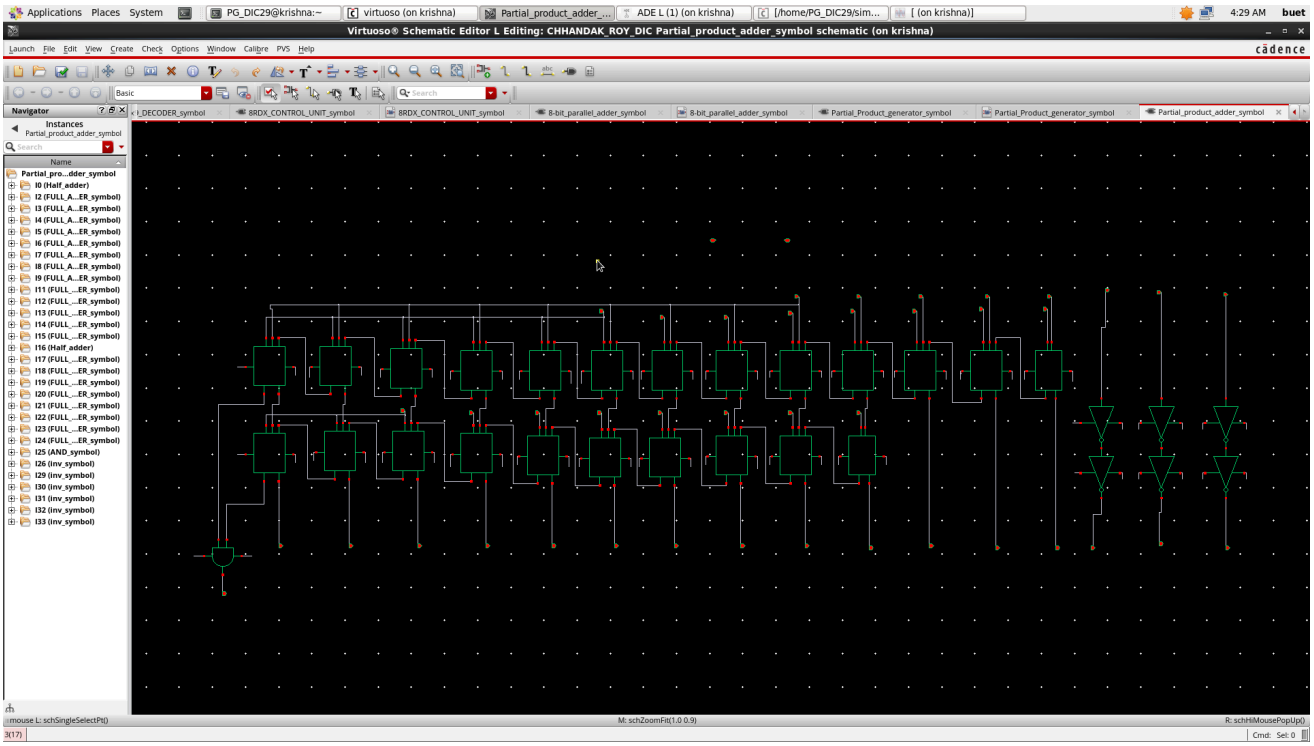




- **Partial Product Adder**

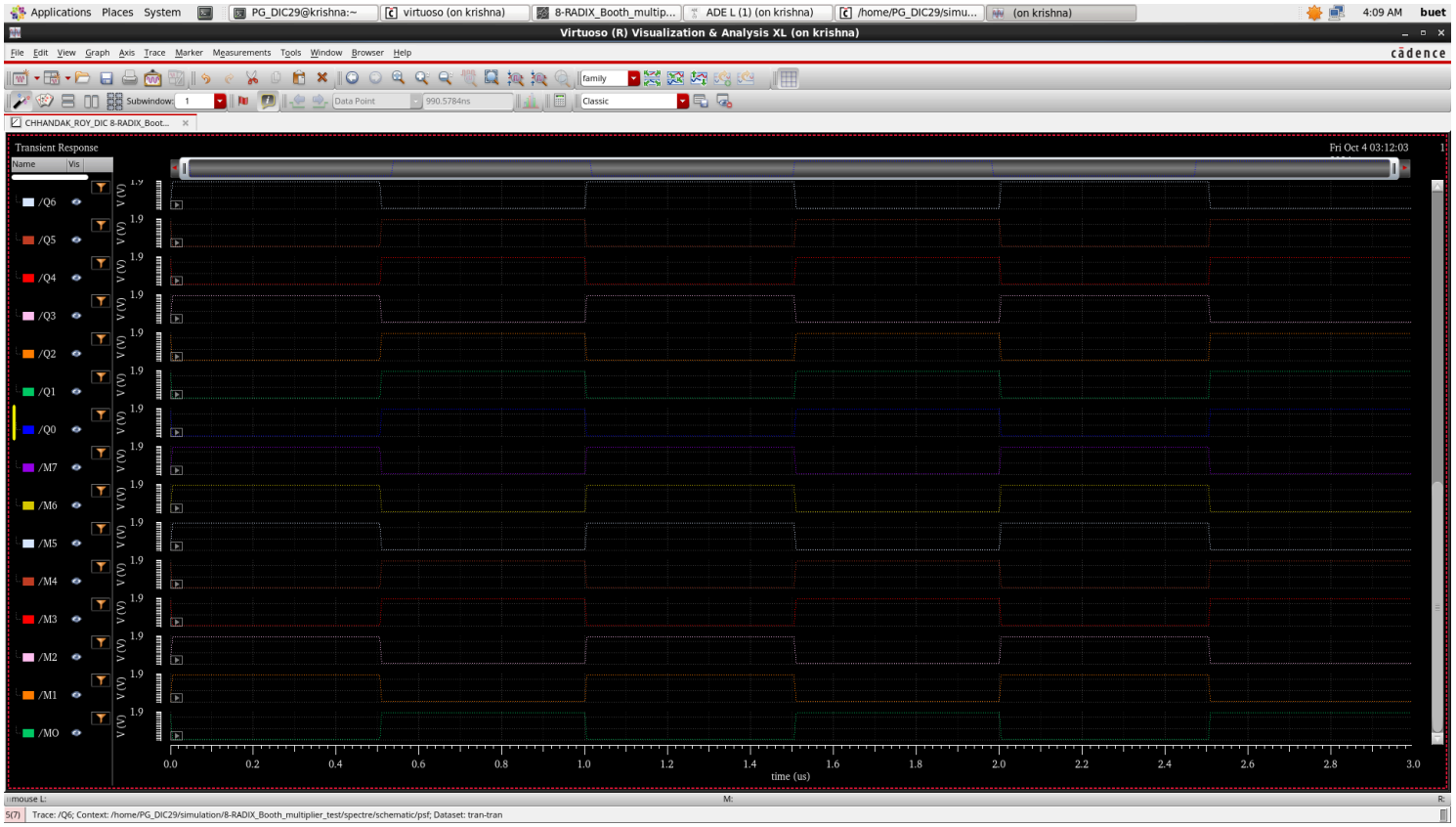
  All the partial products generated in the previous stage are added here, where each partial products is interpolated to 16 bit (because multiplication is in 8-radix format) by copying the MSB to the next 8 bits and then all of the 3 partial products are added by Ripple carry adder to generate 16 bit output.



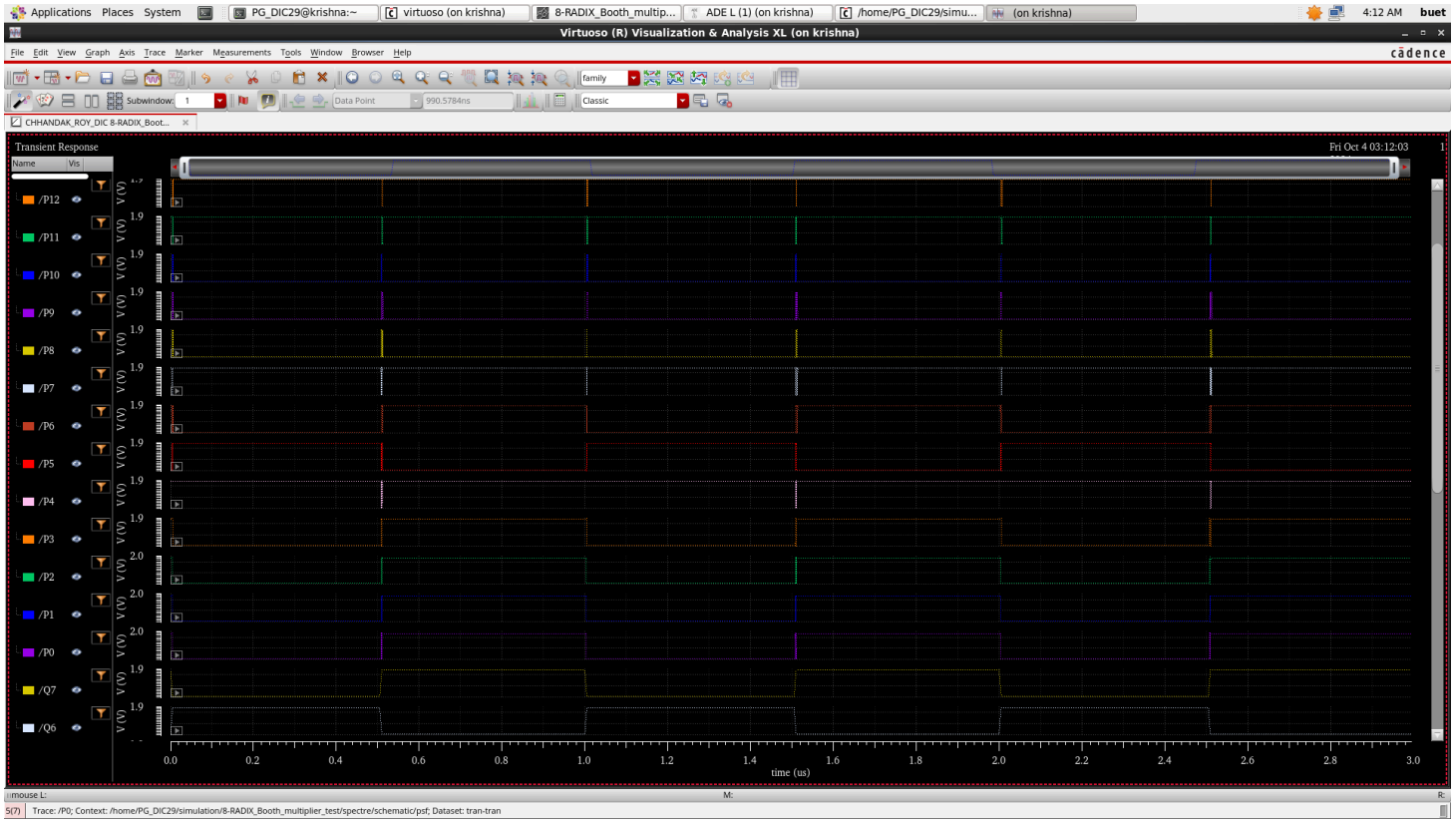


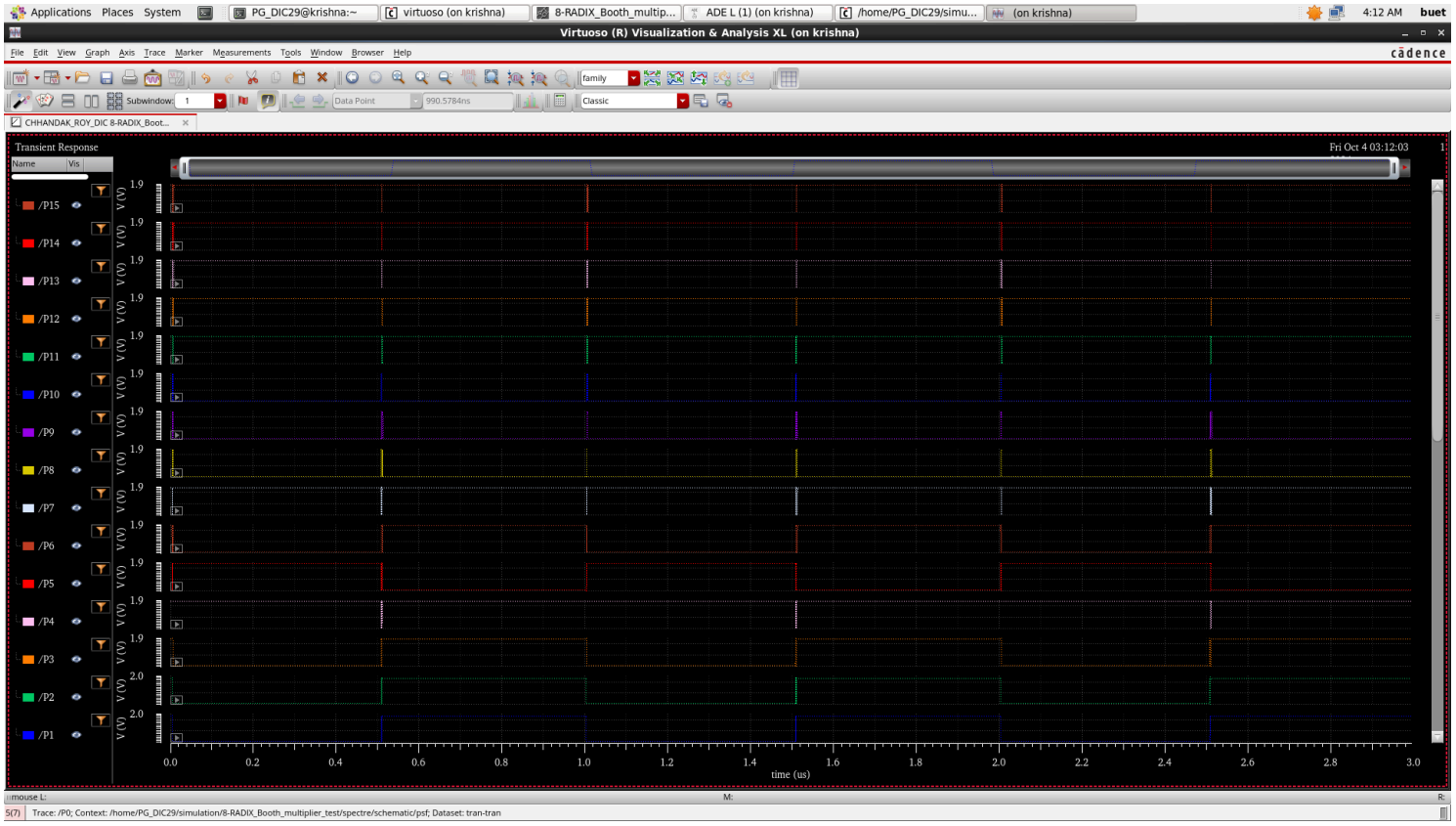
Results

Multiplier(Q) = 1 0 1 1 0 1 1 1 (-73)
Multiplicand (M)= 0 0 0 1 1 0 0 1 (25)
Output= 25 x -73 =-1825= 1 1 1 1 1 1 0 0 0 1 1 0 1 1 1 1 1



M and Q inputs (in 2nd cycle)





Output (in 2nd cycle)