Pre-Lab 4

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Problem 1. DFF Flip Flop Truth Table

Input				Output	
$\overline{\text{PRESET}}$	$\overline{\text{CLEAR}}$	Clock	D	Q	Q'
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	X	X
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_0	Q'_0

Problem 2. JK Flip Flop Truth Table

Input				Output	
Clear	Clock	J	K	Q	Q'
0	X	X	X	1*	1*
1	↓	0	0	Q_0	Q'_0
1	↓	0	1	0	1
1	↓	1	0	1	0
1	↓	1	1	Q'_0	Q_0
1	↓	X	X	Q_0	Q'_0

Problem 3. Logic Diagram of tiny ALU with DFF Accumulator