CS4341.504 HW#1 - solution
FALL SEMESTER 2023

INSTRUCTOR: DR. ALICE WANG

Part 1 - Signed/Unsigned (10pts)

What is the 2's complement for the following numbers? Show the number to **16 bits**

Dec	Bin	Hex
-400	0b1111_1110_0111_0000	0xFE70
-7	0b1111_1111_1111_1001	0xFFF9
0	0b0000_0000_0000_0000	0x0000
5693	0b_0001_0110_0011_1101	0x163D
10453	0b_0010_1000_1101_0101	0x28D5

Part 2 - Multi-bit gates (10pts)

Fill out the following Truth Table for inputs A, B, and C.

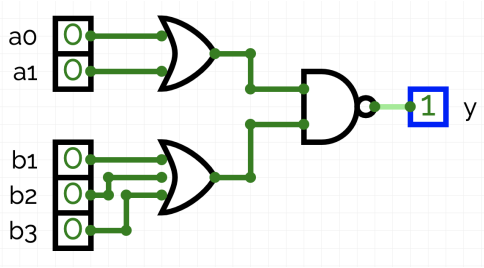
ABC	NAND3	OR3	XNOR3	INV	BUF
000	1	0	1	111	000
001	1	1	0	110	001
010	1	1	0	101	010
011	1	1	1	100	011
100	1	1	0	011	100
101	1	1	1	010	101
110	1	1	1	001	110
111	0	1	0	000	111

Part 3 - Schematic and Verilog (30pts)

1. Use the circuitverse website to verify the functionality of an OAI23 (2-input OR 3-input AND-INVERT) Capture the screenshot of the complete logic circuit with inputs (a0, a1,

b0, b1, b2) and output (out). Use the toggle function (i.e. click on each input to change the input value) and observe the value of the output for ALL combinations of inputs, capture the screenshot of the circuit for each input combination. Write a report (PDF format) to document the task. The report must contain ALL screenshots and explanations for each of them as to why you think that the design is correct. Name this report HW01-Part3-1.

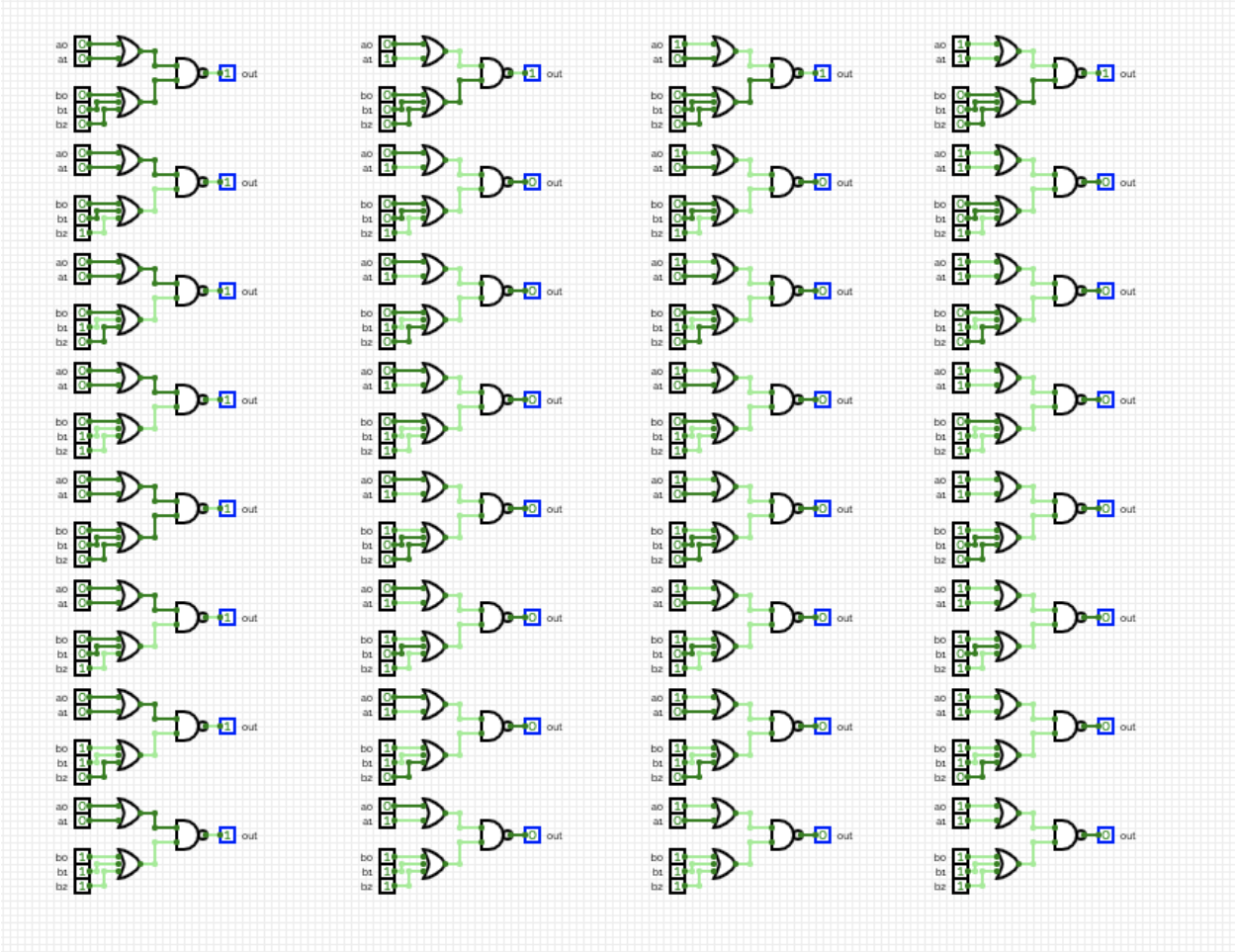
Schematic in circuitverse:



a0	a1	b0	b1	b2	out
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0

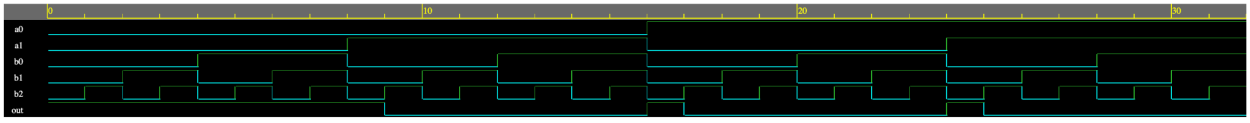
What I observe from the truth table is that out is “1” if a0 = a1 = 0 OR if b0 = b1 = b2 = 0. Otherwise it’s “0”.

In circuitverse I created 32 copies of the OAI23, toggled all inputs and verified the output to be the same as my truth table.



2. Using the edaplayground website, simulate the function of the OAI23 using the behavioral style. Name the file **`oai23.v`**. Write the code for a test bench file to run a simulation of the OAI23 and name the test bench file as **`oai23_tb.v`** and run the simulation. The test bench must cover all combinations of the inputs and when the simulation runs using the test bench, the waveform diagram must show the output of all combinations of the inputs.
   Log file:

```
# KERNEL: Start
# KERNEL: a0:0,a1:0,b0:0,b1:0,b2:0, out:1
# KERNEL: a0:0,a1:0,b0:0,b1:0,b2:1, out:1
# KERNEL: a0:0,a1:0,b0:0,b1:1,b2:0, out:1
# KERNEL: a0:0,a1:0,b0:0,b1:1,b2:1, out:1
# KERNEL: a0:0,a1:0,b0:1,b1:0,b2:0, out:1
# KERNEL: a0:0,a1:0,b0:1,b1:0,b2:1, out:1
# KERNEL: a0:0,a1:0,b0:1,b1:1,b2:0, out:1
# KERNEL: a0:0,a1:0,b0:1,b1:1,b2:1, out:1
# KERNEL: a0:0,a1:1,b0:0,b1:0,b2:0, out:1
# KERNEL: a0:0,a1:1,b0:0,b1:0,b2:1, out:0
# KERNEL: a0:0,a1:1,b0:0,b1:1,b2:0, out:0
# KERNEL: a0:0,a1:1,b0:0,b1:1,b2:1, out:0
# KERNEL: a0:0,a1:1,b0:1,b1:0,b2:0, out:0
# KERNEL: a0:0,a1:1,b0:1,b1:0,b2:1, out:0
# KERNEL: a0:0,a1:1,b0:1,b1:1,b2:0, out:0
# KERNEL: a0:0,a1:1,b0:1,b1:1,b2:1, out:0
# KERNEL: a0:1,a1:0,b0:0,b1:0,b2:0, out:1
# KERNEL: a0:1,a1:0,b0:0,b1:0,b2:1, out:0
# KERNEL: a0:1,a1:0,b0:0,b1:1,b2:0, out:0
# KERNEL: a0:1,a1:0,b0:0,b1:1,b2:1, out:0
# KERNEL: a0:1,a1:0,b0:1,b1:0,b2:0, out:0
# KERNEL: a0:1,a1:0,b0:1,b1:0,b2:1, out:0
# KERNEL: a0:1,a1:0,b0:1,b1:1,b2:0, out:0
# KERNEL: a0:1,a1:0,b0:1,b1:1,b2:1, out:0
# KERNEL: a0:1,a1:1,b0:0,b1:0,b2:0, out:1
# KERNEL: a0:1,a1:1,b0:0,b1:0,b2:1, out:0
# KERNEL: a0:1,a1:1,b0:0,b1:1,b2:0, out:0
# KERNEL: a0:1,a1:1,b0:0,b1:1,b2:1, out:0
# KERNEL: a0:1,a1:1,b0:1,b1:0,b2:0, out:0
# KERNEL: a0:1,a1:1,b0:1,b1:0,b2:1, out:0
# KERNEL: a0:1,a1:1,b0:1,b1:1,b2:0, out:0
# KERNEL: a0:1,a1:1,b0:1,b1:1,b2:1, out:0
```



3. Create a folder named HW01-Part3 containing all of the Verilog code, a report (PDF format) describing the steps that you have done for the simulation, and the waveform results when the simulation runs and describe how you can verify that the OAI23 design functions correctly. Include this folder in your homework submission.

See files
oai23.v, oai23_tb.v

I can see from the waveform that when a0 = a1 = 0, then out is 1, when b0 = b1 = b2 = 0, then out is 1. Otherwise it is 0.