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CS 4141.115
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Experiment 3 Post-Lab”

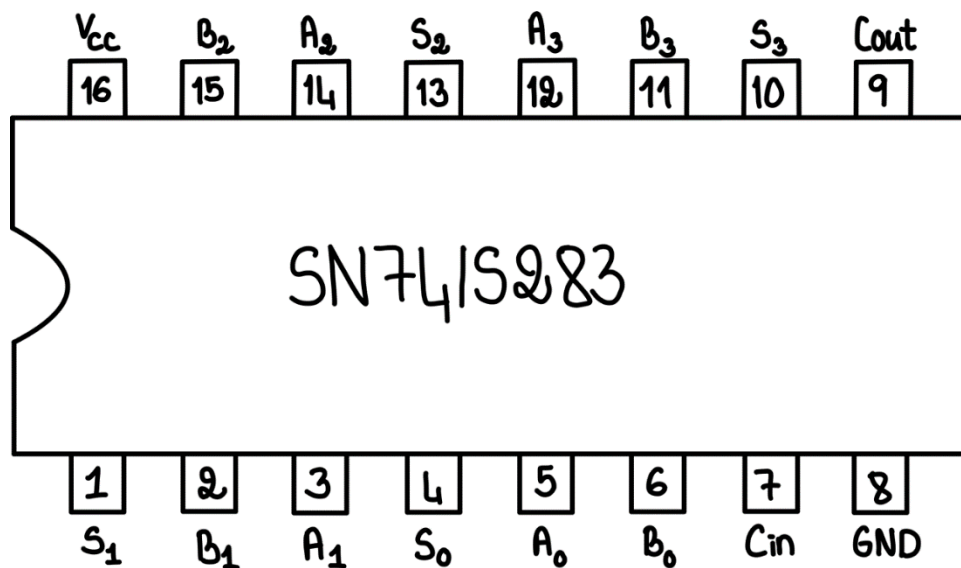
Partners: Korbin Schulz and Bennett Quigley

Part 1. 4-bit Addition using an IC chip such as 74LS283

- Results of 10 4-bit Additions

Input A	Input B	Cin	Sum	Cout
0000	0000	0	0000	0
0000	0001	0	0001	0
0000	0010	0	0010	0
0000	0011	0	0011	0
0000	0100	0	0100	0
0000	0101	0	0101	0
0000	0110	0	0110	0
0000	0111	0	0111	0
0000	1000	0	1000	0
0000	1001	0	1001	0

- Circuit Diagram of the IC chip

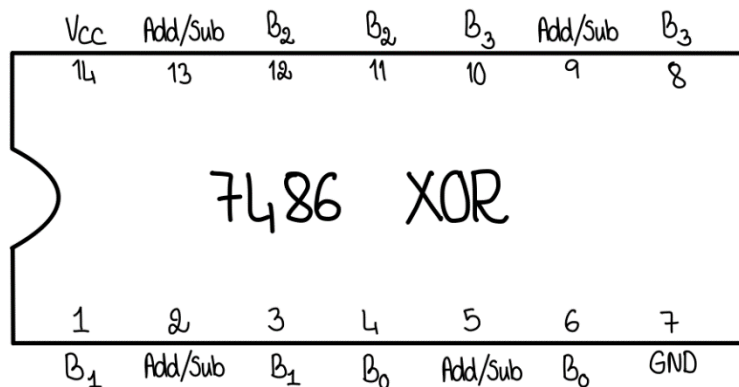
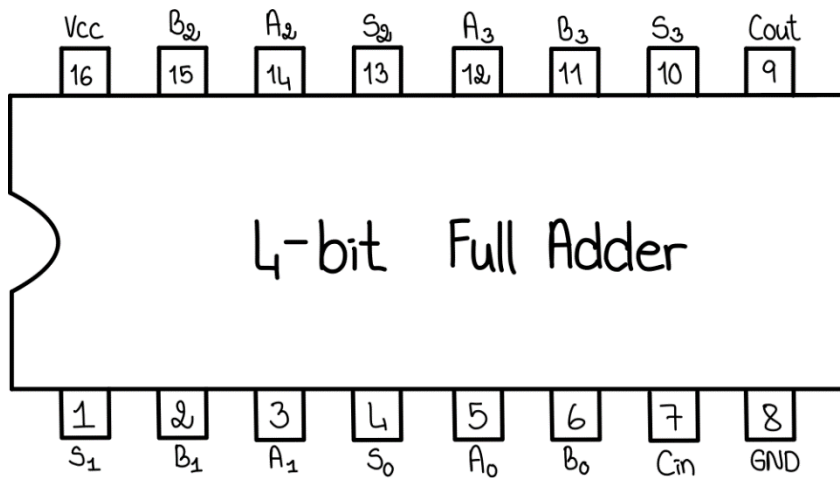


Part 2. 4-bit Subtraction using an IC chip such as 74LS283

- Results of 5 2-bit additions, and 5 2-bit subtractions

Input A	Input B	Cin	Binary Output	Binary Integer	2's Complement Integer
0000	0000	0	0000	0	0
0000	0001	0	0001	1	1
0001	0011	1	1110	14	-2
0001	0010	1	1111	15	-1
0011	0101	1	1000	8	8
0011	0010	0	0101	5	5
0101	0111	0	1100	12	-4
0101	1100	1	1001	9	-7
1100	1010	1	0010	2	2
1100	1100	0	0000	0	0

- Circuit Diagram of the 2-bit Adder/Subtractor



Part 3. Construct a Binary Coded Decimal (BCD) adder using the 4-bit binary full adders.

- Truth Table of 0 through 19 for the BCD Adder

Decimal	Binary	Binary Coded Decimal (BCD)
0	0000_0000	0000_0000
1	0000_0001	0000_0001
2	0000_0010	0000_0010
3	0000_0011	0000_0011
4	0000_0100	0000_0100
5	0000_0101	0000_0101
6	0000_0110	0000_0110
7	0000_0111	0000_0111
8	0000_1000	0000_1000
9	0000_1001	0000_1001
10	0000_1010	0001_0000
11	0000_1011	0001_0001
12	0000_1100	0001_0010
13	0000_1101	0001_0011
14	0000_1110	0001_0100
15	0000_1111	0001_0101
16	0001_0000	0001_0110
17	0001_0001	0001_0111
18	0001_0010	0001_1000
19	0001_0011	0001_1001

- Circuit Diagram of the BCD Adder

