Chhay Lay Heng
CS 4141.115
November 17, 2023

Experiment 4 Post-Lab

Partners: Korbin Schulz and Bennett Quigley

Part 1. D Flip-Flop

Initially we had trouble setting up the DFF because we had a faulty chip. After we changed the chip, it worked as intended. When PRE and CLR were not 1, then the value for D and CLK did not matter. When they are both 1, if D is 1 and CLK was high then it was 10, else it was 01.

Part 2. JK Flip-Flop

Our setup for JKFF was very similar to the one we used for the DFF. When J and K were 0 and CLK was ↑, we saw change. When J and K were 11, we saw it was opposite (toggled). Else we saw 10=1 and 01=0, FF changed to set state when we toggled the clock pulse switch and set J=1. Then when we changed to J=0, K=1 and re-toggled we saw Q go to Q, and the other light turned on (1).

Part 3. Building ALU based 4-bit addition using two 74SL74 (4 D FF's) and a 4-bit adder: