Pre-Lab 2
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Class: CS 4141.115
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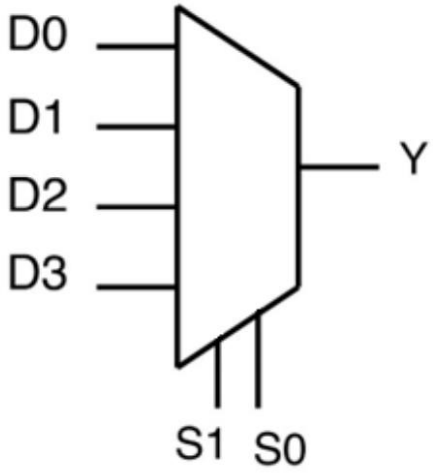
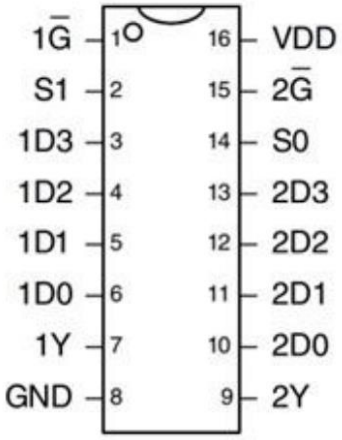
Problem 1. Understanding the Multiplexer



Multiplexer Symbol for Logic Diagram



74153 4 :1 Mux

IC Pinout

Two 4:1 Multiplexers
$D_{3:0}$: data
$S_{1:0}$: select
Y: output
Gb: enable

Legend for IC Pinout

1.1 For the 4:1 Mux, there are 2 select bits.

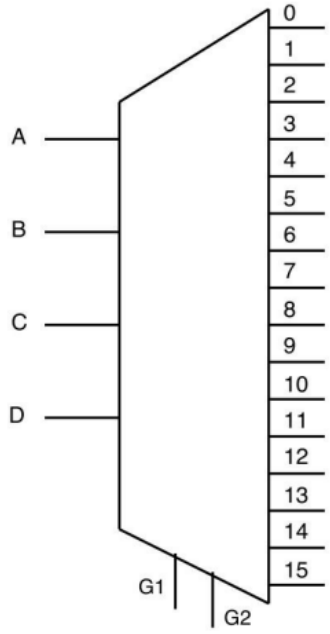
1.2 The most significant bit is S1.

1.3 Suppose S1 = 1, S0 = 0 and 1G = 0, then the signal will be assigned to output 1Y is 1D.

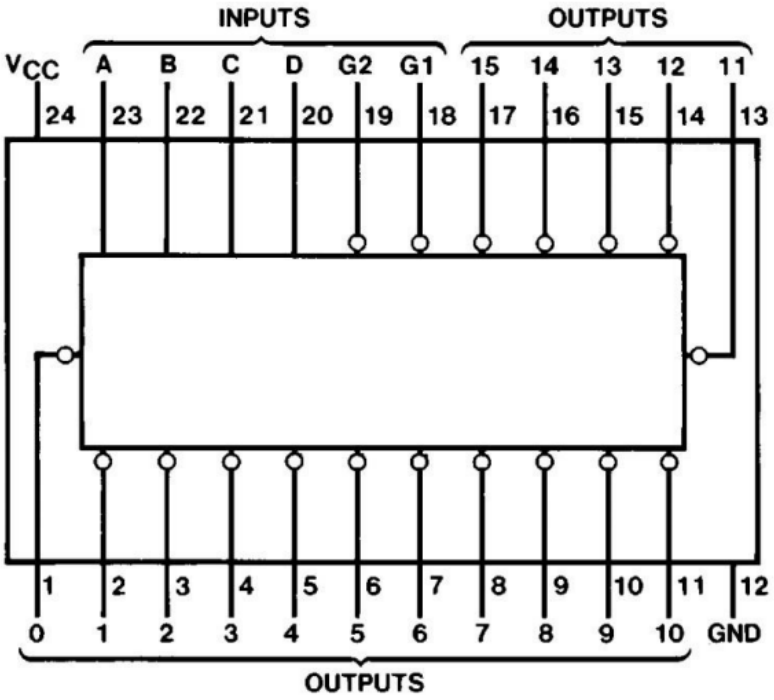
1.4 Now we still have S1 = 1, S0 = 0 but 1G = 1, then 1Y will be in a high-impedance state, which means Y1 is not connected to any inputs.

1.5 Since the signal 1D is assigned to output 1Y, then the signal that assigned to output 2Y is 2D.

Problem 2. Understanding the Decoder



Decoder Symbol for Logic Diagram



IC Pinout

2.1. Given G1 and G2 are two enable pins. For the decoder to function, the logic value we should assign to G1 and G2 is L= Low level or logic value 0.

2.2. In a decoder, basically we select one output (among all outputs) based on the inputs. Suppose we set the enable pins correctly, and we set A = 0, B = 1, C = 0, D = 1, the chosen output is 10.

2.3. Based on the IC pinout, the chosen output is low.

2.4. Given that the output number indicates the decimal value of the inputs, the input that should be considered the most significant bit is D.

2.5. Given that the output number indicates the decimal value of the inputs, the input that should be considered the least significant bit is A.

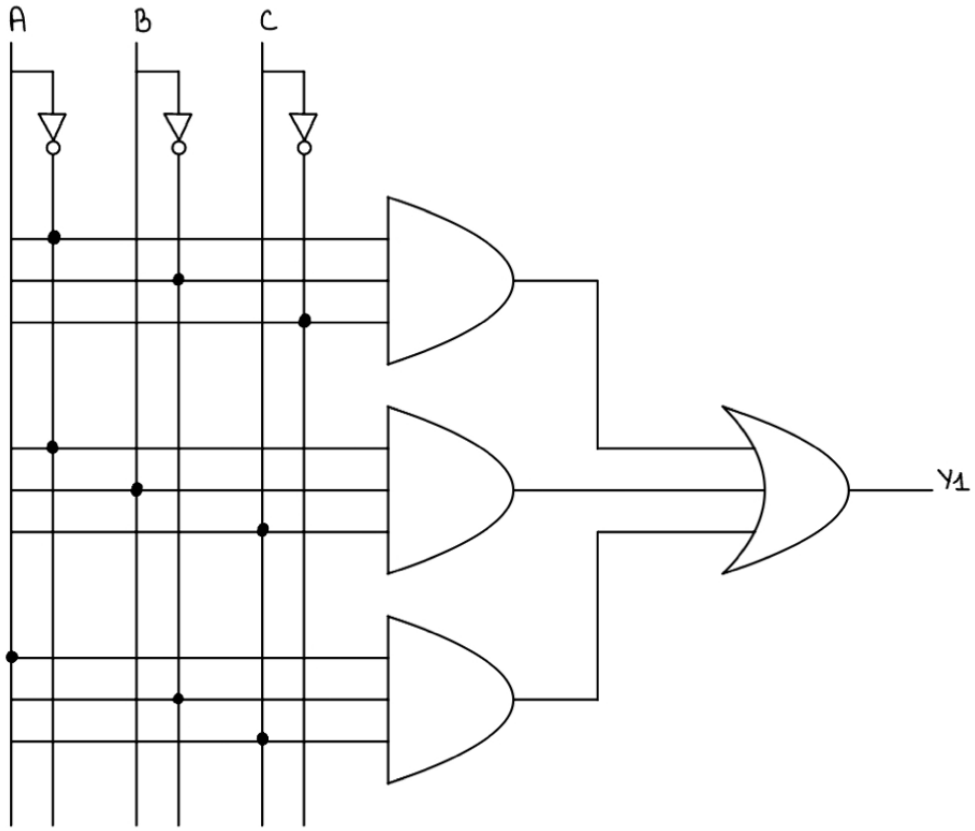
Problem 3. Using a Multiplexer to represent a Boolean equation.

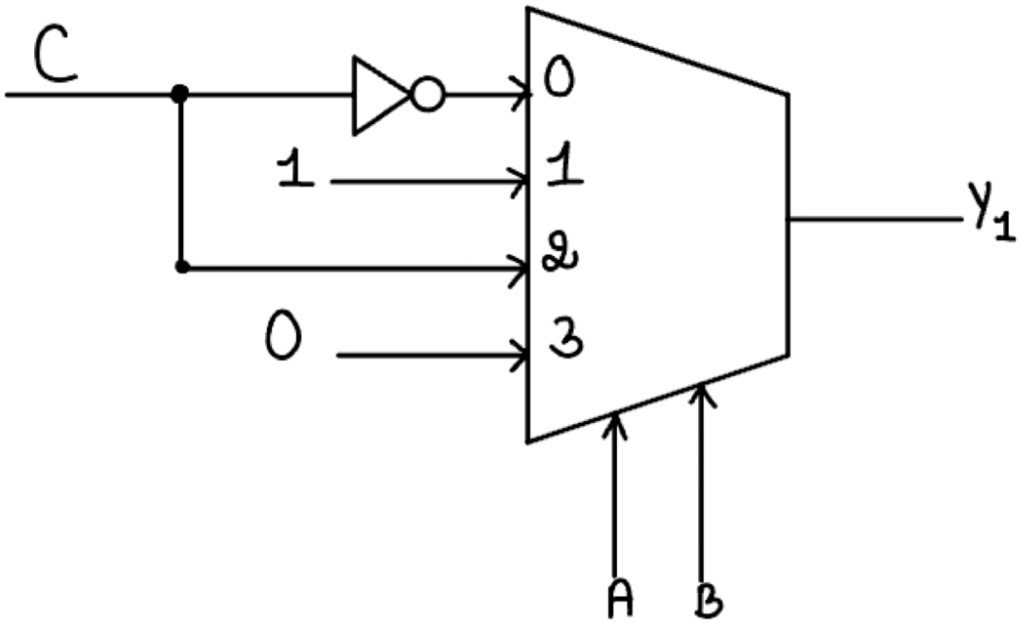
Implement the following Boolean function using 4:1 Multiplexer. Y1=A'B'C'+A'BC+AB'C

Truth Table

A	B	C	Y1
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Logic Diagram




C
0
1
2
3
1
0
y_1
A
B

Problem 4. Using a Decoder to represent a Boolean Equation.

Design a logic circuit that will output HIGH when the input is an odd number less than 8, and an even number greater than or equal to 8, and all inputs are smaller than 16. The input should be a 4-bit binary number. Design the circuit using a 4:16 decoder and other gates.

Truth Table

Inputs				Outputs																
A	B	C	D	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Y
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Logic Diagram