The University of Texas at Dallas
Department of Computer Science
CS 4141: Digital Systems Lab

Experiment #4 – Familiarization with Sequential Logic Circuits (Flip-Flops)

CS 4141 Laboratory 4, EXPERIMENT

Introduction

In previous laboratory exercises, we became familiar with logic gates which represented the six fundamental Boolean functions (NAND/AND, NOR/OR, XOR, and NOT) and the binary adder circuit. In this laboratory we will study another type of logic function namely ***sequential logic*** or flip-flop. Simple logic gates, such as we have studied so far, are referred to as *combinational logic*. Combinational logic circuits have outputs that depend only on their inputs. Thus, the output of a combinational logic circuit changes state as soon as the input stimulus is changed. Sequential logic circuits, on the other hand, may maintain an internal state, under certain conditions (and so long as power is available to the circuit) even when the input stimulus is changed. This means that sequential logic allows the circuit to have memory, to remember the previous value.

Objective

The purpose of Experiment #4 is to familiarize students with the functionality of the D and J-K flip-flops, and with the construction of a clocked flip-flop (an accumulator register) for the creation of a very tiny version of an Arithmetic Logic Unit (ALU).

Turn-In Check List

The laboratory has two items to grade.

1. Demonstrate the working circuits to the Lab Instructor (40 points)
2. ***Put supplies away correctly sorting and returning all chips. (10 points)***
3. Produce the Post-Lab Report (30 points)

Equipment List

The following components are required for this experiment:

- IDL-800a Digital Lab Station ("breadboard" unit with test equipment built-in power supply)
- Full Adder (Such as SN74LS283)
- D Flip-Flops (Such as SN74LS74)
- JK Flip-Flops (Such as SN74LS107)
- Breadboard wires (jumpers)

Experimental Procedure

Part 1. D Flip-Flop

- Plug in the 74LS74 D-type flip-flop and connect ground to pin 7 and 5V to pin 14 as usual. This is a two-circuit DIP. Referring to the 74LS74 pin-out diagram, choose one of the two D FFs on the chip and connect the input switches to the D and Preset inputs. Since the preset is negative-true logic input, make sure the switch is set to 1. Connect the pulse switches (the negative-true outputs) to the Clock and Clear inputs. The Q and Q outputs should be connected to LED inputs.
- Turn on the power. The D FF may power up in either state, so toggle the Clear pulse switch to initialize the circuit. After you do so, the Q LED should be off, and the Q LED on. Toggle the Preset switch (to low and back) and notice that the FF "sets" – that is, Q goes to 1 and its LED lights. The Preset switch allows an initial "on" state to be set before any clocked data is introduced into the FF, if the circuit requires an initial "on" condition. Toggle the Clear switch to reset the FF once more.
- Toggle the Clock pulse switch with the D input switch still set at 0. Notice that the FF does not change state. Now set D input to 1 (5V), and re-toggle Clock. Note that the D FF "sets," that is, as with the Preset input, the Q goes to one (its LED lights) and the Q goes to 0 (its LED turns off).
- The D FF can now be reset by setting the D input to 0 once more and re-pulsing Clock. Try these various inputs (Clock with D, Preset, Clear) and observe the circuit operation. Note that simultaneous switching of Clear and Preset results in both Q and Q going to 1 (both LEDs will light). This is a forbidden state and will not persist if either Preset or Clear is released. The reason we say that the state is "forbidden" is that it is unstable and is not a state in which the FF will remain when inputs are taken to their non-active states.
- Turn off the power and disconnect the circuit connections.

Part 2. JK Flip-Flop

- Plug in the 74LS107 J-K-type flip-flop and connect ground to pin 7 and 5V to pin 14 as usual. This is also a two-circuit DIP. Referring to the 74LS107 pin-out diagram, select one of the two JK FFs and connect the input switches to the J and K inputs. Connect the pulse switches (the negative-true outputs) to the Clock and Clear inputs. The Q and Q outputs should be connected to LED inputs.
- Turn on the power. The FF may power up in an undefined state, so toggle the Clear pulse switch to initialize the circuit. After you do so, the Q LED should be off, and the Q LED on.
- Both J and K should be set to 0. Now set J to 1 and toggle the Clock pulse switch. Notice that the FF changes state to the “set” state (Q = 1, Q = 0). Now set the J input to 0 and the K to 1 (5V), and re-toggle Clock. Note that, when FF “resets,” that is, the Q goes to 0 (its LED extinguishes) and the Q goes to 1 (its LED turns on).
- Now set the J-K inputs both to 1. Press Clock. Note that the FF “sets” again. Toggle Clock again
- the FF now resets. Press Clock several more times noting that with both J and K at 1, the J-K FF simply shifts to the reverse state when Clock is pulsed. Now switch both J and K to 0. When Clock is toggled, there is no change in the outputs. Now try to set various states while holding Clear low. Note that the FF remains “reset” as long as Clear is low, regardless of the state of Clock or J or K. This well-ordered design prevents the “forbidden state” of the R-S FFs – notice that regardless of the input, the J-K FF is in a stable state. Experiment with the J-K FF and get a feel for its operation and for the prevention of a forbidden state.
- Turn off the power and disconnect the circuit connections.

Part 3. Building ALU based 4-bit addition using two 74SL74 (4 D FF's) and a 4-bit adder:

- Build a 4-bit Register out of D flip-flops. This register should have the basic Clear pulse switch to clear the data and the Clock pulse switch input to give a clock pulse to the D flip-flop indicating the change of state. In this case, we have one input switch connected to input if each D flip-flop. All four outputs of the D flip-flops are connected to the 4 LEDs.

- Extend this implementation to perform the following ALU addition operation.
- Add A,B – This operation adds A and B and stores the result in A.
- This 4-bit register acts as an accumulator. This accumulator is connected with an adder and is performing the following task.
- The initial value of the accumulator is 0 and every time a clock pulse is given, it adds the current value of the accumulator (let's call it A) and a given 4-bit input B. The B input is provided using 4 input switches. Thus, the accumulator stores the addition of multiple 4-bit values provided to the ALU.
- Draw the pinout diagram, showing the connections of the pins on the IC chips. A pinout diagram should contain layouts of chips and the wiring combination. (Such as SN74lS283, SN74LS004, SN74LS586, SN74LS502) and with the correct wires on the correctly labeled pins.

Equipment Disassembly: The experimental procedure is complete. Please disassemble the circuit wiring, replace in the wires and replace all IC chips in their proper boxes. Make sure that your work area is clean.

For the Post-Lab Report (30 points)

- First, include your name, section, and date of the experiment.
- Second, include the title "Experiment 4 Post-Lab"
- If you were working with a partner on a lab station,
    - Then include your partners' name
- For each section
    - For the D Flip-Flop, write a paragraph about your observations. (7.5 points)
    - For the JK Flip-Flop, write a paragraph about your observations. (7.5 points)
    - For the tiny ALU, include a circuit diagram. That is, show the chips and the connecting wires. (30 points)
- Citations: If you are using software to draw your diagrams, identify the software.