The University of Texas at Dallas
Department of Computer Science
CS 4141: Digital Systems Lab

Experiment #2 – Familiarization with Multiplexers & Decoders; Construction of Circuits to Represent Given Boolean Expressions

CS 4151 Laboratory 2, EXPERIMENT

Introduction

In the previous laboratory exercises, we became familiar with logic gates which represented the Boolean functions: AND, OR, NOT, NAND, NOR, XOR. In this laboratory session we will become familiar with other logic gates which can be helpful in solving various problems in industry more efficiently, we will use them and solve the same Boolean expressions that we solved using the other gates.

Objective

The purposes Experiment #2 are to:

(1) familiarize students with the functionality of the Multiplexer (MUX)
(2) familiarize students with the functionality of the Decoder (DEC)

Turn-In Check List

1. Demonstrate the working circuits to the Lab Instructor (40 points)
2. ***Put supplies away correctly sorting and returning all chips. (10 points)***
3. Produce the Post-Lab Report (30 points)

Equipment List

The following components are required for this experiment.

- IDL-800a Digital Lab Station ("breadboard" unit with test equipment built-in power supply)
- AND gate IC Chip (Such as SN74LS08)
- NOT gate IC Chip (Such as SN74LS04)
- OR gate IC Chip (Such as SN74LS32)
- NAND gate IC Chip (Such as SN74LS00)
- NOR gate IC Chip (Such as SN 74LS02)
- XOR gate IC Chip (Such as SN 74LS86)
- Breadboard wires (jumpers)
- 4:1 Multiplexer (such as SN 74LS153)
- 3:8 Decoder (such as SN 74LS138)

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Experimental Procedure:

Note: Multiplication represents an AND gate. Addition represents an OR gate, and an apostrophe represents a negation. Exclusive Disjunction (⊕) represents an XOR gate.

For example:
Y_0=A'•B+C'•D would represent Y = (NOT A AND B) OR (NOT C AND D)

Part 1: Solving the Boolean Expressions using a 4:1 Multiplexer.

For each equation, show the truth table and the logic diagram. A logical diagram should contain block notations (such as Full Adder, D Flip-Flop, Decoder, Multiplexer) and gate symbols (such as AND, OR, and NOT).

Y_1=A'B+AB'+AC
Y_2=A'B'C+A'BC+AB'C'+ABC'

Part 2: Solving a problem using a 3:8 Decoder.

A Full Adder has two outputs, that is two equations: the Carry and the Sum.

Show the truth table and the logic diagram for Implementing a Full Adder using a 3:8 Decoder and appropriate logic gates, A logical diagram should contain block notations (such as Full Adder, D Flip-Flop, Decoder, Multiplexer) and gate symbols (such as AND, OR, and NOT).

Equipment Disassembly

The experimental procedure is complete. Please disassemble the circuit wiring, wires and all IC chips in their proper boxes. Make sure that your work area is clean.

For the Post-Lab Report

- First, include your name, section, and date of the experiment.
- Second, include the title "Experiment 2 Post-Lab"
- If you were working with a partner on a lab station,
  - Then include your partners' name.
- For each equation in section 3, include.
  - Equation Y1, its truth table, and its logic diagram (10 Points)
  - Equation Y2, its truth table, and its logic diagram (10 points)
  - The Truth Table for the Full Adder, and the Logic Diagram for the Full Adder using the Decoder (10 points)
- Citations: If you are using software to draw your diagrams, identify the software.