FPGA DESIGN

Homework 5
Report

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1. Problem1

- Design introduction

  - Interface between software and hardware

Main.c 引入專案必要的標頭文件，其中引入了 xil_printf.h, xil_io.h 和 xparameters.h，提供 Zynq 的開發板上的輸出、輸入輸出操作以及相關參數和定義等功能。定義 unsigned-32 位元整數變數，用於儲存計算和輸入輸出數值及位址。依據題要求跟硬體 bram0 要指定資料到 DSP，並由 Main.c 指定 Controller 傳指令給 DSP 做指定的運算，運算完後寫入 bram1 後把 write enable 拉低。最後 Main.c 將 bram1 前 32 個地址的資料呈列。即為 Step 過程。Step1 後，依序號加一的平方值寫給 bram1 後，Step2 完成 print 辛普森圖案後結束。

  - Instruction format

inst[30:27]	inst[30:27]	inst[26:20]	inst[19:15]	inst[14:10]	inst[9:5]	inst[4:0]
read enable	dsp_alumode	dsp_opmode	dsp_inmode	bram1_Waddr	bram1_Raddr	bram0_Raddr

bram0_Raddr ： 輸入讀取 bram0 資料的地址。

Bram1_Raddr ： 輸入讀取 bram1 資料的地址。

Bram1_Waddr ： 輸入寫入 bram1 資料的地址。

dsp_inmode ： 選擇多工器輸入值的控制訊號。

dsp_opmode ： 選擇多工器輸出值的控制訊號。

dsp_alumode ： 控制 DSP 邏輯運算模式的控制訊號。

read enable ： 輸入是否寫入的控制訊號。

以下為 Main.c 過程中 inst 值的變化。

		inst[30:27]	inst[30:27]	inst[26:20]	inst[19:15]	inst[14:10]	inst[9:5]	inst[4:0]
		read enable	dsp_alumode	dsp_opmode	dsp_inmode	bram1_Waddr	bram1_Raddr	bram0_Raddr
step1	1	1	0000	0110011	00000	00011	00010	00000
step1	2	0	0000	0110011	00000	00011	00010	00000
step1	3	1	0000	0000101	10001	00111	00011	01011
step1	4	0	0000	0000101	10001	00111	00011	01011
step1	5	1	0000	0110101	10001	01010	00111	11111
step1	6	0	0000	0110101	10001	01010	00111	11111
step1	7	1	0011	0110101	10001	01101	00110	00001
step1	8	0	0011	0110101	10001	01101	00110	00001
step1	9	1	0001	0110101	10001	01111	11111	00000
step1	10	0	0001	0110101	10001	01111	11111	00000
step2	11	1	0000	0000101	10001	10000	00010	00000
step2	12	0	0000	0000101	10001	10000	00010	00000
step2	13	1	0000	0000101	10001	10001	01011	00011
step2	14	0	0000	0000101	10001	10001	01011	00011
step2	15	1	0000	0110101	10001	10010	00111	11111
step2	16	0	0000	0110101	10001	10010	00111	11111
step2	17	1	0011	0110101	10001	10011	00110	00001
step2	18	0	0011	0110101	10001	10011	00110	00001
step2	19	1	0001	0110101	10001	10100	11111	00000
step2	20	0	0001	0110101	10001	10100	11111	00000

1, 2 → BRAM1[3] <= BRAM0[0] * BRAM1[2]

3, 4 → BRAM1[7] <= BRAM0[11] * BRAM1[3]

5, 6 → BRAM1[10] <= BRAM0[31] * BRAM1[7] + C

7,8 → BRAM1[13] <= C - BRAM0[1] * BRAM1[6]

9,10 → BRAM1[15] <= BRAM0[0] * BRAM1[31] - C - 1

11,12 → BRAM1[16] <= BRAM0[0] * BRAM1[2]

13,14 → BRAM1[17] <= BRAM0[11] * BRAM1[3]

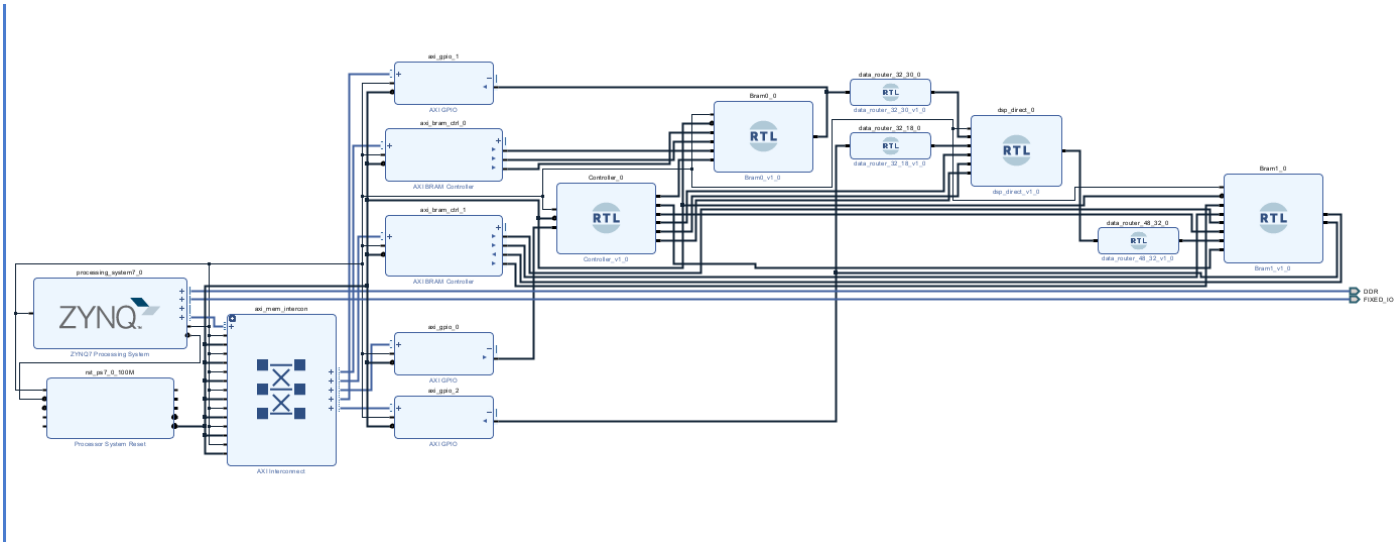
15,16 → BRAM1[18] <= BRAM0[31] * BRAM1[7] + C

17,18 → BRAM1[19] <= C - BRAM0[1] * BRAM1[6]

19,20 → BRAM1[20] <= BRAM0[0] * BRAM1[31] - C - 1

- Block Design

全



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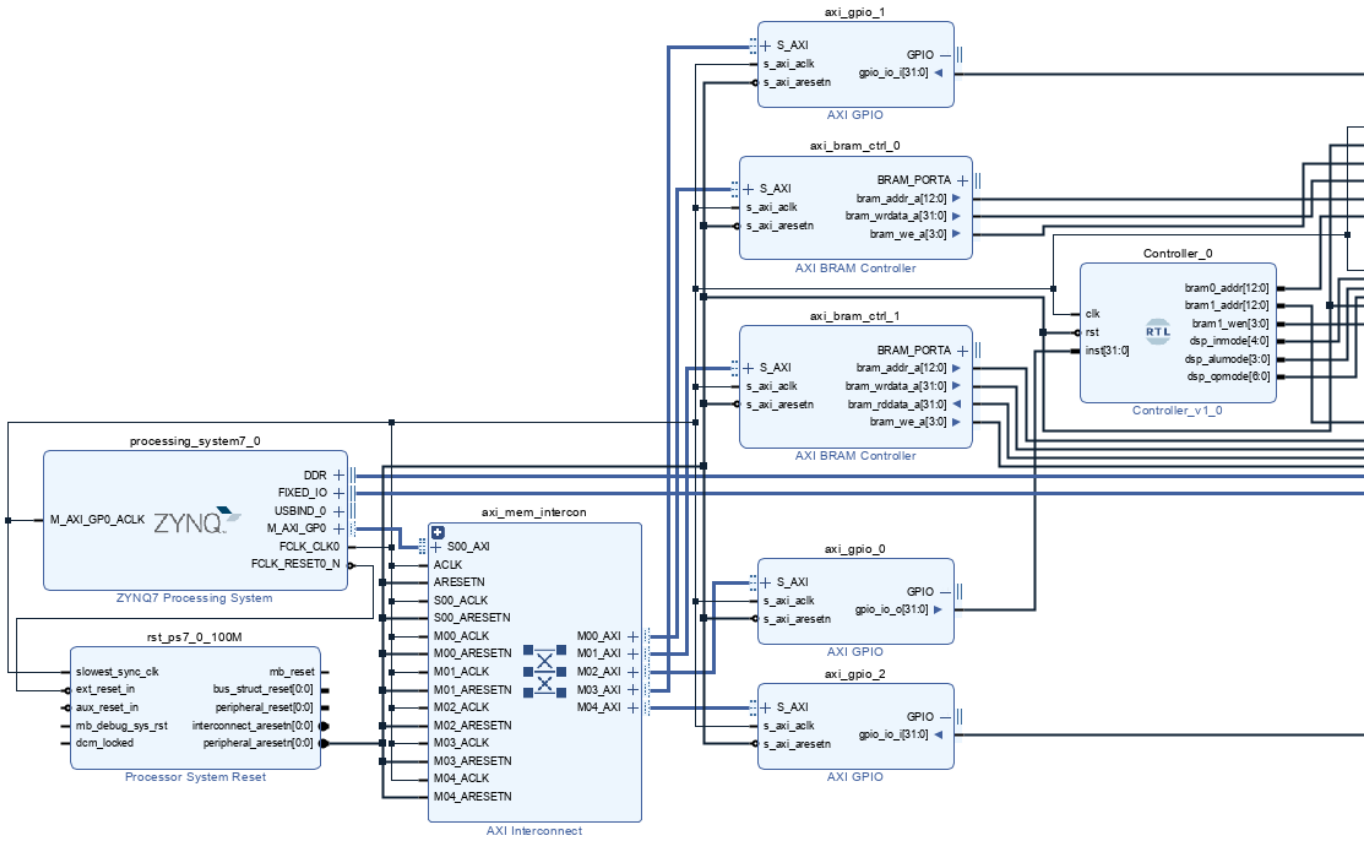

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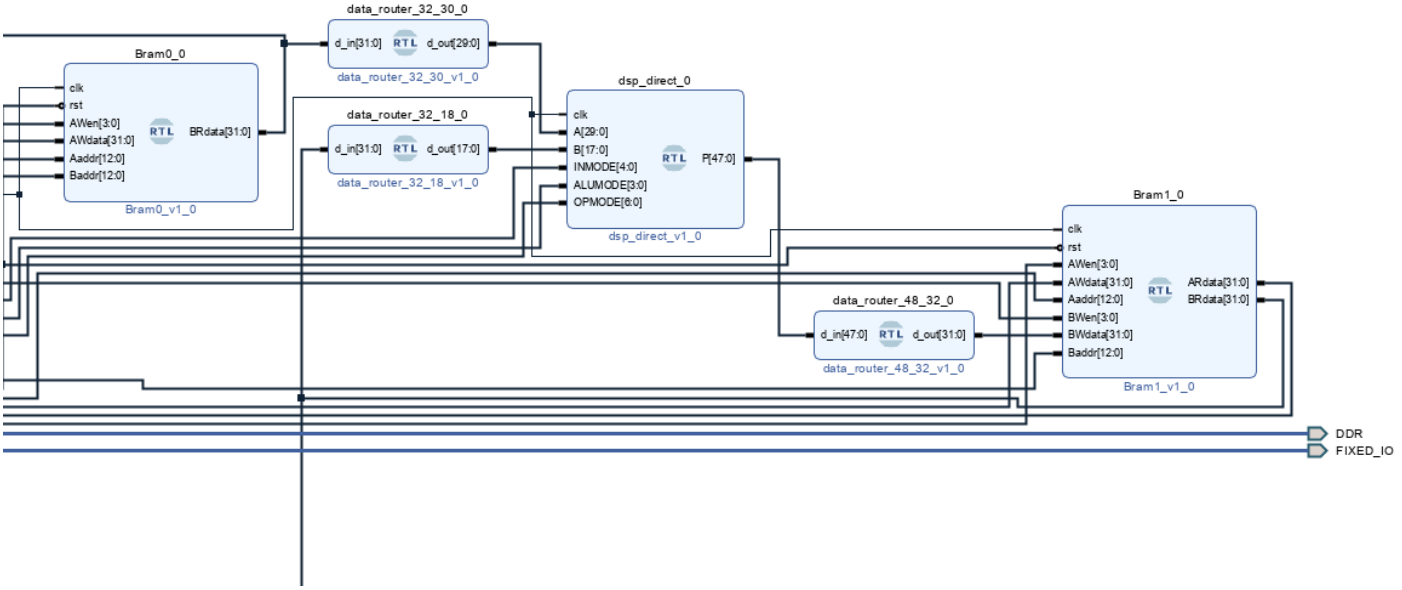

- Simulation result

```
step 1.
BRAM1[0] = 23
BRAM1[1] = 1
BRAM1[2] = 1201
BRAM1[3] = 27623
BRAM1[4] = 0
BRAM1[5] = 0
BRAM1[6] = 531
BRAM1[7] = 15403c9
BRAM1[8] = 0
BRAM1[9] = 0
BRAM1[10] = 8ad37a
BRAM1[11] = ffffff23
BRAM1[12] = 0
BRAM1[13] = 94fe3
BRAM1[14] = 0
BRAM1[15] = fffb584d
BRAM1[16] = 0
BRAM1[17] = 0
BRAM1[18] = 0
BRAM1[19] = 0
BRAM1[20] = 0
BRAM1[21] = 0
BRAM1[22] = 0
BRAM1[23] = 0
BRAM1[24] = 0
BRAM1[25] = 0
BRAM1[26] = 0
BRAM1[27] = 0
BRAM1[28] = 0
BRAM1[29] = 0
BRAM1[30] = 0
BRAM1[31] = 2236
```

```
step 2.
BRAM1[0] = 23
BRAM1[1] = 1
BRAM1[2] = 1201
BRAM1[3] = 27623
BRAM1[4] = 0
BRAM1[5] = 0
BRAM1[6] = 531
BRAM1[7] = 15403c9
BRAM1[8] = 0
BRAM1[9] = 0
BRAM1[10] = 8ad37a
BRAM1[11] = ffffff23
BRAM1[12] = 0
BRAM1[13] = 94fe3
BRAM1[14] = 0
BRAM1[15] = fffb584d
BRAM1[16] = 1201
BRAM1[17] = ff2273b0
BRAM1[18] = 187914
BRAM1[19] = 94050
BRAM1[20] = fff6cd21
BRAM1[21] = 0
BRAM1[22] = 0
BRAM1[23] = 0
BRAM1[24] = 0
BRAM1[25] = 0
BRAM1[26] = 0
BRAM1[27] = 0
BRAM1[28] = 0
BRAM1[29] = 0
BRAM1[30] = 0
BRAM1[31] = 2236
```

2. Problem2

PYNQ-Z2 上共有多少個 DSP48E1 Slice？

From the reference ,the number of RAMB36E1 in z-7020 is 220.

Reference:

https://docs.xilinx.com/v/u/en-US/zynq-7000-product-selection-guide

Zynq-7000 SoC Features

- Dual ARM® Cortex™-A9 MPCore™ with CoreSight™
- 32 KB Instruction, 32 KB Data per processor L1 Cache
- 512 KB unified L2 Cache
- 256 KB On-Chip Memory
- 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO
- 2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO on-chip peripherals
- 85K logic cells (13300 logic slices, each with four 6-input LUTs and 8 flip-flops)
- 630 KB of fast block RAM
- Four clock management tiles, each with phase-locked loop (PLL)
- 220 DSP slices
- Internal clock speeds exceeding 450MHz
- 2x 12 bit, 1 MSPS On-chip analog-to-digital converter (XADC)

	Cost-Optimized Devices					
Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020
Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020
Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz		
Processor Extensions	NEON™ SIMD Engine and Single/Double Precisi					
L1 Cache	32KB Instruction, 32KB Dat					
L2 Cache	512KB					
On-Chip Memory	256KB					
External Memory Support[2]	DDR3, DDR3L, DDR2					
External Static Memory Support[2]	2x Quad-SPI, NAN					
DMA Channels	8 (4 dedicated t					
Peripherals	2x UART, 2x CAN 2.0B, 2x I2C,					
Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Giga					
Security[3]	RSA Authentication of First S AES and SHA 256b Decryption and Aut					
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x A 4x AXI 64b/32b M AXI 64b ACI 16 Interrupt					
7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7
Logic Cells	23K	55K	65K	28K	74K	85K
Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200
Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400
Total Block RAM (# 36Kb Blocks)	1.8Mb (50)	2.5Mb (72)	3.8Mb (107)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)
DSP Slices	66	120	170	80	160	220
PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—