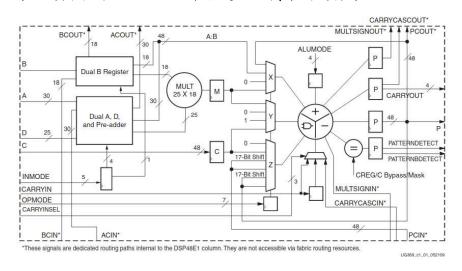
(2) Simple compute system use DSP module

甲、摘要

利用 Verilog Template 呼叫 DSP48E1 及 RAMB36E1 module, 並自行設定其中的 attributes, 來搭建一個簡單的運算系統。



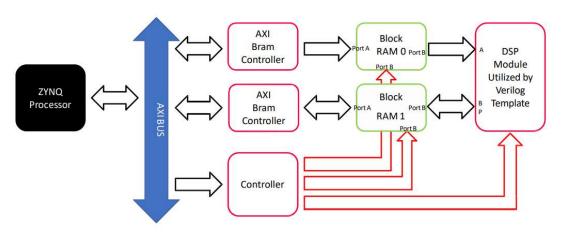
圖一、DSP48E1內部結構

乙、想法

自行建立 Instruction format, 並根據指令的各種 opmode 和 Bram address 來進行操作。最後用 Block design 搭建整個系統,並用 embedded C 在 Vitis IDE 上與 PL 端作互動。

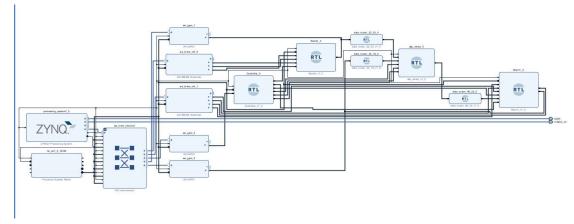
inst[30:27]	inst[30:27]	inst[26:20]	inst[19:15]	inst[14:10]	inst[9:5]	inst[4:0]
read enable	dsp_alumode	dsp opmode	dsp_inmode	bram1 Waddr	bram1 Raddr	bram0 Raddr

圖二、Instruction format



圖三、系統方塊圖

丙、結果



圖四、Block design

```
step 2.
BRAM1[0] = 23
BRAM1[0] = 23
                                       BRAM1[1] = 1
BRAM1[1] = 1
BRAM1[2] = 1201
                                       BRAM1[2] = 1201
                                       BRAM1[3] = 27623
BRAM1[4] = 0
BRAM1[3] = 27623
BRAM1[4] = 0
BRAM1[5] = 0
                                       BRAM1[5]
                                       BRAM1[6] = 531
BRAM1[7] = 15403c9
BRAM1[6] = 531
BRAM1[7] = 15403c9
                                       BRAM1[8] = 0
BRAM1[8] = 0
BRAM1[9] = 0
                                       BRAM1[9] = 0
BRAM1[10] = 8ad37a
BRAM1[10] = 8ad37a
BRAM1[11] = ffffff23
BRAM1[12] = 0
                                       BRAM1[11] = ffffff23
                                       BRAM1[12]
                                        BRAM1[13]
                                                    = 94fe3
BRAM1[13] = 94fe3
                                       BRAM1[14] = 0
BRAM1[14] = 0
BRAM1[15] = fffb584d
                                        BRAM1[15] = fffb584d
                                        BRAM1[16] = 1201
BRAM1[16] = 0
                                       BRAM1[17] = ff2273b0
BRAM1[17] = 0
BRAM1[18] = 0
                                       BRAM1[18]
                                       BRAM1[19]
BRAM1[20]
                                                    = 94050
BRAM1[19]
                                                    = fff6cd21
BRAM1[20]
                                        BRAM1[21]
BRAM1[21]
                                       BRAM1[22]
BRAM1[23]
BRAM1[22] = 0
                                                     = 0
BRAM1[23]
                                        BRAM1 [24]
BRAM1[24]
                                       BRAM1 [25]
BRAM1 [26]
                                                     = 0
BRAM1[25]
             = 0
BRAM1[26]
                                        BRAM1[27]
BRAM1[27]
BRAM1[28]
                                       BRAM1[28]
BRAM1[29]
                                                    = 0
             = 0
BRAM1[29] = 0
                                       BRAM1[30] = 0
BRAM1[30] = 0
BRAM1[31] = 2236
                                        BRAM1[31] = 2236
```

		inst[30:27]	inst[30:27]	inst[26:20]	inst[19:15]	inst[14:10]	inst[9:5]	inst[4:0]
		read enable	dsp_alumode	dsp_opmode	dsp_inmode	bram1_Waddr	bram1_Raddr	bram0_Raddr
step1	1	1	0000	0110011	00000	00011	00010	00000
step1	2	0	0000	0110011	00000	00011	00010	00000
stepl	3	1	0000	0000101	10001	00111	00011	01011
step1	4	0	0000	0000101	10001	00111	00011	01011
step1	5	1	0000	0110101	10001	01010	00111	11111
step1	6	0	0000	0110101	10001	01010	00111	11111
step1	7	1	0011	0110101	10001	01101	00110	00001
step1	8	0	0011	0110101	10001	01101	00110	00001
step1	9	1	0001	0110101	10001	01111	11111	00000
step1	10	0	0001	0110101	10001	01111	11111	00000
step2	11	1	0000	0000101	10001	10000	00010	00000
step2	12	0	0000	0000101	10001	10000	00010	00000
step2	13	1	0000	0000101	10001	10001	01011	00011
step2	14	0	0000	0000101	10001	10001	01011	00011
step2	15	1	0000	0110101	10001	10010	00111	11111
step2	16	0	0000	0110101	10001	10010	00111	11111
step2	17	1	0011	0110101	10001	10011	00110	00001
step2	18	0	0011	0110101	10001	10011	00110	00001
step2	19	1	0001	0110101	10001	10100	11111	00000
step2	20	0	0001	0110101	10001	10100	11111	00000

圖五六七、利用 Vitis IDE 完成系統驗證