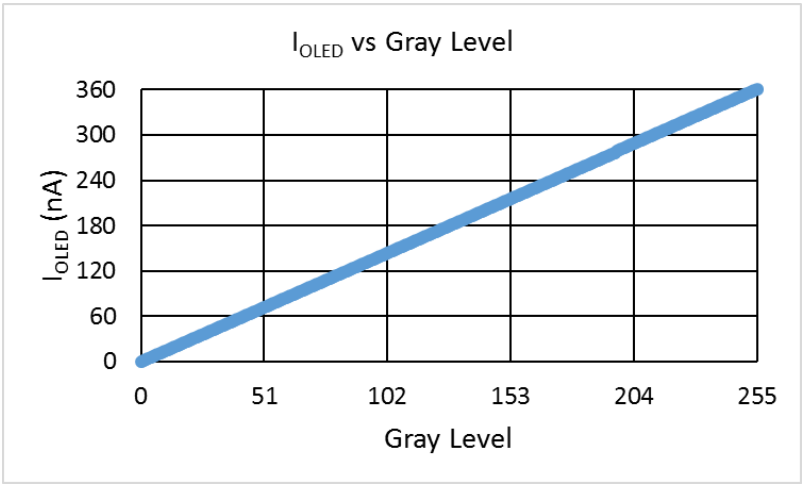
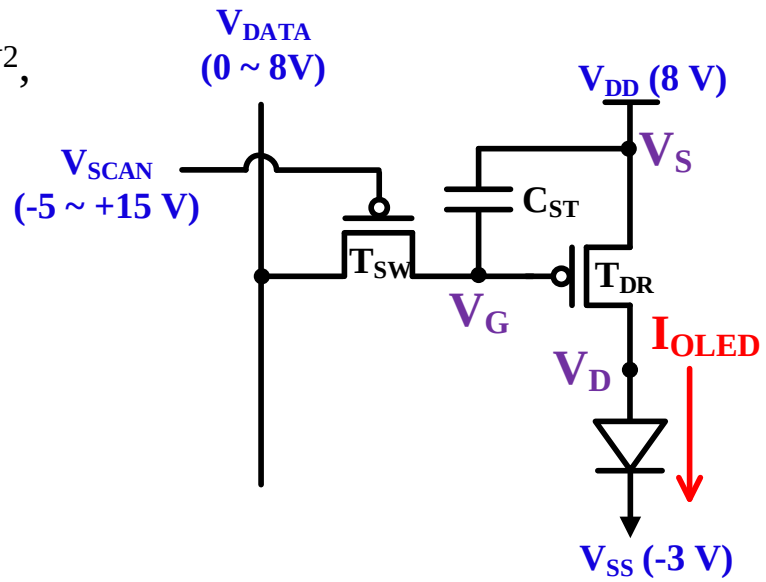
1. FPGA Design with Verilog for AMOLED

1. 2T1C AMOLED Pixel Circuit:

I_{OLED_Max} = 360 nA, I_{OLED_Min} = 0 nA, K = 10 nA/V^2,

$|V_{TH}|$ = 1.5 V, γ = 1





$$I_{OLED\_GL} = I_{OLED\_Max} \times \left(\frac{Gray\ Level}{255}\right)^{\gamma}$$

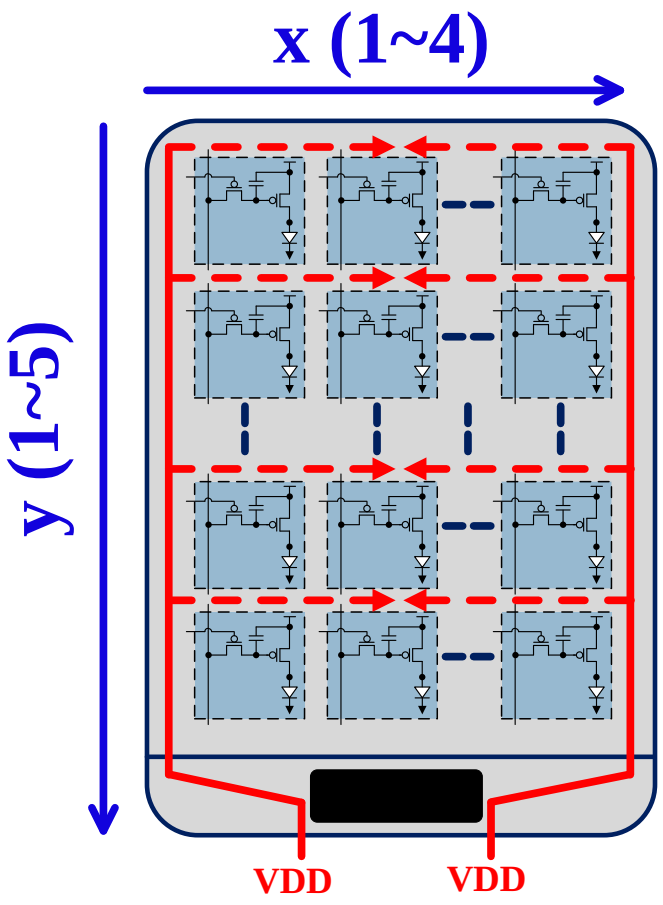
OLED current equation:

$$I_{OLED} = K(V_{DD} - V_{DATA} - |V_{TH}|)^2$$

$$V_{DATA} = V_{DD} - |V_{TH}| - \sqrt{\frac{I_{OLED}}{K}}$$

1. FPGA Design with Verilog for AMOLED

2. AMOLED V_{TH} Compensation



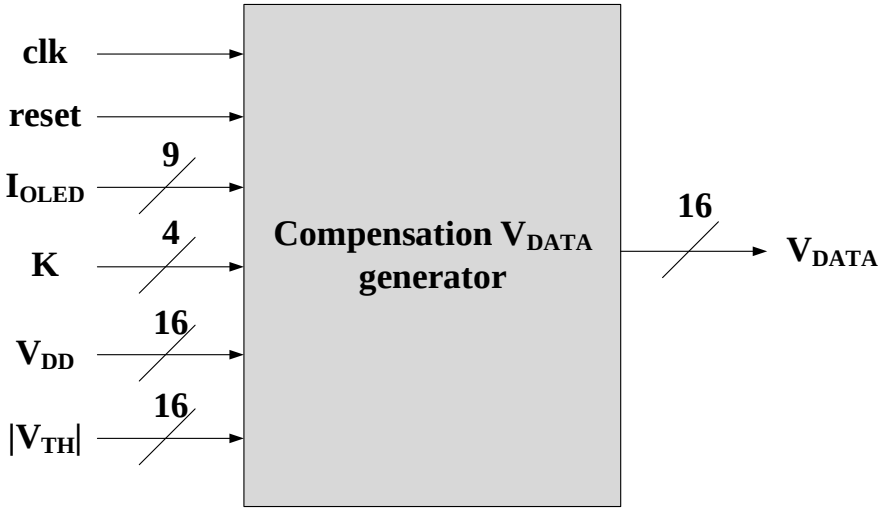
TFTs suffer from V_{TH} variations, causing significant non-uniform driving current levels in each pixel.

Given $|V_{TH}|$ variation for each pixel:
(Unit: V)

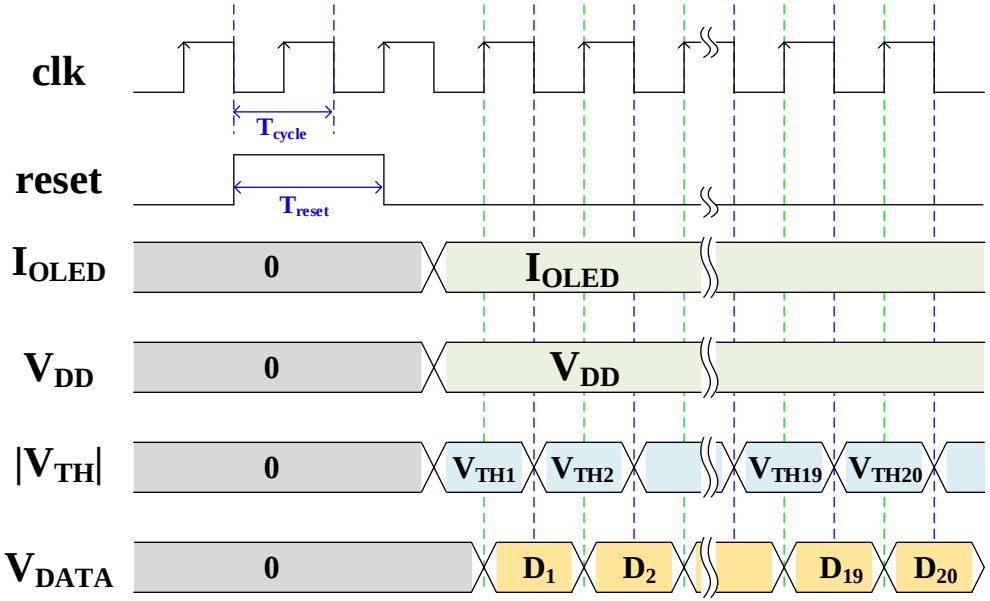
0	-0.1	-0.2	+0.2
-0.1	-0.1	+0.2	-0.2
+0.3	+0.1	-0.2	-0.3
+0.4	-0.2	+0.3	-0.4
+0.5	-0.5	+0.3	+0.3

1. FPGA Design with Verilog for AMOLED

3. Use Verilog to implement compensation V_{DATA} generator



Block diagram



Timing diagram

integer	floating number
8 bits	8 bits

Data format for V_{DD}, $|V_{TH}|$, V_{DATA}

1. FPGA Design with Verilog for AMOLED

4. I/O Interface

Signal Name	I/O	Width	Description
clk	I	1	Clock for the computational system
reset	I	1	Reset the state of the computational system when it asserts
IOLED	I	9	OLED current, which is composed of 9 bits unsigned integer
K	I	4	K coefficient, which is composed of 4 bits unsigned integer
VDD	I	16	Power supply VDD, which is composed of 8 bits unsigned integer and 8 bits floating number
|VTH|	I	16	Absolute value of threshold voltage, which is composed of 8 bits unsigned integer and 8 bits floating number
VDATA	O	16	Computed output data voltage, which is composed of 8 bits unsigned integer and 8 bits floating number

1. FPGA Design with Verilog for AMOLED

- i. Considering the given V_{TH} variations, please calculate the value of V_{DATA} for each pixel circuit to generate uniform I_{OLED}= 360 nA.

- ii. Following the above questions, please calculate the value of V_{DATA} for each pixel circuit to generate uniform I_{OLED}= 250, 160, 90, and 40 nA.

- iii. Please briefly describe your code.

➢ Please modify the COMP_tb.v to simulate different I_{OLED} and V_{DATA}

```
4   `define VDATA_dat "./VDATA_360nA.txt" //change verified VDATA here!
73      IOLED = 9'd360; // change your IOLED here!
```

1. FPGA Design with Verilog for AMOLED

- Simulation results in transcript window of ModelSim

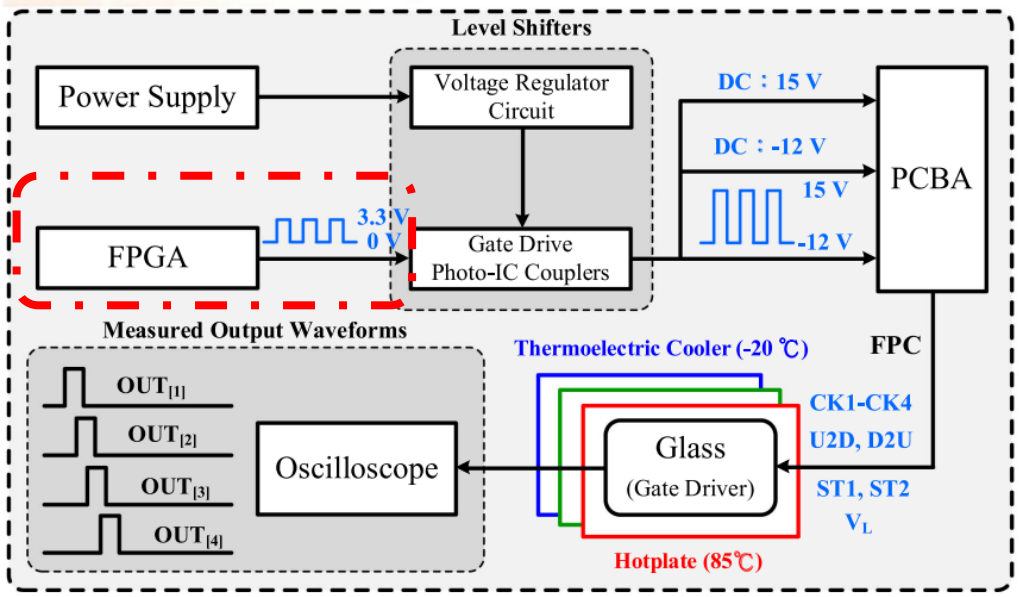
Pass	Error

```
VSIM 52> run -all
#           0 VDATA is correct 0480
#           1 VDATA is correct 049a
#           2 VDATA is correct 04b3
#           3 VDATA is correct 044d
#           4 VDATA is correct 049a
#           5 VDATA is correct 049a
#           6 VDATA is correct 044d
#           7 VDATA is correct 04b3
#           8 VDATA is correct 0433
#           9 VDATA is correct 0466
#          10 VDATA is correct 04b3
#          11 VDATA is correct 04cd
#          12 VDATA is correct 041a
#          13 VDATA is correct 04b3
#          14 VDATA is correct 0433
#          15 VDATA is correct 04e6
#          16 VDATA is correct 0400
#          17 VDATA is correct 0500
#          18 VDATA is correct 0433
#          19 VDATA is correct 0433
# ------------------------------------------------
#
# All VDATA have been generated successfully!
#
# --------------------PASS--------------------
#
# ------------------------------------------------
```

```
VSIM 54> run -all
#           0 VDATA is error 0680, correct is 0480, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=0180
#           1 VDATA is error 069a, correct is 049a, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=0166
#           2 VDATA is error 06b3, correct is 04b3, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=014d
#           3 VDATA is error 064d, correct is 044d, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=01b3
#           4 VDATA is error 069a, correct is 049a, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=0166
#           5 VDATA is error 069a, correct is 049a, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=0166
#           6 VDATA is error 064d, correct is 044d, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=01b3
#           7 VDATA is error 06b3, correct is 04b3, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=014d
#           8 VDATA is error 0633, correct is 0433, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=01cd
#           9 VDATA is error 0666, correct is 0466, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=019a
#          10 VDATA is error 06b3, correct is 04b3, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=014d
#          11 VDATA is error 06cd, correct is 04cd, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=0133
#          12 VDATA is error 061a, correct is 041a, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=01e6
#          13 VDATA is error 06b3, correct is 04b3, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=014d
#          14 VDATA is error 0633, correct is 0433, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=01cd
#          15 VDATA is error 06e6, correct is 04e6, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=011a
#          16 VDATA is error 0600, correct is 0400, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=0200
#          17 VDATA is error 0700, correct is 0500, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=0100
#          18 VDATA is error 0633, correct is 0433, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=01cd
#          19 VDATA is error 0633, correct is 0433, when IOLED= 40 nA, K=10 nA/v2, VDD=0800, VTH=01cd
# ------------------------------------------------
#
# There are          20 errors!
#
# ------------------------------------------------
```

2. Waveform Simulation

1. Measurement platform for glass sample



Signals provided by the power supplies

- Gate Driver Circuit
  - V_{GH} and V_{GL}
- Pixel Circuit
  - VDD, VSS, V_{REF} …

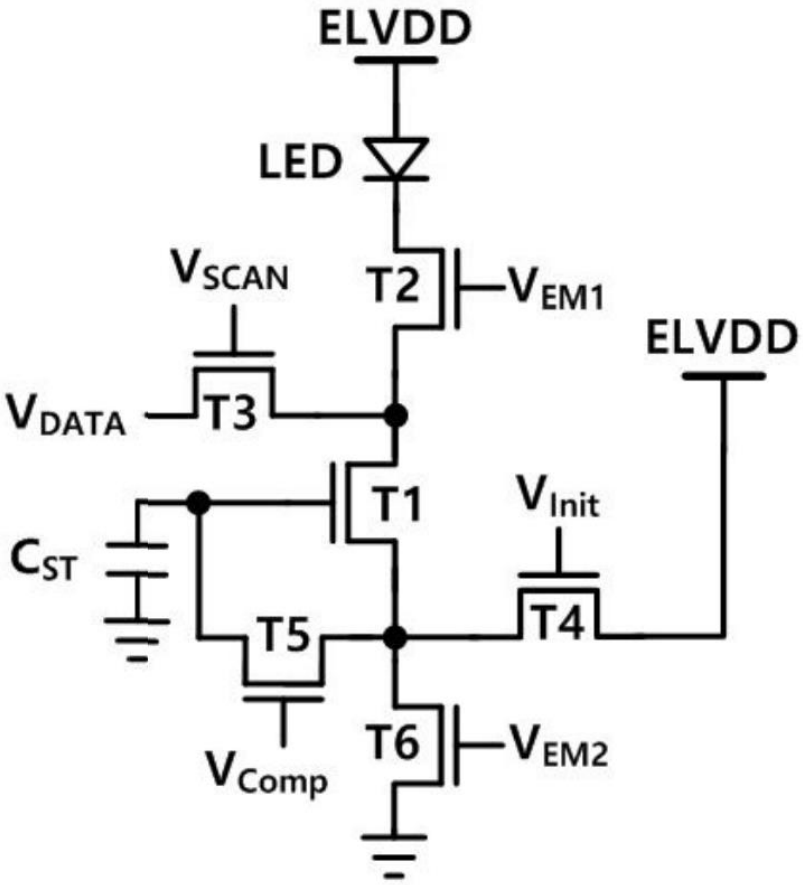
Signals provided by the FPGA board

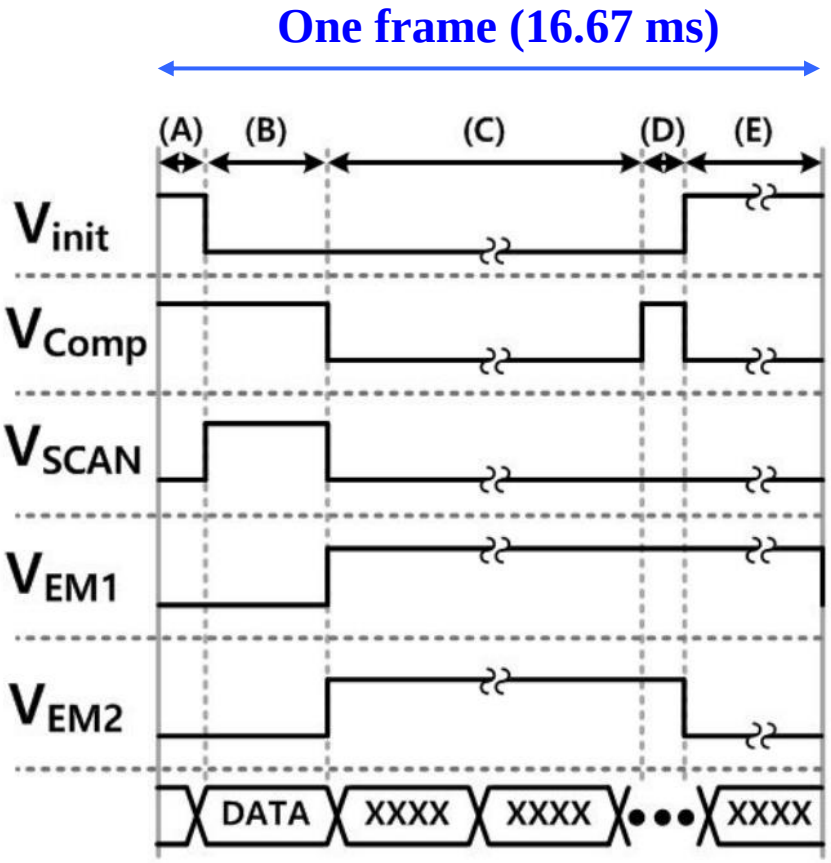
- Gate Driver Circuit
  - Start pulse and clock signals
- Pixel Circuit
  - Scan signals

C.-L. Lin *et al.*, "A Pre-Bootstrapping Method for Use in Gate Driver Circuits to Improve the Scan Pulse Delay of High-Resolution TFT-LCD Systems," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 8, pp. 7015-7024, Aug. 2020

2. Waveform Simulation

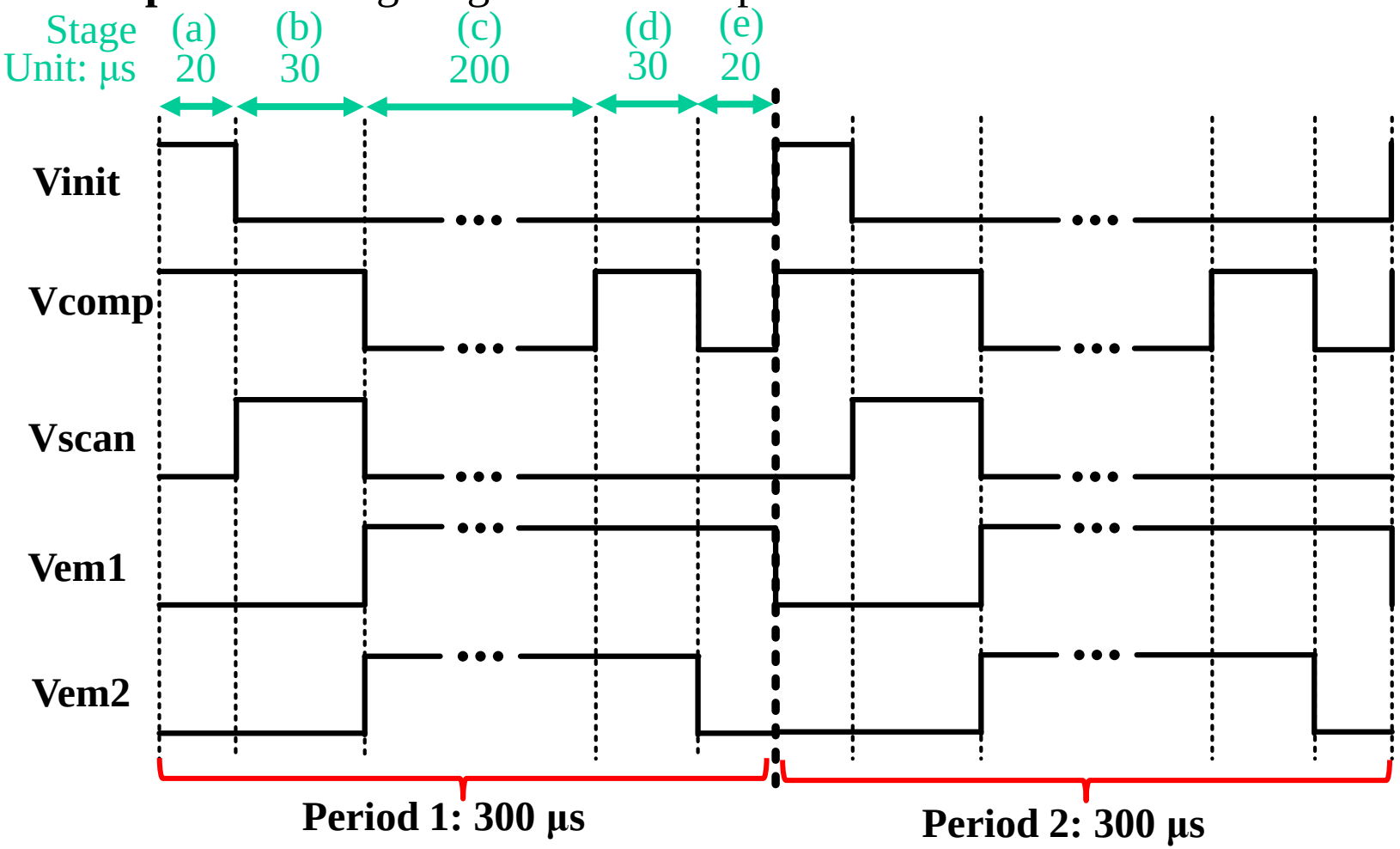
2. 6T1C pixel circuit and timing diagram





2. Waveform Simulation

3. **Simplified** timing diagram of 6T1C pixel circuit



2. Waveform Simulation

- i. Generate the simplified waveforms of 6T1C circuit by utilizing the 100M Hz clock provided by FPGA.

  Modify “waveform .v” to generate the waveforms.

  Verify your results by using “waveform_tb.v”.

  Upload your code and screen captures.

截圖 1. **6**個period的波形(Use zoom full) **2.** 請將cursor對齊1550 us，並放大截圖證明波形誤差在0.1 us內(vcomp, vscan的falling edge 以及 vem1, vem2的rising edge)。

- ii. Please decrease the frequency to half without modifying the duration of stages (a), (b), (d), and (e).

截圖 1. **3**個period的波形(Use zoom full) **2.** 請將cursor對齊1250 us，並放大截圖證明波形誤差在0.1 us內(vcomp, vscan的falling edge 以及 vem1, vem2的rising edge)。

- iii. Please briefly describe your code.