Ex.

1. 使用方法:
   - Include IP

   // synopsys translate_off

   .

   . `include"想使用的 IP.v"

   .

   // synopsys translate_on

   - Build Instance

     Ex.乘法器:

     DW_mult_seq

     #(.a_width(8), .b_width(8), .tc_mode(1), .num_cyc(16), .rst_mode(1), .inp

     ut_mode(0), .output_mode(0), .early_start(0))

     mult1(clk, rst, mult1_hold, mult1_start, mult1_a, mult1_b, mult1_complete, mult1_product);

2. 使用指令:
   - 以 ncverilog 編譯器及乘法器 IP 為例(建議使用 VCS 因為波型與 nWave 不太相容)

     ncverilog -sv tb.sv +ncmaxdelays -y +($DW IP Path) +libext+DW_mult_seq.v +incdir+($DW IP Path)
   - IP 參考文件位置 : /……/Synopsys/synthesis/dw/doc

Application Specific: Control Logic (Overview)	
DW_arb_2t	Two-Tier Arbiter with Dynamic/Fair-Among-Equal Scheme
DW_arb_dp	Arbiter with Dynamic Priority Scheme
DW_arb_fcfs	Arbiter with First-Come-First-Served Priority Scheme
DW_arb_rr	Arbiter with Round Robin Priority Scheme
DW_arb_sp	Arbiter with Static Priority Scheme
Datapath: Arithmetic Components (Overview)	
DW01_absval	Absolute Value
DW01_add	Adder
DW01_addsub	Adder-Subtractor
DW01_ash	Arithmetic Shifter
DW01_bsh	Barrel Shifter
DW01_cmp2	2-Function Comparator
DW01_cmp6	6-Function Comparator
DW01_csa	Carry Save Adder
DW01_dec	Decrementer
DW01_inc	Incrementer
DW01_incdec	Incrementer-Decrementer
DW01_satrnd	Arithmetic Saturation and Rounding Logic
DW01_sub	Subtractor
DW02_mac	Multiplier-Accumulator
DW02_mult	Multiplier

DW02_mult	Multiplier
DW02_multp	Partial Product Multiplier
DW02_mult_2_stage	Two-Stage Pipelined Multiplier
DW02_mult_3_stage	Three-Stage Pipelined Multiplier
DW02_mult_4_stage	Four-Stage Pipelined Multiplier
DW02_mult_5_stage	Five-Stage Pipelined Multiplier
DW02_mult_6_stage	Six-Stage Pipelined Multiplier
DW02_prod_sum	Generalized Sum of Products
DW02_prod_sum1	Multiplier-Adder
DW02_sum	Vector Adder
DW02_tree	Wallace Tree Compressor
DW_addsub_dx	Duplex Adder/Subtractor with Saturation and Rounding
DW_bin2gray	Binary to Gray Converter
DW_cmp_dx	Duplex Comparator
DW_cntr_gray	Gray Code Counter
DW_div	Combinational Divider
DW_div_pipe	Stallable Pipelined Divider
DW_div_sat	Combinational Divider with Saturation
DW_exp2	Base-2 Exponential
DW_gray2bin	Gray to Binary Converter
DW_inc_gray	Gray Incrementer
DW_inv_sqrt	Reciprocal of Square-Root
DW_lbsh	Barrel Shifter with Preferred Left Direction
DW_ln	Natural Logarithm
DW_log2	Base-2 Logarithm
DW_lp_multifunc	minPower Low Power Multi-function Unit
DW_lp_multifunc_DG	minPower Low Power Multi-function Unit with Datapath Gating
DW_lp_piped_div	minPower Low Power Pipelined Divide
DW_lp_piped_mult	minPower Low Power Pipelined Multiplier
DW_lp_piped_prod_sum	minPower Low Power Pipelined Sum of Products
DW_lp_piped_sqrt	minPower Low Power Pipelined Square Root
DW_minmax	Minimum/Maximum Value
DW_mult_dx	Duplex Multiplier
DW_mult_pipe	Stallable Pipelined Multiplier
DW_norm	Normalization for Fractional Input
DW_norm_rnd	Normalization and Rounding
DW_piped_mac	Pipelined Multiplier-Accumulator
DW_prod_sum_pipe	Stallable Pipelined Generalized Sum of Products
DW_rash	Arithmetic Shifter with Preferred Right Direction
DW_rbsh	Barrel Shifter with Preferred Right Direction
DW_shifter	Combined Arithmetic and Barrel Shifter
DW_sla	Arithmetic Left Shifter
DW_sqrt	Combinational Square Root
DW_sqrt_pipe	Stallable Pipelined Square Root

DW_square	Integer Squarer
DW_squarep	Partial Product Integer Squarer
DW_sra	Arithmetic Right Shifter
Datapath: Floating Point (Overview)	
DW_fp_add	Floating-Point Adder
DW_fp_addsub	Floating-Point Adder/Subtractor
DW_fp_addsub_DG	Floating-Point Adder/subtractor with Datapath Gating
DW_fp_add_DG	Floating-Point Adder with Datapath Gating
DW_fp_cmp	Floating-Point Comparator
DW_fp_cmp_DG	Floating-Point Comparator with Datapath Gating
DW_fp_div	Floating-Point Divider
DW_fp_div_DG	Floating-Point Divider with Datapath Gating
DW_fp_div_seq	Floating-Point Sequential Divider
DW_fp_dp2	2-Term Floating-Point Dot-product
DW_fp_dp3	3-Term Floating-Point Dot-product
DW_fp_dp4	4-Term Floating-Point Dot-product
DW_fp_exp	Floating-Point Exponential (e^a)
DW_fp_exp2	Floating-Point Base-2 Exponential
DW_fp_flt2i	Floating-Point to Integer Converter
DW_fp_i2flt	Integer to Floating-Point Converter
DW_fp_invsqrt	Floating-Point Reciprocal of Square Root
DW_fp_ln	Floating-Point Natural Logarithm
DW_fp_log2	Floating-Point Base-2 Logarithm
DW_fp_mac	Floating-Point Multiply and Add
DW_fp_mac_DG	Floating-Point Multiply-and-Add with Datapath Gating
DW_fp_mult	Floating-Point Multiplier
DW_fp_mult_DG	Floating-Point Multiply with Datapath Gating
DW_fp_recip	Floating-Point Reciprocal
DW_fp_recip_DG	Floating-Point Reciprocal with Datapath Gating
DW_fp_sincos	Floating-Point Sine or Cosine
DW_fp_sqrt	Floating-Point Square Root
DW_fp_square	Floating-Point Square
DW_fp_sub	Floating-Point Subtractor
DW_fp_sub_DG	Floating-Point Subtractor with Datapath Gating
DW_fp_sum3	3-input Floating-Point Adder
DW_fp_sum3_DG	3-Input Floating-Point Adder with Datapath Gating
DW_fp_sum4	4-input Floating-Point Adder
DW_lp_fp_multifunc	minPower Low Power Floating-Point Multi-function Unit
DW_lp_fp_multifunc_DG	minPower Low Power Floating-Point Multi-function Unit with Datapath Gating
DW_lp_piped_fp_add	minPower Low Power Pipelined Floating-Point Adder
DW_lp_piped_fp_div	minPower Low Power Pipelined Floating-Point Divide
DW_lp_piped_fp_mult	minPower Low Power Pipelined Floating-Point Multiplier
DW_lp_piped_fp_recip	minPower Low Power Pipelined Floating-Point Reciprocal
DW_lp_piped_fp_sum3	minPower Low Power Pipelined 3-input Floating-Point Adder
Datapath: Sequential (Overview)	
DW_div_seq	Sequential Divider
DW_mult_seq	Sequential Multiplier

DW_sqrt_seq	Sequential Square Root
Datapath: Trigonometric (Overview)	
DW_sincos	Sine and Cosine
Data Integrity (Overview)	
DW04_par_gen	Parity Generator and Checker
DW_crc_p	Universal Parallel (Combinational) CRC Generator/Checker
DW_crc_s	Universal Synchronous (Clocked) CRC Generator/Checker
DW_ecc	Error Checking and Correction
DW_lp_piped_ecc	minPower Low Power Pipelined Error Correction (ECC)
Data Integrity: Coding (Overview)	
DW_8b10b_dec	8b10b Decoder
DW_8b10b_enc	8b10b Encoder
DW_8b10b_unbal	8b10b Coding Balance Predictor
Digital Signal Processing (Overview)	
DW_dct_2d	Two Dimensional Discreet Cosine Transform (DCT)
DW_fir	High-Speed Digital FIR Filter
DW_fir_seq	Sequential Digital FIR Filter Processor
DW_iir_dc	High-Speed Digital IIR Filter with Dynamic Coefficients
DW_iir_sc	High-Speed Digital IIR Filter with Static Coefficients
Interface: Clock Domain Crossing (Overview)	
DW_data_qsync_hl	Quasi-Synchronous Data Interface for H-to-L Frequency Clocks
DW_data_qsync_lh	Quasi-Synchronous Data Interface for L-to-H Frequency Clocks
DW_data_sync	Data Bus Synchronizer with Acknowledge

DW_data_sync	Data Bus Synchronizer with Acknowledge
DW_data_sync_1c	Single Clock Filtered Data Bus Synchronizer
DW_data_sync_na	Data Bus Synchronizer without Acknowledge
DW_gray_sync	Gray Coded Synchronizer
DW_pulseack_sync	Pulse Synchronizer with Acknowledge
DW_pulse_sync	Dual Clock Pulse Synchronizer
DW_reset_sync	Reset Sequence Synchronizer
DW_stream_sync	Data Stream Synchronizer
DW_sync	Single Clock Data Bus Synchronizer
Logic: Combinational Components (Overview)	
DW01_binenc	Binary Encoder
DW01_decode	Decoder
DW01_mux_any	Universal Multiplexer
DW01_prienc	Priority Encoder
DW_decode_en	Binary Decoder with Enable
DW_lod	Leading One's Detector
DW_lsd	Leading Signs Detector
DW_lza	Leading Zero's Anticipator
DW_lzd	Leading Zero's Detector
DW_pricod	Priority Coder
DW_thermdec	Binary Thermometer Decoder with Enable
Logic: Sequential Components (Overview)	
DW03_bictr_dcnto	Up/Down Binary Counter with Dynamic Count-to Flag
DW03_bictr_decode	Up/Down Binary Counter with Output Decode

DW03_bictr_scnto	Up/Down Binary Counter with Static Count-to Flag
DW03_lfsr_dcnto	LFSR Counter with Dynamic Count-to Flag
DW03_lfsr_load	LFSR Counter with Loadable Input
DW03_lfsr_scnto	LFSR Counter with Static Count-to Flag
DW03_lfsr_updn	LFSR Up/Down Counter
DW03_updn_ctr	Up/Down Counter
DW_dpll_sd	Digital Phase Locked Loop
DW_lp_cntr_updn_df	minPower Low Power Counter with Dynamic Terminal Count Flag
DW_lp_cntr_up_df	minPower Low Power Up Counter with Dynamic Terminal Count Flag
Memory: FIFO (Overview)	
DW_asymdata_inbuf	Asymmetric Data Input Buffer
DW_asymdata_outbuf	Asymmetric Data Output Buffer
DW_asymfifo_s1_df	Asymmetric I/O Synchronous (Single Clock) FIFO with Dynamic Flags
DW_asymfifo_s1_sf	Asymmetric I/O Synchronous (Single Clock) FIFO with Static Flags
DW_asymfifo_s2_sf	Asymmetric Synchronous (Dual-Clock) FIFO with Static Flags
DW_fifo_2c_df	Dual clock FIFO with Dynamic Flags
DW_fifo_s1_df	Synchronous (Single Clock) FIFO with Dynamic Flags
DW_fifo_s1_sf	Synchronous (Single Clock) FIFO with Static Flags
DW_fifo_s2_sf	Synchronous (Dual-Clock) FIFO with Static Flags
DW_lp_fifo_1c_df	Low Power Single Independent Clock FIFO
Memory: FIFO Controllers (Overview)	
DW_asymfifoctl_2c_df	Asymmetric Synchronous (Dual Clock) FIFO Controller with Dynamic Flags
DW_asymfifoctl_s1_df	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Dynamic Flags
DW_asymfifoctl_s1_sf	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Static Flags
DW_asymfifoctl_s2_sf	Asymmetric Synchronous (Dual-Clock) FIFO Controller with Static Flags
DW_fifoctl_2c_df	Dual clock FIFO Controller with Synchronous Memory Support and Dynamic Flags
DW_fifoctl_s1_df	Synchronous (Single Clock) FIFO Controller with Dynamic Flags
DW_fifoctl_s1_sf	Synchronous (Single-Clock) FIFO Controller with Static Flags
DW_fifoctl_s2_sf	Synchronous (Dual-Clock) FIFO Controller with Static Flags
DW_lp_fifoctl_1c_df	minPower Low Power Single clock FIFO Controller with Dynamic Flags
Memory: Registers (Overview)	
DW03_pipe_reg	Pipeline Register
DW03_reg_s_pl	Register with Synchronous Enable Reset
DW03_shftreg	Shift Register
DW04_shad_reg	Shadow and Multibit Register
DW_pl_reg	Pipeline Register with individual enables
Memory: SRAMs (Overview)	
DW_ram_2r_2w_s_dff	Synchronous write, asynchronous read, 4-port RAM (FF-based)
DW_ram_2r_w_a_dff	Asynchronous Three-Port RAM (Flip-Flop Based)
DW_ram_2r_w_a_lat	Write-Port, Dual-Read-Port RAM (Latch-Based)
DW_ram_2r_w_s_dff	Synchronous Write-Port, Asynchronous Dual Read-Port RAM (Flip-Flop Based)
DW_ram_2r_w_s_lat	Synchronous Write-Port, Asynchronous Dual Read-Port RAM (Latch-Based)
DW_ram_rw_a_dff	Asynchronous Single-Port RAM (Flip-Flop Based)
DW_ram_rw_a_lat	Asynchronous Single-Port RAM (Latch-Based)
DW_ram_rw_s_dff	Synchronous Single-Port, Read/Write RAM (Flip-Flop Based)
DW_ram_rw_s_lat	Synchronous Single-Port, Read/Write RAM (Latch-Based)
DW_ram_r_w_2c_dff	Synchronous Two-Clock RAM (Flip-Flop-Based))

DW_ram_r_w_a_dff	Asynchronous Dual-Port RAM (Flip-Flop Based)
DW_ram_r_w_a_lat	Asynchronous Dual-Port RAM (Latch-Based)
DW_ram_r_w_s_dff	Synchronous Write-Port, Asynchronous Read-Port RAM (Flip-Flop Based)
DW_ram_r_w_s_lat	Synchronous Write-Port, Asynchronous Read-Port RAM (Latch-Based)
Memory: Stacks (Overview)	
DW_stack	Synchronous (Single Clock) Stack
DW_stackctl	Synchronous (Single Clock) Stack Controller
Test: JTAG (Overview)	
DW_bc_1	Boundary Scan Cell Type BC_1
DW_bc_10	Boundary Scan Cell Type BC_10
DW_bc_2	Boundary Scan Cell Type BC_2
DW_bc_3	Boundary Scan Cell Type BC_3
DW_bc_4	Boundary Scan Cell Type BC_4
DW_bc_5	Boundary Scan Cell Type BC_5
DW_bc_7	Boundary Scan Cell Type BC_7
DW_bc_8	Boundary Scan Cell Type BC_8
DW_bc_9	Boundary Scan Cell Type BC_9
DW_tap	TAP Controller
DW_tap_uc	TAP Controller with USERCODE Support
Datapath Functions (Overview)	
DWF_dp_absval	Returns the absolute value (magnitude) of an argument
DWF_dp_blend	Implements an alpha blender or linear interpolator
DWF_dp_count_ones	Counts ones in argument
DWF_dp_mult_comb	Performs a combined unsigned/signed multiply
DWF_dp_mult_comb_ovfldet	Performs a combined unsigned/signed multiply and overflow detection
DWF_dp_mult_comb_sat	Performs a combined unsigned/signed multiply and saturation
DWF_dp_mult_ovfldet	Performs a multiplication with overflow detection
DWF_dp_mult_sat	Performs a multiplication and saturation
DWF_dp_rnd	Performs arithmetic rounding
DWF_dp_rndsat	Performs arithmetic rounding and saturation
DWF_dp_sat	Performs arithmetic saturation
DWF_dp_sign_select	Performs sign selection / conditional two's complement
DWF_dp_simd_add	Configurable SIMD adder
DWF_dp_simd_addc	Configurable SIMD adder with carry
DWF_dp_simd_mult	Configurable SIMD multiplier
DWF_dp_sub_abs	Returns the absolute value of a subtraction
DW_lp_pipe_mgr	minPower Low Power Pipeline Manager