CS6135 VLSI Physical Design Automation

Homework 1: P&R Tool

賈俊佑 studentID:114062645

1.Introdution

This project uses Cadence Innovus to perform the Place and Route (P&R) flow for a given synthesized standard-cell design. The goal is to optimize timing, chip area, and wire length.

2.Objective

- Optimize the timing by adjust the clock period in the sdc/misty.sdc file
  - Default clock period:1850
- Optimize the area by adjust the core utilization in the floorplan stage
  - Default core utilization:0.5
- Achieve non-negative slack and zero DRC violation
- Get the lower value for following attributes
  - Clock period
  - Total area of chip
  - Total wire length

3.Experiment result

3.1Set up

In this experiment, I explored the effect of two key parameters during the place-and-route (P&R) flow: clock period and core utilization. Three different clock periods were tested, namely 1850,1825, and 1800(ps), while the core utilization was gradually increased from 0.4 up to 0.75.

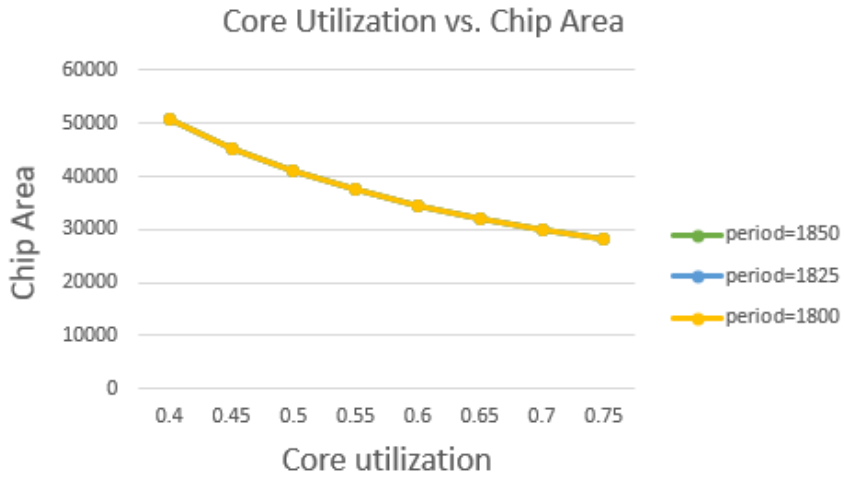
3.2Configuration

Core Utilization	Clock Period	DRC violations	Slack	Chip Area	Wire length
0.4	1850	2	0	50689.193	211254.496
0.45	1850	0	0.5	45389.196	210312.516
0.5	1850	0	0.5	41107.357	208818.26

0.55	1850	0	0.2	37595.032	206415.312
0.6	1850	1	0	34640.234	202944.116
0.65	1850	1	-0.1	32167.01	205670.284
0.7	1850	7	0.4	30033.649	197128.008
0.75	1850	3	-6.5	28191.235	193714.748
0.4	1825	0	0.2	50689.193	218412.056
0.45	1825	5	0	45389.196	218027.408
0.5	1825	1	0.3	41107.357	215782.052
0.55	1825	0	0	37595.032	216977.768
0.6	1825	5	0.1	34640.234	208570.9
0.65	1825	5	-22.1	32167.01	216118.752
0.7	1825	4	-20.1	30033.649	208308.008
0.75	1825	6	-15.7	28191.235	206398.828
0.4	1800	4	-29.2	50689.193	224405.672
0.45	1800	0	-25.3	45389.196	226181.44
0.5	1800	1	-32	41107.357	223573.72
0.55	1800	2	-25	37595.032	225362.7
0.6	1800	4	-24.8	34640.234	217850.592
0.65	1800	2	-32	32167.01	217371.08
0.7	1800	8	-26	30033.649	207686.312
0.75	1800	16	-30.4	28191.235	203157.812

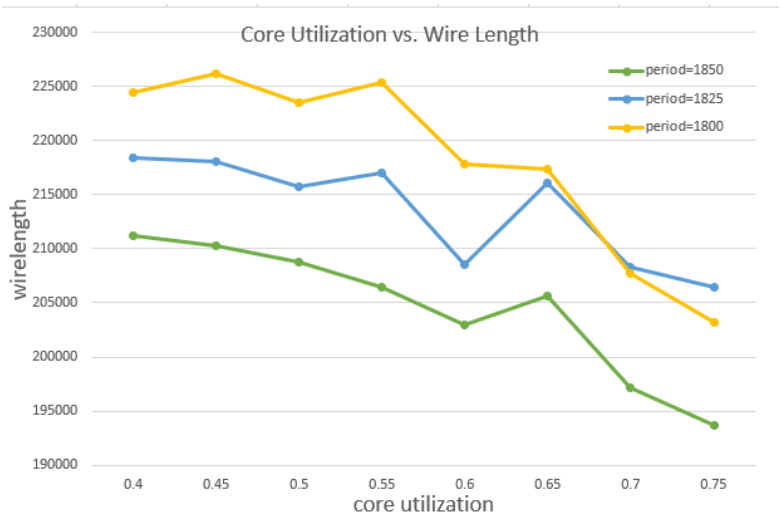
3.3 Observations and Analysis

a. Core Utilization vs. Chip Area



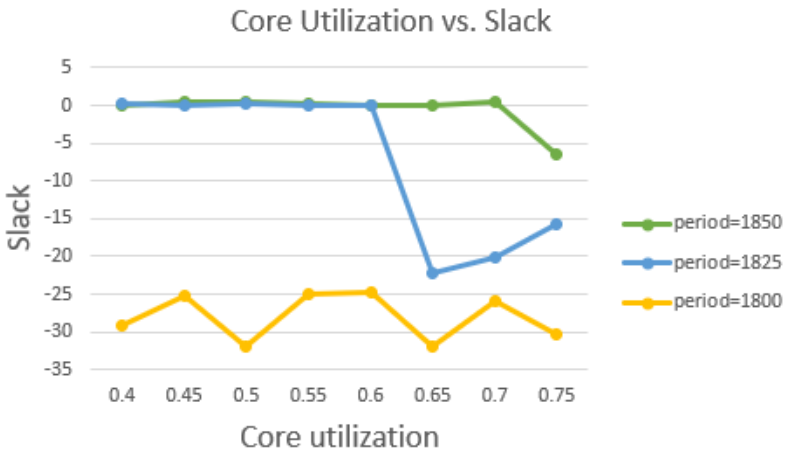
The figure above shows the relationship between core utilization and chip area. It can be observed that as the core utilization increases, the chip area decreases accordingly.

b. Core Utilization vs. Wire Length



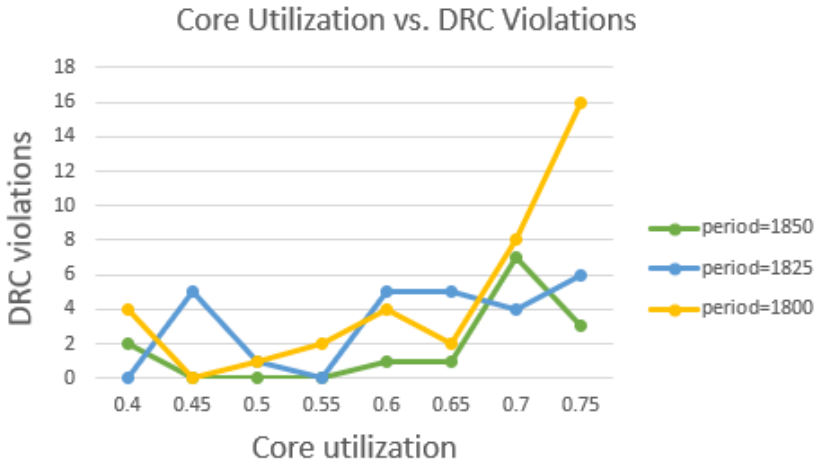
The figure above shows the relationship between core utilization and wire length. It can be observed that, in general, as the core utilization increases, the wire length tends to decrease. However, for clock periods of 1850 and 1825, the wire length increases when the core utilization is 0.65.

c. Core Utilization vs. Slack



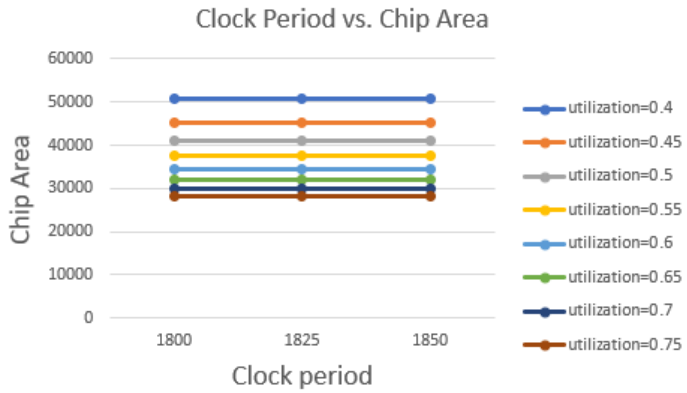
The figure above shows the relationship between core utilization and slack. It can be observed that the slack remains within a similar range regardless of the core utilization, except for the case of 1825 clock period. When the clock period is 1825 and the core utilization exceeds 0.6, the slack decreases to a negative value.

d. Core Utilization vs. DRC Violations



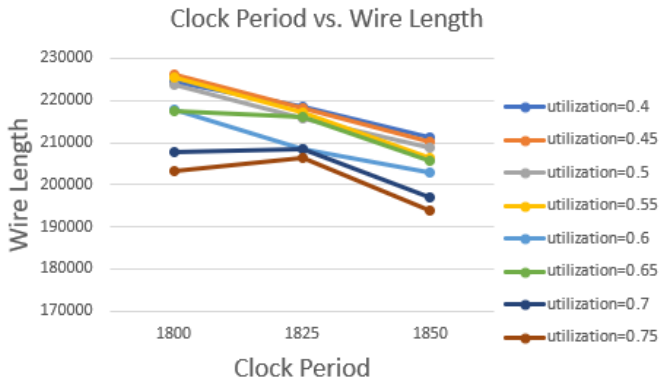
The figure above shows the relationship between core utilization and DRC violations. It can be observed that when the core utilization exceeds a certain value, the likelihood of DRC violations increases.

e. Clock Period vs. Chip Area



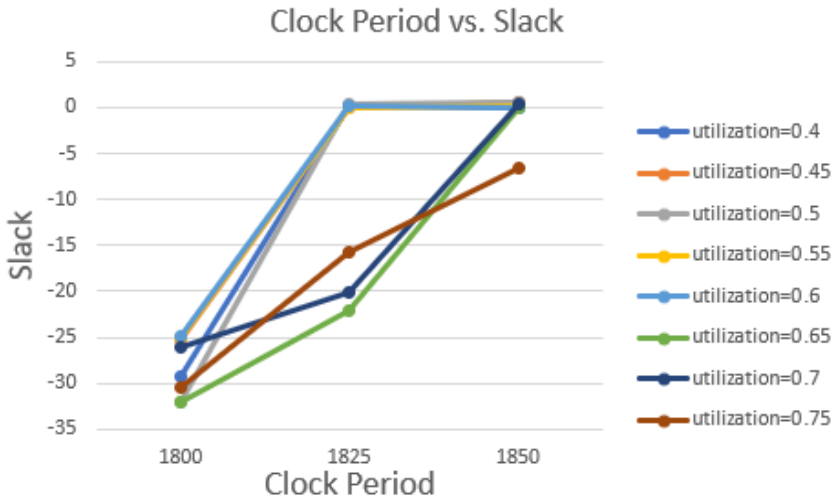
The figure above shows the relationship between clock period and core utilization. It can be observed that, for the same core utilization, the chip area remains constant regardless of the clock period. Therefore, we can conclude that the clock period does not influence the chip area.

f. Clock Period vs. Wire Length



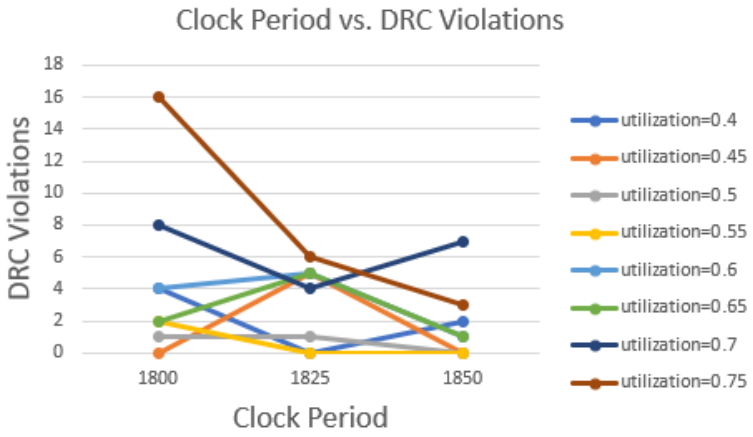
The figure shows the relationship between clock period and wire length. It can be observed that, for all utilizations, the wire length decreases slightly as the clock period increases. This indicates that a longer clock period generally leads to reduced wire length, although the degree of reduction varies depending on utilization.

g. Clock Period vs. Slack



The figure shows the relationship between clock period and slack. As the clock period increases, the slack improves significantly, moving from negative values toward zero. This indicates that a longer clock period relaxes timing constraints, thereby enhancing slack performance across all utilization levels. Additionally, it can be observed that when the clock period is set to 1800, all slack values remain negative, suggesting that the clock period cannot be reduced excessively.

h. Clock Period vs. DRC Violations



The figure shows the relationship between clock period and the number of DRC violations. It can be observed that the number of violations varies with different utilizations and does not follow a strictly decreasing trend as the clock period increases. For instance, at utilization 0.75, the number of violations drops significantly from 16 at a clock period of 1800 to 6 at longer periods, while other utilization levels fluctuate slightly across different periods.

4.The purpose of inserting well tap cell

Well tap cells are incorporated into the layout to provide a direct connection between the wells/substrate and the power or ground rails. This design practice prevents latch-up by suppressing parasitic PNPN conduction, enhances circuit reliability by stabilizing the substrate potential, and ensures consistent biasing of transistors across the chip.

5.Best result

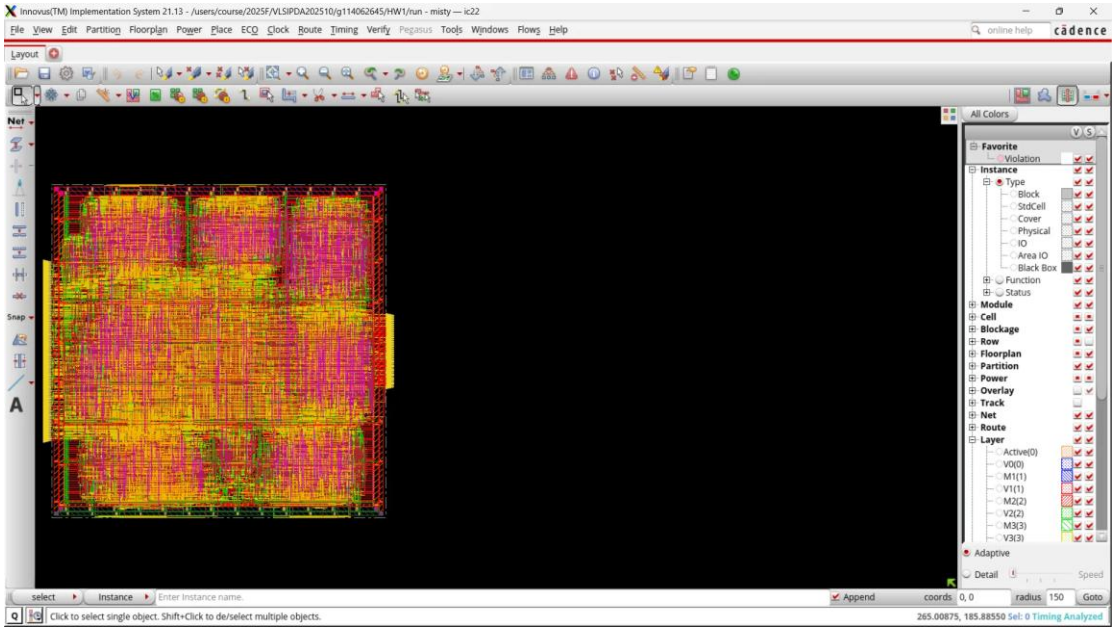
5.1configuration

Core Utilization	Clock Period	DRC violations	Slack	Chip Area	Wire length
0.66	1843	0	0	31729.564	201026.92

5.2result picture

```
--- Summary of the Current Result ---
Slack Time:          0.000
DRC Violations:      0
Clock Period:        1843.000
Total area of chip: 31729.564
Total wire length:  201026.9200
-------------------------------------
```

5.3layout



6.other result

This is the configuration to find the best result

Core Utilization	Clock Period	DRC violations	Slack	Chip Area	Wire length
0.6	1830	1	0.1	34640.234	210666.408
0.65	1835	4	-20.5	32167.01	216636.916
0.65	1840	1	-1.4	32167.01	211835.016
0.65	1845	2	0.1	32167.01	207966.256
0.6	1835	0	0.1	34640.234	208786.176
0.7	1840	5	-17.3	30033.649	206316.948
0.7	1845	1	0	30033.649	198262.352
0.75	1845	8	0.3	28191.235	194436.236
0.75	1860	10	-11.9	28191.235	190167.404
0.7	1835	10	-9.9	30033.649	205350.92
0.68	1845	10	-11.2	30837.294	200890.556

0.68	1840	4	0	30837.294	200778.976
0.71	1845	6	0.1	29635.891	201634.284
0.67	1845	4	0	31293.859	199955.66
0.69	1845	8	0.1	30434.269	195998.012
0.66	1845	1	0.4	31829.564	200174.928
0.64	1849	0	0.3	32633.446	205173.66
0.65	1849	1	0.2	32167.01	205337.296
0.66	1849	1	0	31729.564	198615.084
0.67	1849	1	0.1	31293.859	198898.128
0.68	1849	4	0.1	30837.294	197608.076
0.69	1849	6	0.3	30434.269	196122.616
0.64	1847	1	0	32633.446	206430.26
0.65	1847	1	0.2	32167.01	205108.528
0.66	1847	5	0.1	31729.564	196124.456
0.64	1846	1	0.3	32633.446	208039.736
0.65	1846	1	0	32167.01	207923.512
0.66	1846	3	0	31729.564	202477.208
0.67	1846	2	0.2	31293.859	201208.288
0.64	1845	4	0.2	32633.446	205231.52
0.66	1850	1	0	31729.564	200562.732
0.67	1850	3	0.1	31293.859	199254.54
0.68	1850	4	0	30837.294	197302.436
0.64	1844	1	0.3	32633.446	205601.5408
0.65	1844	3	-11.9	32167.01	208349.824
0.64	1843	1	0	32633.446	207185.712
0.65	1843	2	0.8	32167.01	210684.156