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**Lab. 1**

**Pseudo Noise Sequence and Gold Code**

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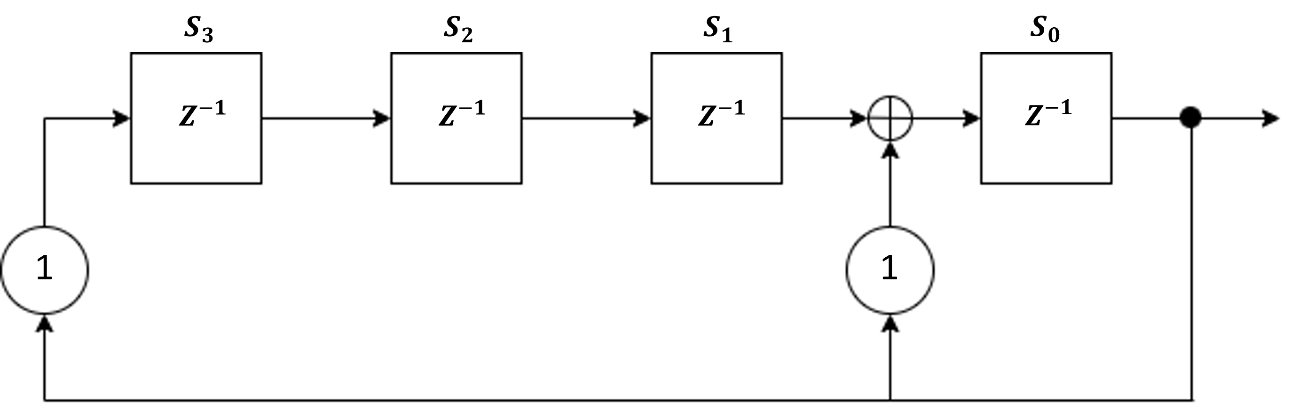
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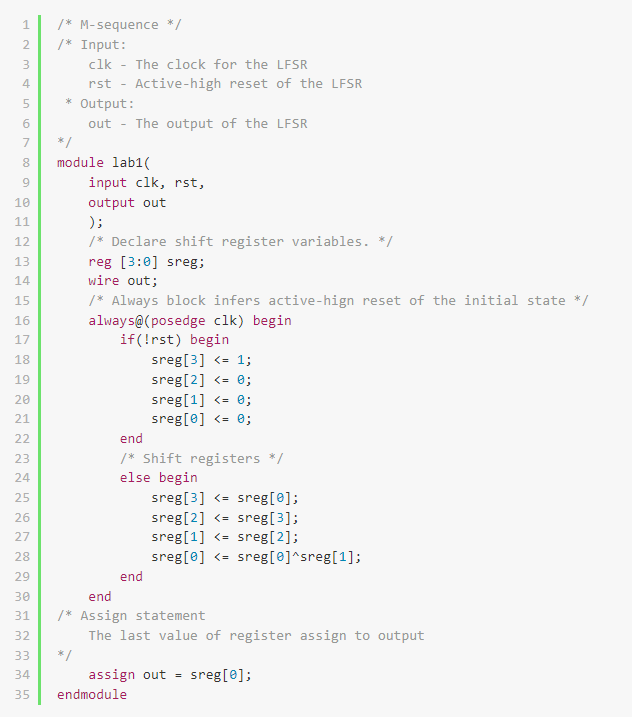
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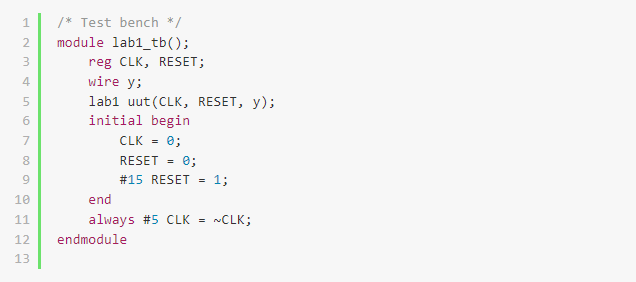
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## Block diagram of the LFSR with coefficients 23oct.



## Verilog code





## The timing diagram of RTL simulation

Initial state: 1 0 0 0

M-sequence (generated by Matlab):

0 0 0 1 1 1 1 0 1 0 1 1 0 0 1



M-sequence (implement by Verilog code):



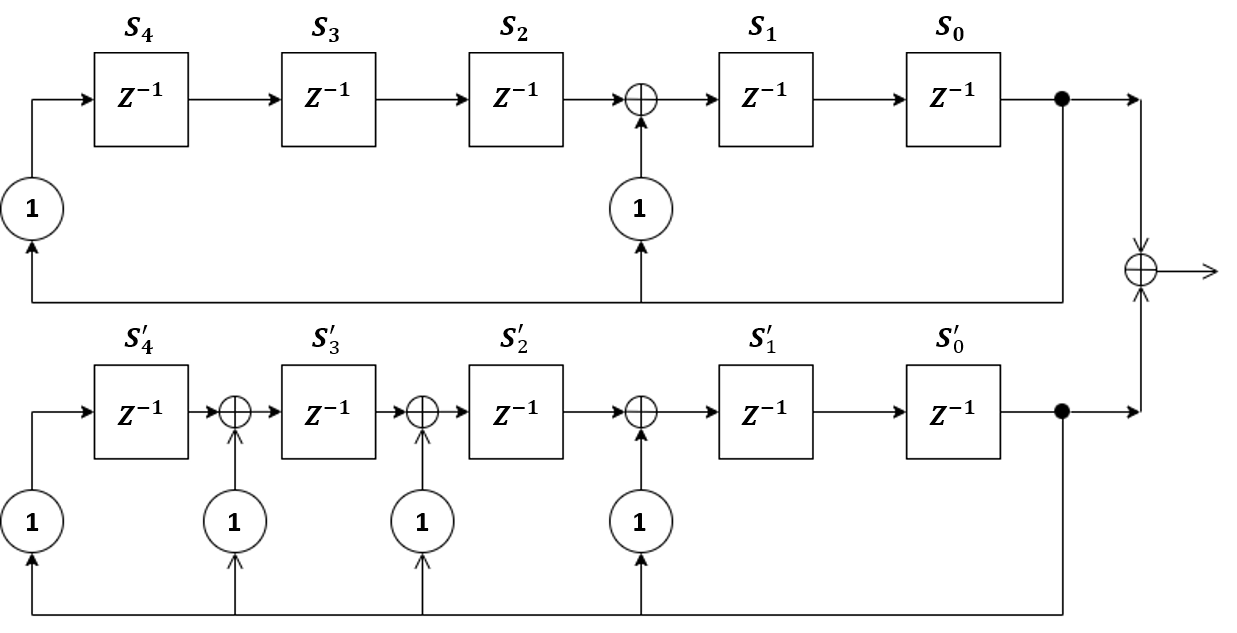
0 0 0 1 1 1 1 0 1 0 1 1 0 0 1



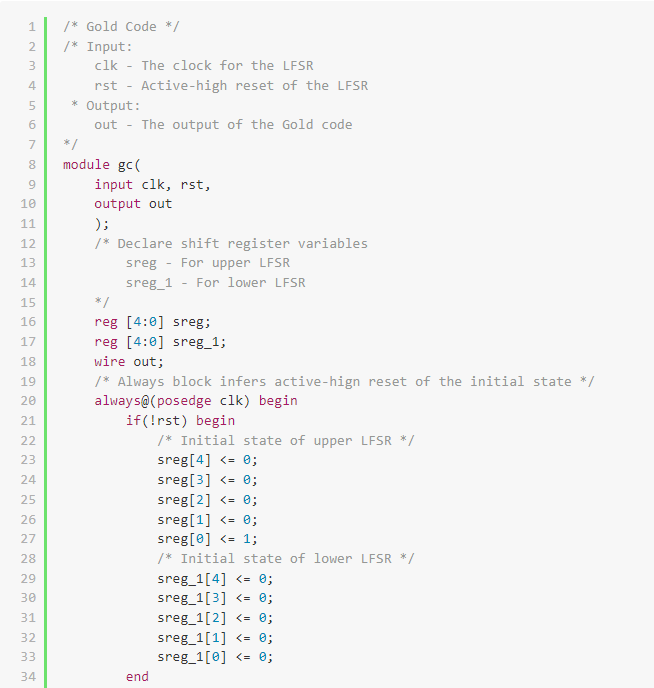
The sequence of 4-stage LFSR has a period of .

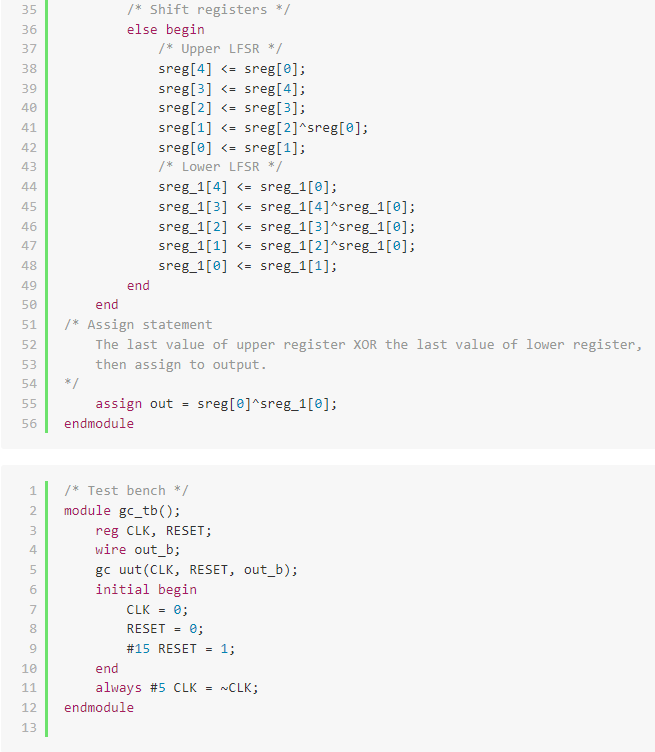
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## Block diagram of Gold code generator.



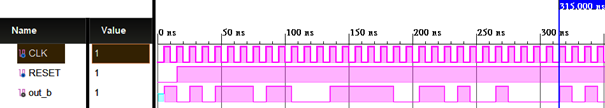
## Verilog Code





## The timing diagram of three code sequences.

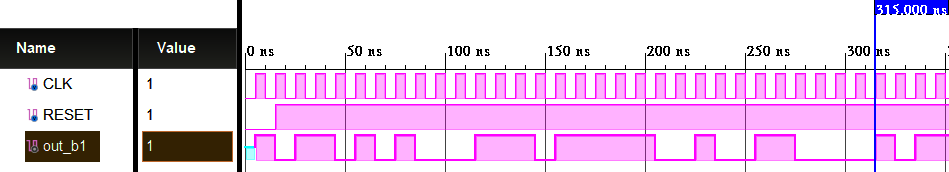
Initial state: Upper LFSR – 0 0 0 0 1 ; Lower LFSR – 0 0 0 0 0



**1 0 1 0 1 1 1 0 1 1 0 0 0 1 1 1 1 1 0 0 1 1 0 1 0 0 1 0 0 0 0**

– sequence:

Initial state: Upper LFSR – 0 0 0 0 0 ; Lower LFSR – 0 0 0 0 1

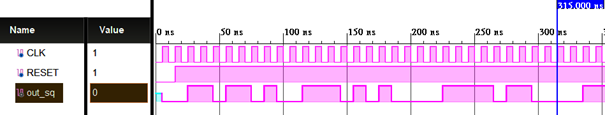


**1 0 1 1 0 1 0 1 0 0 0 1 1 1 0 1 1 1 1 1 0 0 1 0 0 1 1 0 0 0 0**

– sequence:

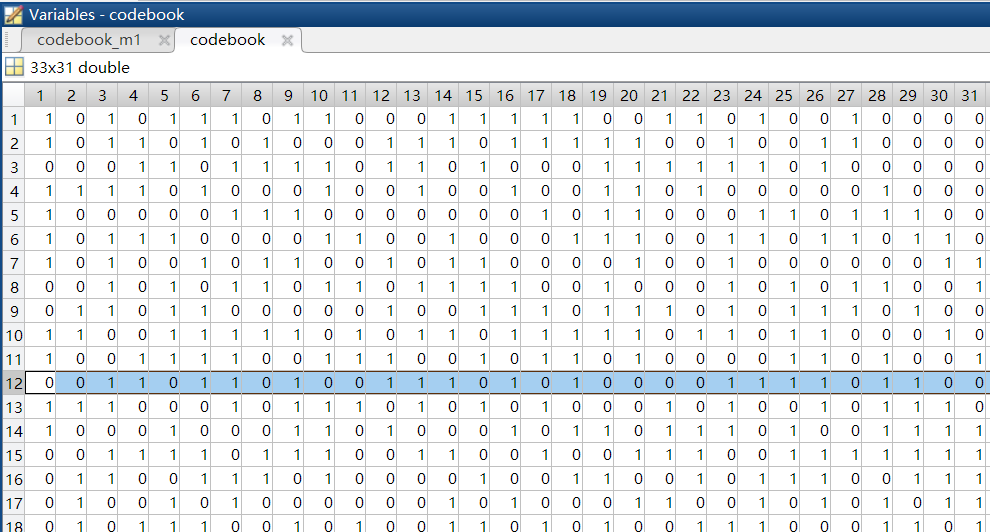
Initial state: Upper LFSR – 0 0 0 0 1 ; Lower LFSR – 0 0 1 0 1

**0 0 1 1 0 1 1 0 1 0 0 1 1 1 0 1 0 1 0 0 0 0 1 1 1 1 0 1 1 0 0**



Third sequence:

## Mathematic result by Matlab.



Third sequence

-sequence

-sequence

# 

Gold code 產生器，是基於M序列設計，由於五次本質多項式係數和是完美對，分別可以產生 序列和 序列，再以固定產生 序列的初始值，和產生 序列的初始值做互斥或，對 序列的初始值做相移有 種，所以得到共33組不同的Gold code序列。

以上驗證結果後，可以得到硬體的產生方式和數學理論產生出的33組Gold code序列是一樣的。