**Lab. 6 Fast Fourier Transform (FFT)\_1**

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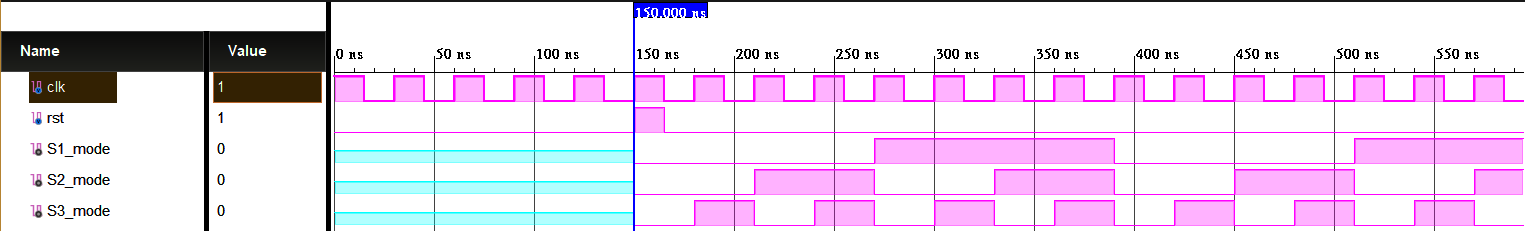
## The real-part and imaginary-part of 𝑌0~𝑌7



## The real-part and imaginary-part of 𝑥0~𝑥7



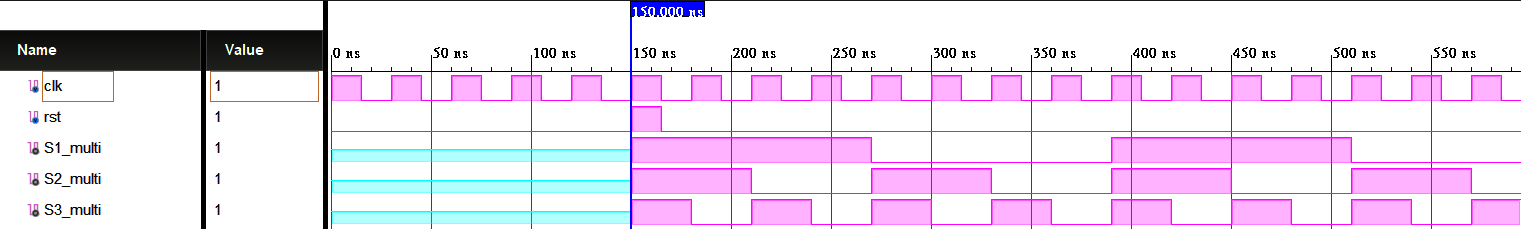
# The control signals to the butterfly module

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S1\_mode: 控制stage1的訊號，1的時候做butterfly，0的時候做bypass。

S2\_mode: 控制stage2的訊號，1的時候做butterfly，0的時候做bypass。

S3\_mode: 控制stage3的訊號，1的時候做butterfly，0的時候做bypass。

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S1\_multi: 控制stage1的訊號，1的時候做乘法，0的時候做bypass。

S2\_multi: 控制stage2的訊號，1的時候做乘法，0的時候做bypass。

S3\_multi: 控制stage3的訊號，1的時候做乘法，0的時候做bypass。

# Implement 8-point SDF FFT architecture with Matlab

## The real-part and imaginary-part of 𝑋0~𝑋7



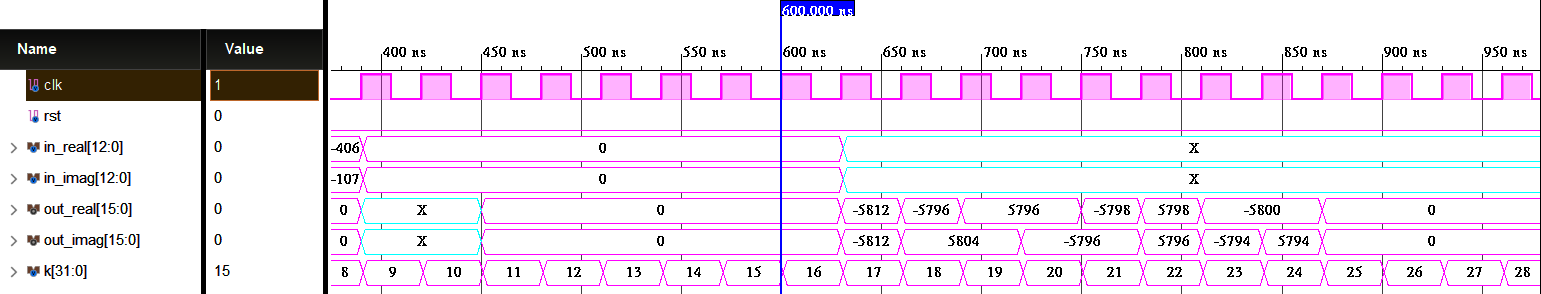
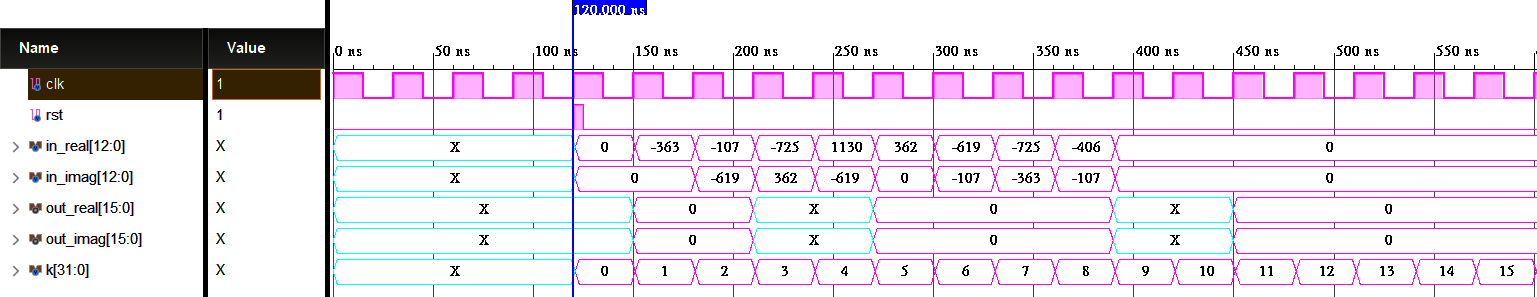
## Bit-reversed order



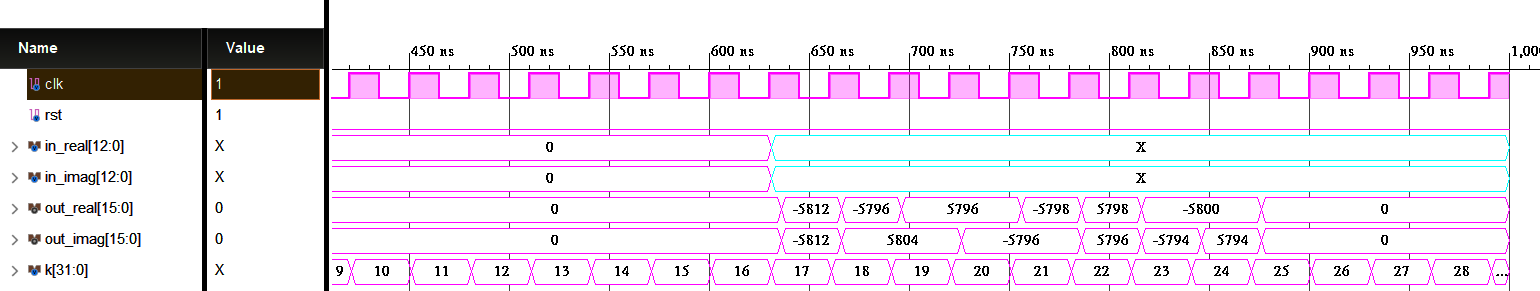
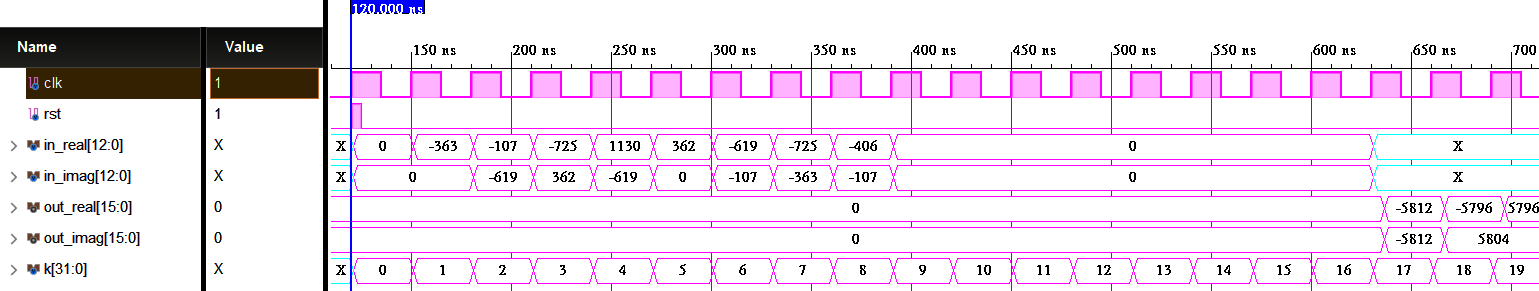
## The difference between 𝑋0~𝑋7 and 𝑌0~𝑌7



## Behavior simulation result



## Post-route simulation results



## Compare with the Verilog and the Matlab results



## The error between the Verilog and the Matlab of real-part



## The error between the Verilog and the Matlab of imaginary-part

