



EE457: Digital IC Design

Fall Semester 2019

Project 3 Report Cover Sheet

Due 11/13/2019

PROJECT TITLE: 16-to-1 Multiplexer (MUX) Using Both Conventional CMOS and Transmission Gates

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Put Check for completion	Topics	GRADES
✓	Section 1: Executive Summary	/5
✓	Section 2: Introduction and Background	/5
✓	Section 3: Electric Circuit Schematics	/10
✓	Section 4: Detailed Electric Layouts	/25
✓	Section 5: IRSIM Logic Simulations and Measurements for Layout and Schematic (<u>must provide comparisons between the two</u>)	/10
✓	Section 6: LTSPICE code and <u>parasitic extractions</u> with calculation analysis for charge sharing. Put only samples of code.	/15
✓	Section 7: Measurements in LTSPICE for delays for Layout and Schematic (<u>must provide comparisons between the two</u>)	/15
✓	Section 8: Measurements of power, delay, chip area, timing, number of transistors for the layout.	Power /2 Delay /2 Area /2 #tran /4
✓	Section 9: Conclusion and References	/5
	Penalty	
	TOTAL	/100

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Section 1: Executive Summary:

In this project, we will be designing a CMOS of a 16-to-1 Multiplexer (MUX) using Electric. By using the Electric software, we'll be creating four different designs, a conventional schematic design, a conventional layout design, a transmission gate (TG) schematic design, and a transmission gate (TG) layout design. The purpose for the use of the transmission gate design is for efficiency and to save on transistors. In order to test if our designs are correct, we'll be generating waveforms to test for correctness by giving a specific input and expecting a certain output. We'll be generating the waveforms using two different software, IRSIM and LTSPICE. The two different software would help support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the two different design, we'll compare them and observe their similarities and differences.

To design a conventional 16-to-1 Multiplexer (MUX), we plan to use three different designs and combining them together to make a 4-to-1 Multiplexer. One design we plan to use is a three input AND gate, the second design we plan to use is a four input OR gate, and the third design we plan to use is an inverter. By combining four AND gates, one OR gates, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexers and link them together to create a 16-to-1 Multiplexer. We would also test each individual design using waveforms before putting them together to make sure they satisfy our requirements. By testing each individual design would also help with the debugging process when combining the two designs together because we'll know where the problem lies in case the waveform doesn't turn out like the way expected.

To design a Transmission Gate (TG) 16-to-1 Multiplexer (MUX), we plan to use two designs and combining them together to make a 4-to-1 Multiplexer. One design we plan to use is an inverter, and the second design we plan to use is a transmission gate. By combining two inverters, and six transmission gates, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexers and link them together to create a 16-to-1 Multiplexer. We would also test each individual design using waveforms before putting them together to make sure they satisfy our requirements. By testing each individual design would also help with the debugging process when combining the two designs together because we'll know where the problem lies in case the waveform doesn't turn out like the way expected.

Section 2: Introduction and Background:

A 16-to-1 Multiplexer is a form of digital circuit that is used to select a certain data. The 16-to-1 Multiplexer would have a total of 20 inputs and one output. 16 of the inputs are data, and the other 4 are what's used to select those data. The output would be the one of the 16 inputs, depending on what the selector selects. Multiplexers itself are often used in larger circuitry and helps a lot in terms of which data are being selected so it could be used for modification without modifying the other data. The truth table of the 16-to-1 Multiplexer is shown on Table 1.

The approach we plan to take to design the conventional 16-to-1 Multiplexer would be to use three different designs and combining them together. The three designs that we plan to use would be a three input AND gate, a four input OR gate, and an inverter. The reason for this approach is because we can't directly build a conventional 16-to-1 Multiplexer without first building a 4-to-1 Multiplexer or any Multiplexer, and we can't build a Multiplexer without using an AND gate, OR gate, or an inverter. By applying four AND gates, one OR gate, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexer and link them together to create a 16-to-1 Multiplexer. The figures on the next few pages show the schematic and layout of the two input AND gate, which becomes a three input AND gate, two input OR gate, which becomes a four input OR gate, an inverter, and a 4-to-1 Multiplexer. In addition, the truth table of a three input AND gate is shown on Table 2; the truth table of a four input OR gate is shown on Table 3; the truth table of an inverter is shown on Table 4; the truth table of a 4-to-1 Multiplexer is shown on Table 5.

The approach we plan to take to design the transmission gate 16-to-1 Multiplexer would be to use two different designs and combining them together. The two designs that we plan to use would be a transmission gate, and an inverter. The reason for this approach is because we can't directly build a transmission gate 16-to-1 Multiplexer without first building a 4-to-1 Multiplexer or any Multiplexer, and we can't build a Multiplexer without using a transmission gate, or an inverter. By applying six transmission gates, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexer and link them together to create a 16-to-1 Multiplexer. The figures on the next few pages show the schematic and layout of the 4-to-1 Multiplexer, which consists of six transmission gates, and two inverters. The truth table of a 4-to-1 Multiplexer is already shown on Table 5.

Table 1: Truth Table of a 16-to-1 Multiplexer

Input: S3	Input: S2	Input: S1	Input: S0	Output: 16-to-1 Multiplexer
0	0	0	0	D0
0	0	0	1	D1
0	0	1	0	D2
0	0	1	1	D3
0	1	0	0	D4
0	1	0	1	D5
0	1	1	0	D6
0	1	1	1	D7
1	0	0	0	D8
1	0	0	1	D9
1	0	1	0	D10
1	0	1	1	D11
1	1	0	0	D12
1	1	0	1	D13
1	1	1	0	D14
1	1	1	1	D15

Boolean Expression:

$$\begin{aligned}
 V_{out} = & \overline{S_0} \overline{S_1} \overline{S_2} \overline{S_3} D_0 + S_0 \overline{S_1} \overline{S_2} \overline{S_3} D_1 + \overline{S}_0 S_1 \overline{S_2} \overline{S_3} D_2 + S_0 S_1 \overline{S_2} \overline{S_3} D_3 + \\
 & \overline{S}_0 \overline{S_1} S_2 \overline{S_3} D_4 + S_0 \overline{S}_1 S_2 \overline{S_3} D_5 + \overline{S}_0 S_1 S_2 \overline{S_3} D_6 + S_0 S_1 S_2 \overline{S_3} D_7 + \\
 & \overline{S}_0 \overline{S_1} \overline{S_2} S_3 D_8 + S_0 \overline{S_1} \overline{S_2} S_3 D_9 + \overline{S}_0 S_1 \overline{S_2} S_3 D_{10} + S_0 S_1 \overline{S}_2 S_3 D_{11} + \\
 & \overline{S}_0 \overline{S_1} S_2 S_3 D_{12} + S_0 \overline{S}_1 S_2 S_3 D_{13} + \overline{S}_0 S_1 S_2 S_3 D_{14} + S_0 S_1 S_2 S_3 D_{15}
 \end{aligned}$$

Table 2: Truth Table of a Three Input AND Gate

Input: A	Input: B	Input: C	Output: A AND B AND C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Boolean Expression:

$$V_{out} = A * B * C$$

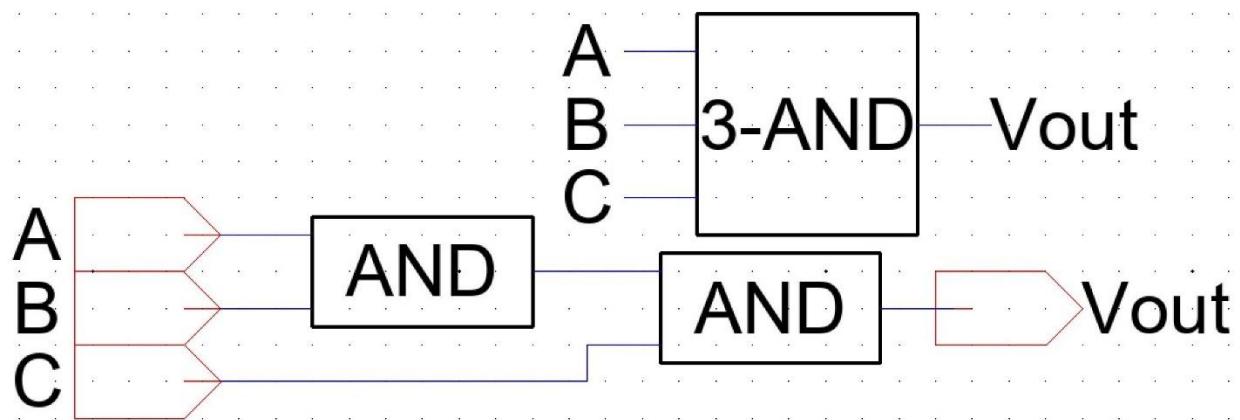


Figure 1: Schematic Design of a Three Input AND Gate

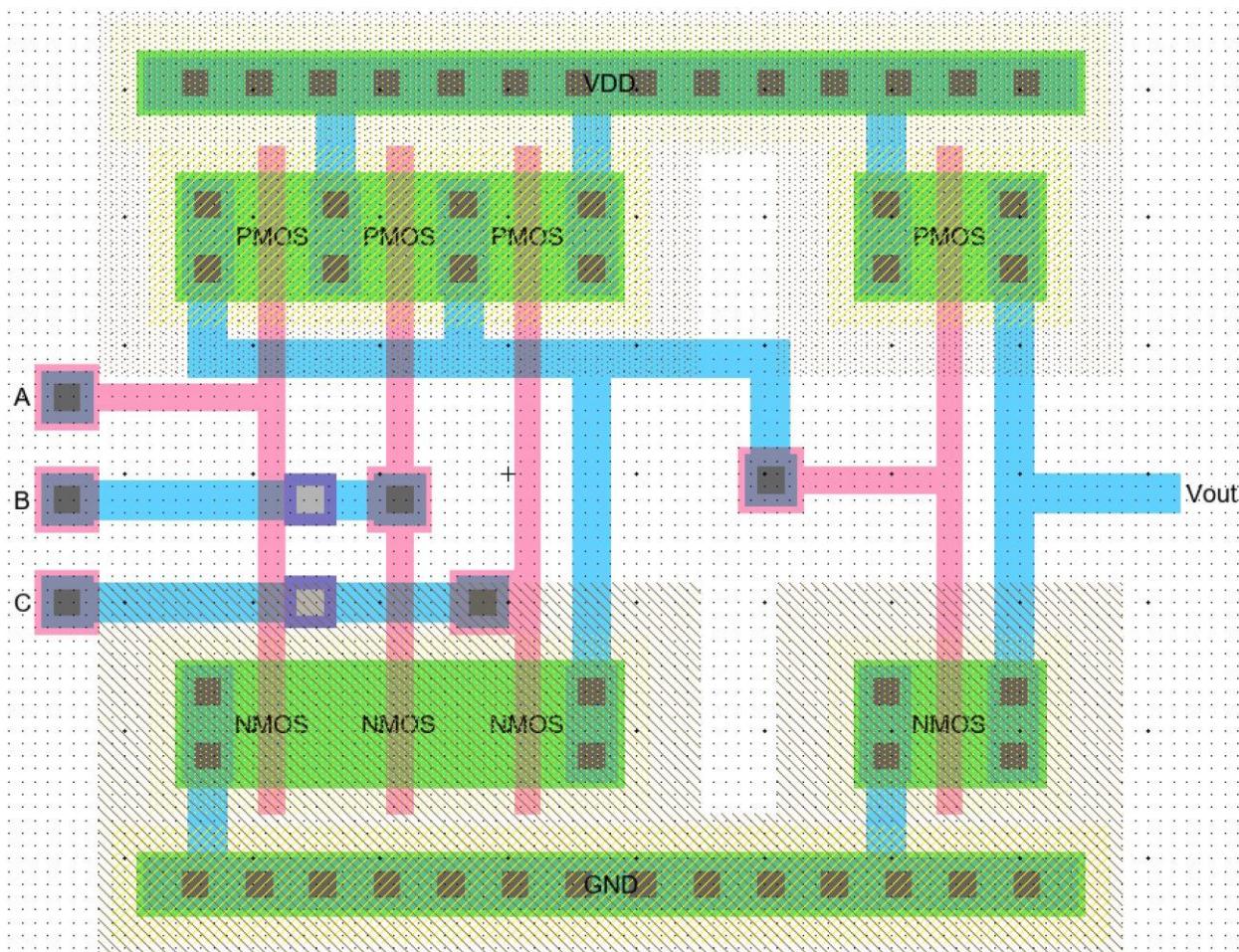


Figure 2: Layout Design of a Three Input AND Gate

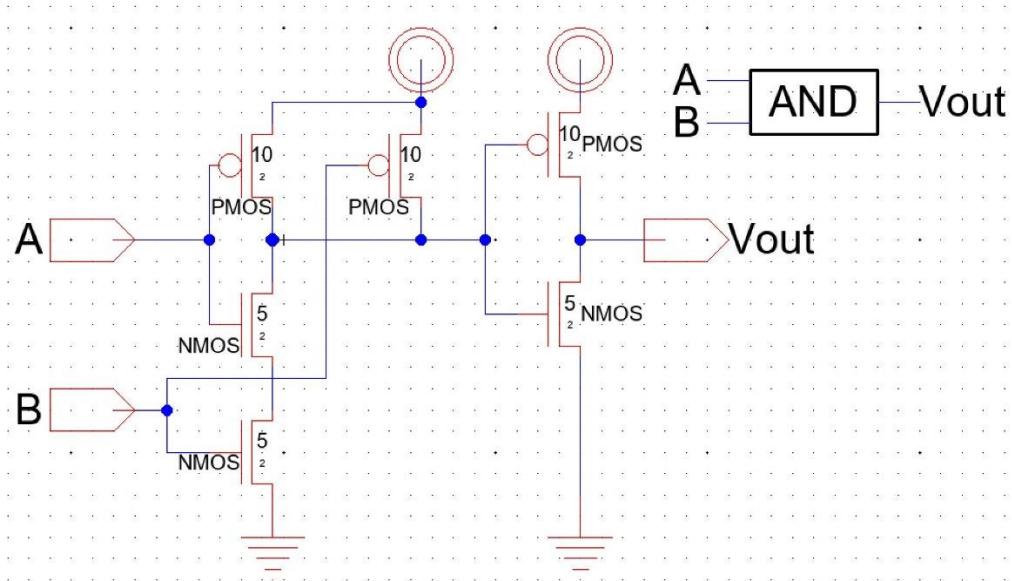


Figure 3: Schematic Design of a Two Input AND Gate That's Used

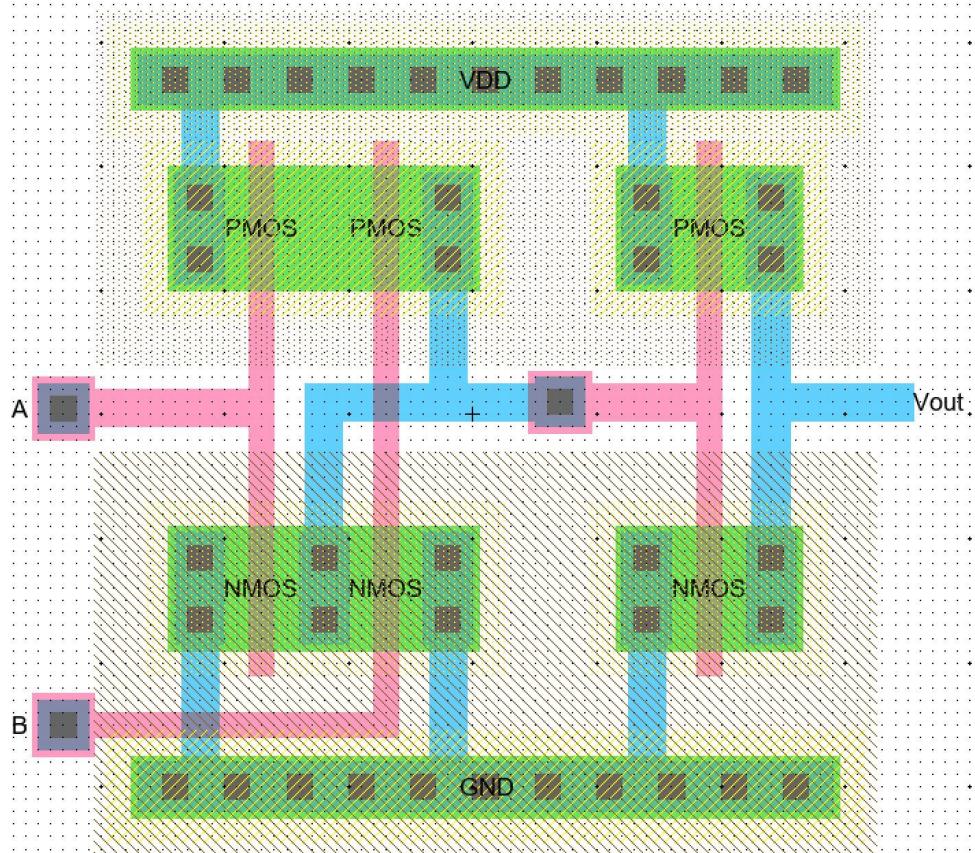


Figure 4: Layout Design of a Two Input AND Gate That's Used

Table 3: Truth Table of a Four Input OR Gate

Input: A	Input: B	Input: C	Input: D	Output: A OR B OR C OR D
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Boolean Expression:

$$V_{out} = A + B + C + D$$

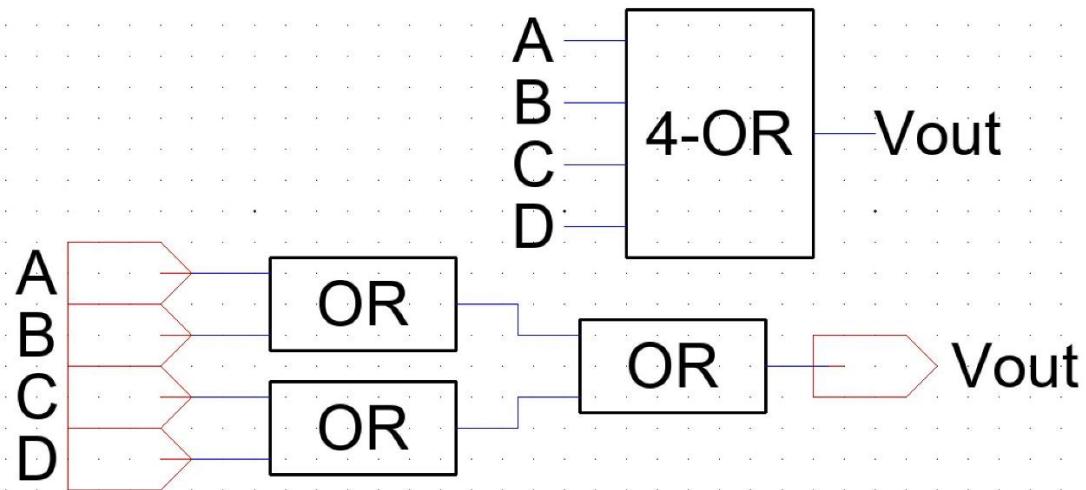


Figure 5: Schematic Design of a Four Input OR Gate

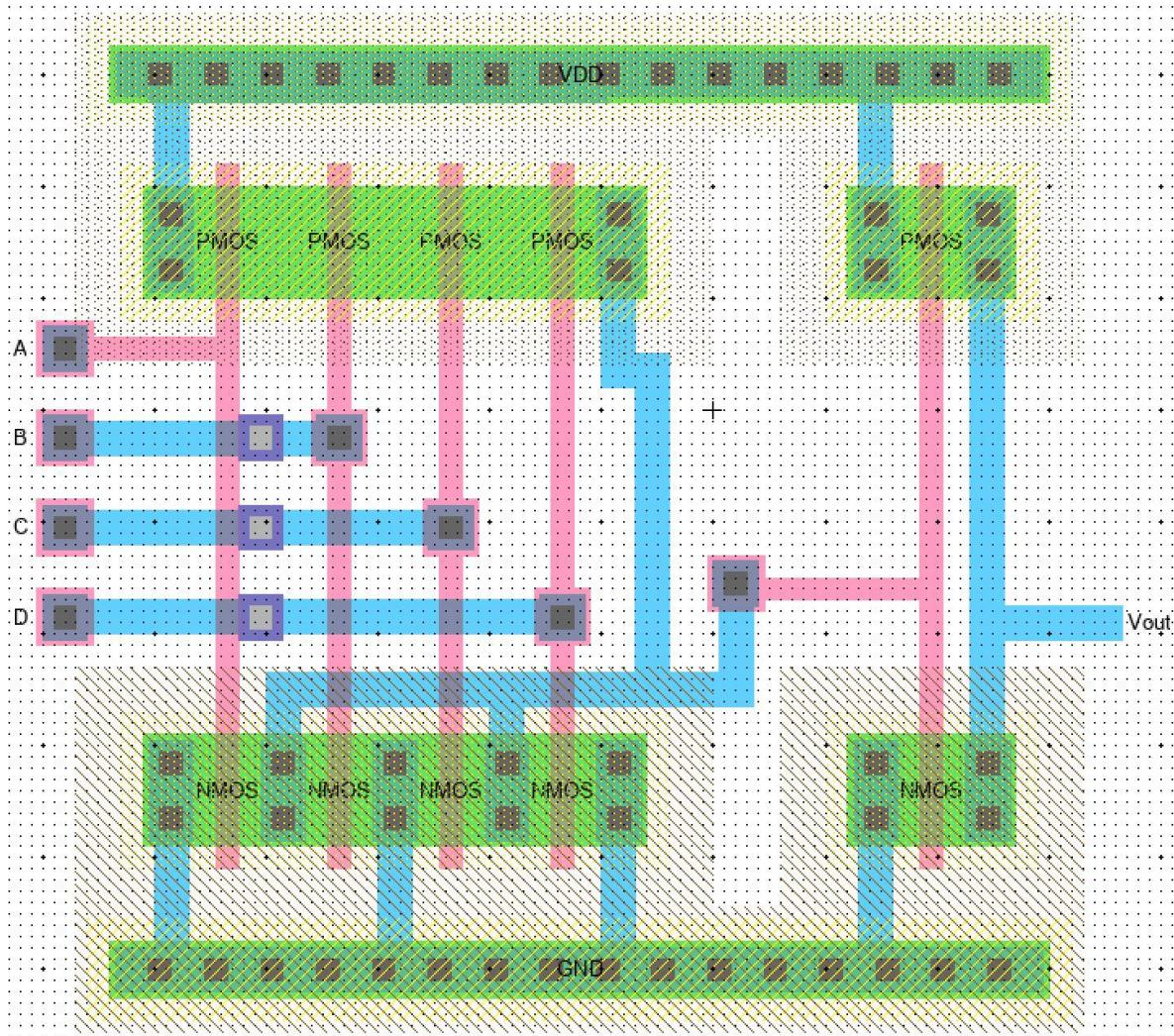


Figure 6: Layout Design of a Four Input OR Gate

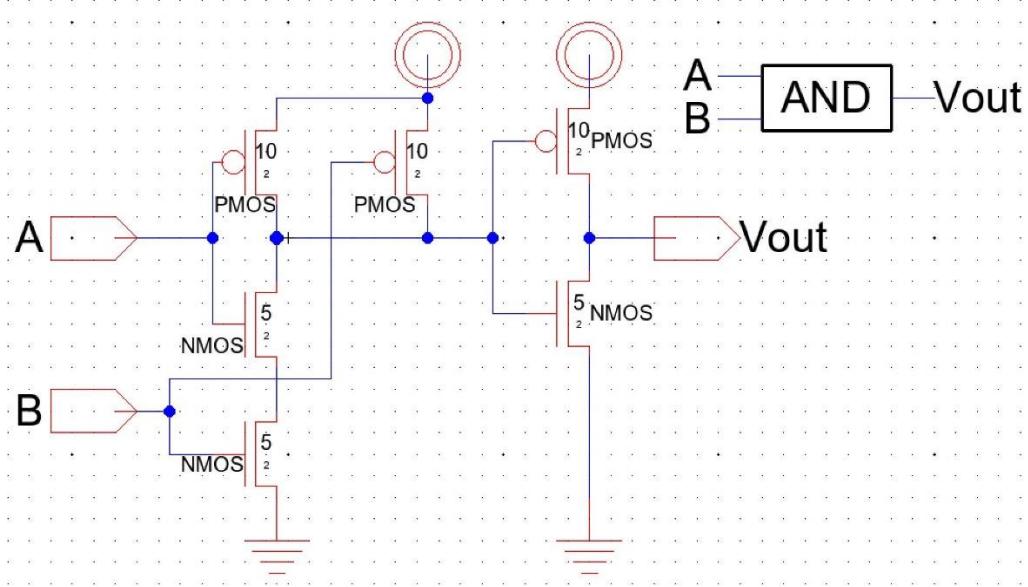


Figure 7: Schematic Design of a Two Input OR Gate That's Used

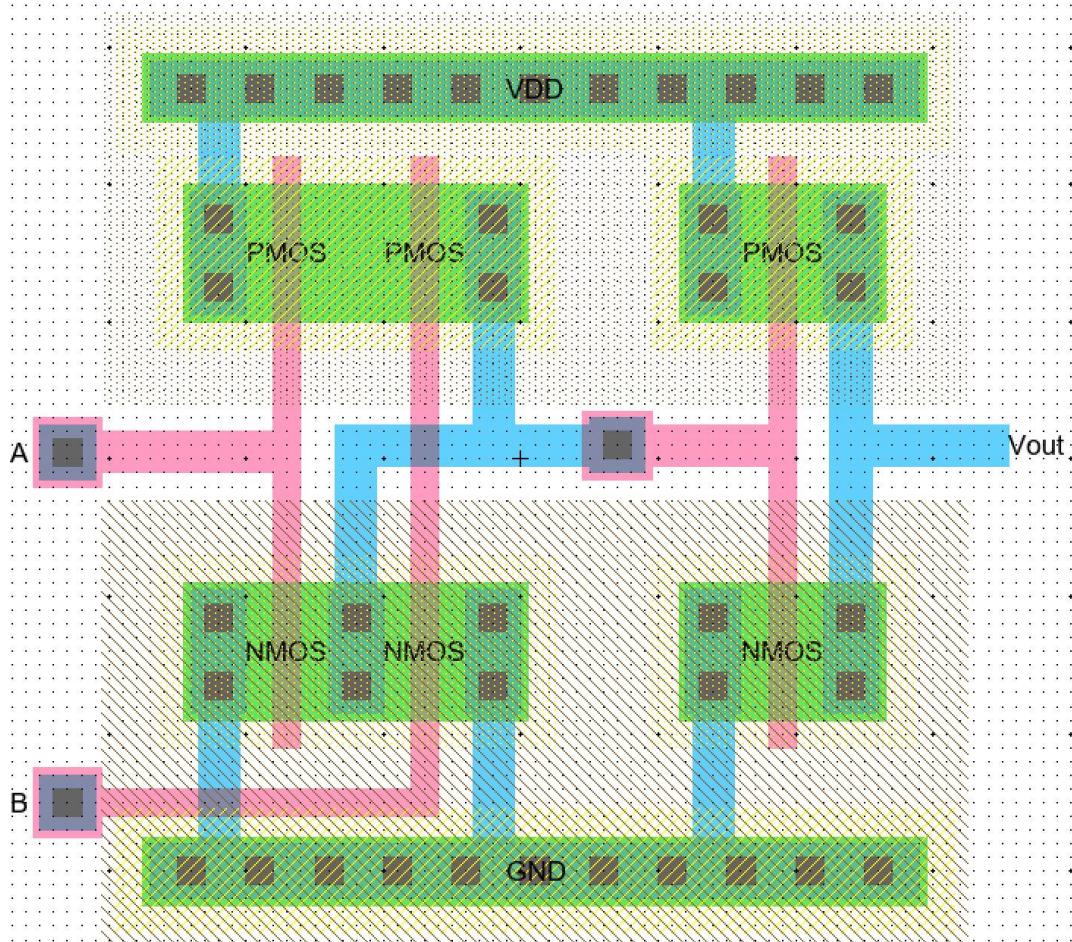


Figure 8: Layout Design of a Two Input AND Gate That's Used

Table 4: Truth Table of an Inverter

Input: In	Output: In NOT
0	1
1	0

Boolean Expression:

$$V_{out} = \overline{In}$$

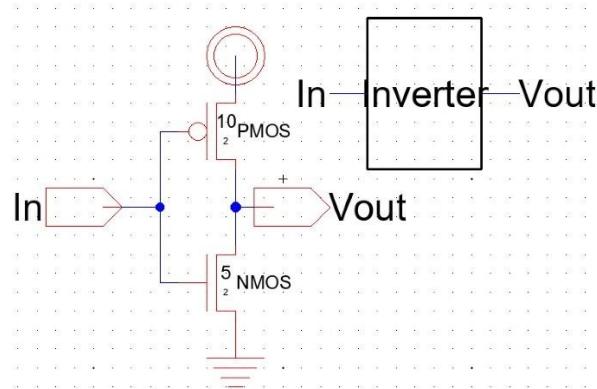


Figure 9: Schematic Design of an Inverter

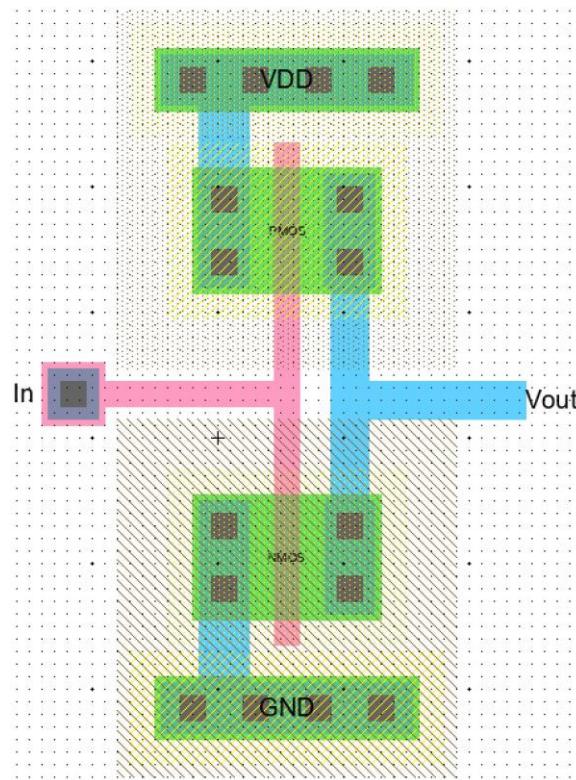


Figure 10: Layout Design of an Inverter

Table 5: Truth Table of a 4-to-1 Multiplexer

Input: S1	Input: S0	Output: 4-to-1 Multiplexer
0	0	A
0	1	B
1	0	C
1	1	D

Boolean Expression:

$$V_{out} = \overline{S_0} \overline{S_1} D_0 + S_0 \overline{S_1} D_1 + \overline{S_0} S_1 D_2 + S_0 S_1 D_3$$

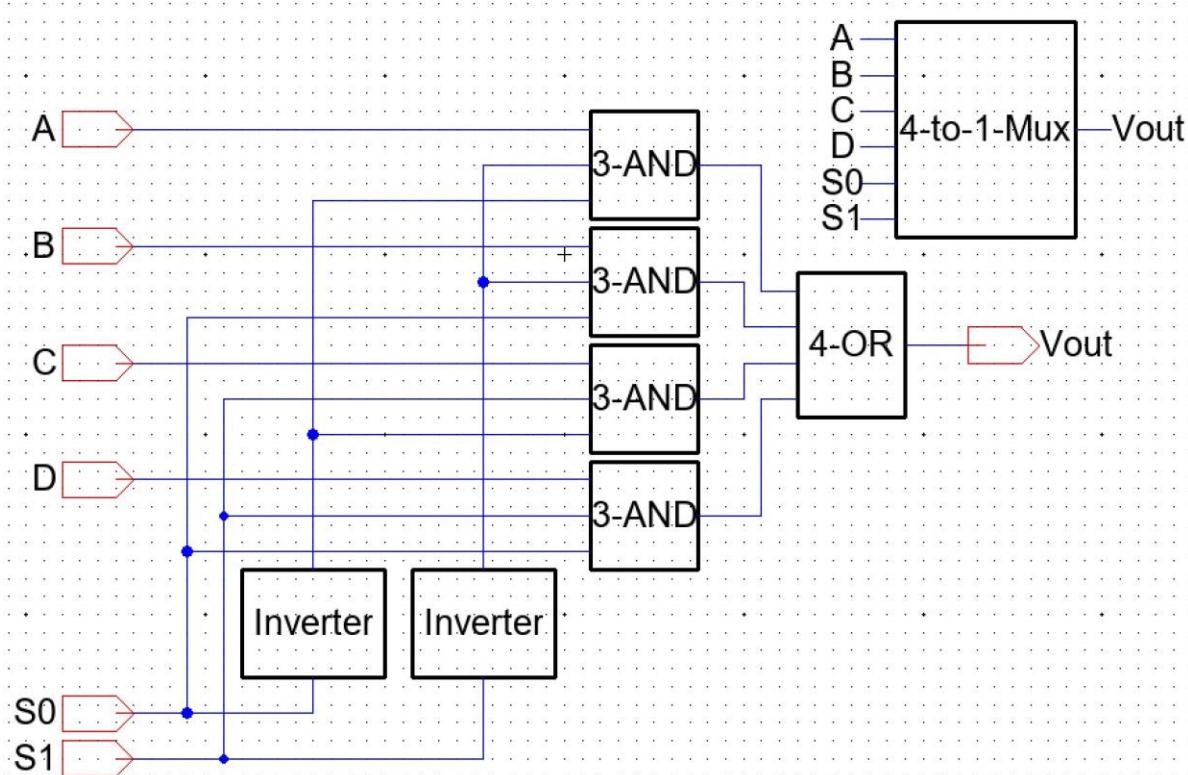


Figure 11: Schematic Design of a 4-to-1 Multiplexer

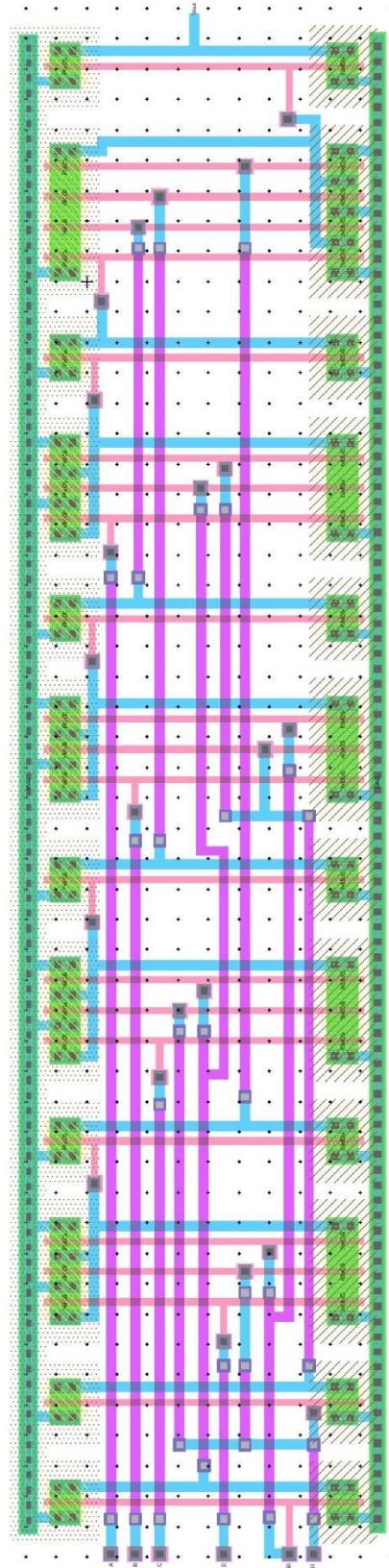


Figure 12.0: Layout Design of a 4-to-1 Multiplexer (Landscape)

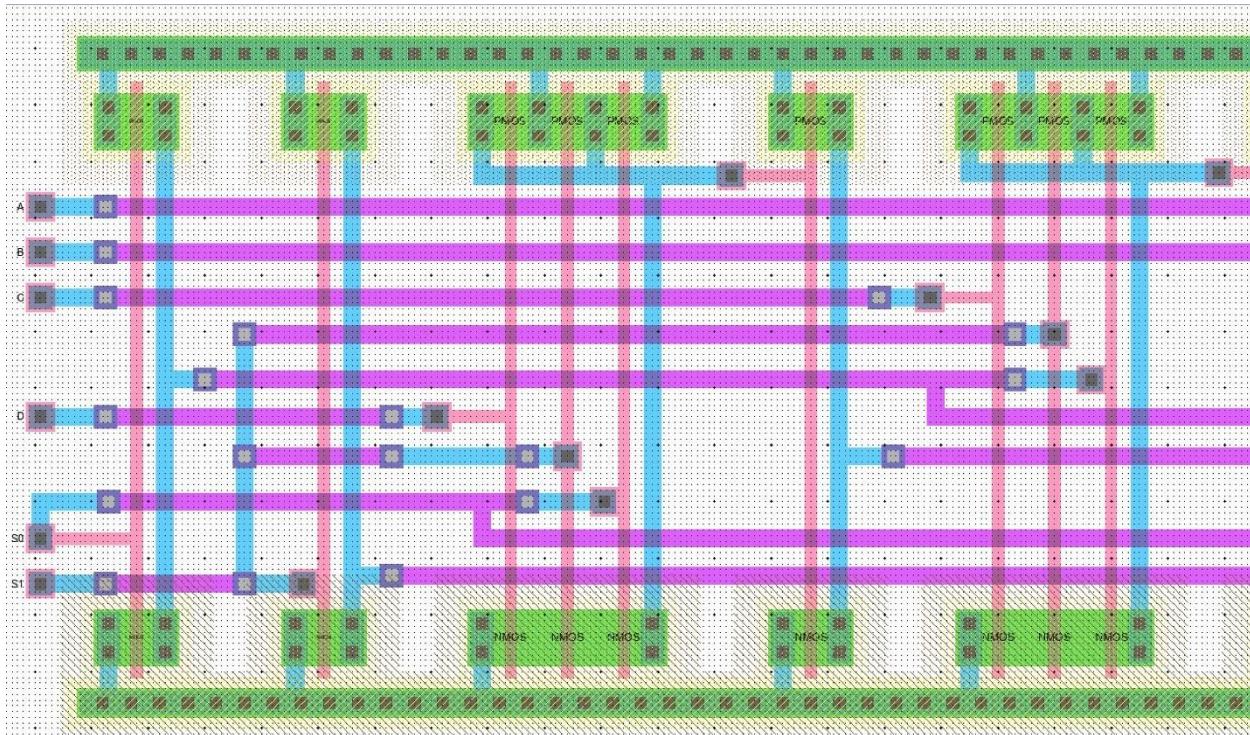


Figure 12.1: Layout Design of a 4-to-1 Multiplexer Zoomed (Left)

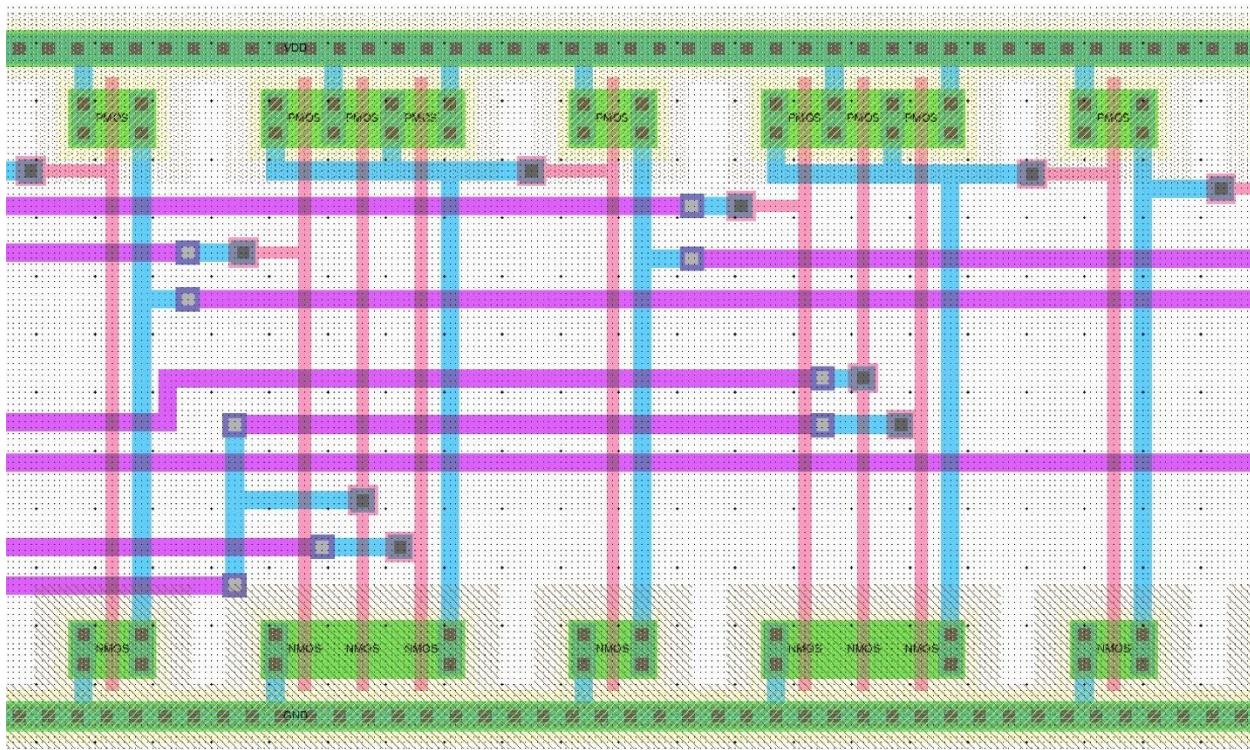


Figure 12.2: Layout Design of a 4-to-1 Multiplexer Zoomed (Middle)

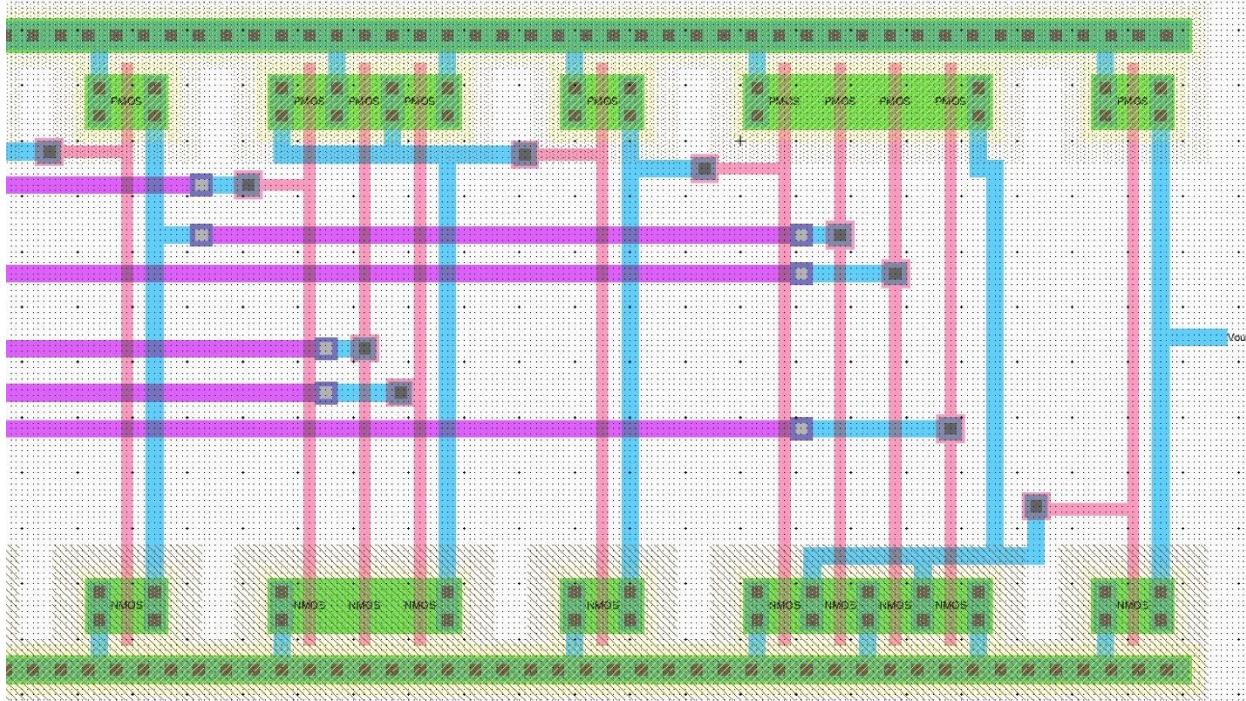


Figure 12.3: Layout Design of a 4-to-1 Multiplexer Zoomed (Right)

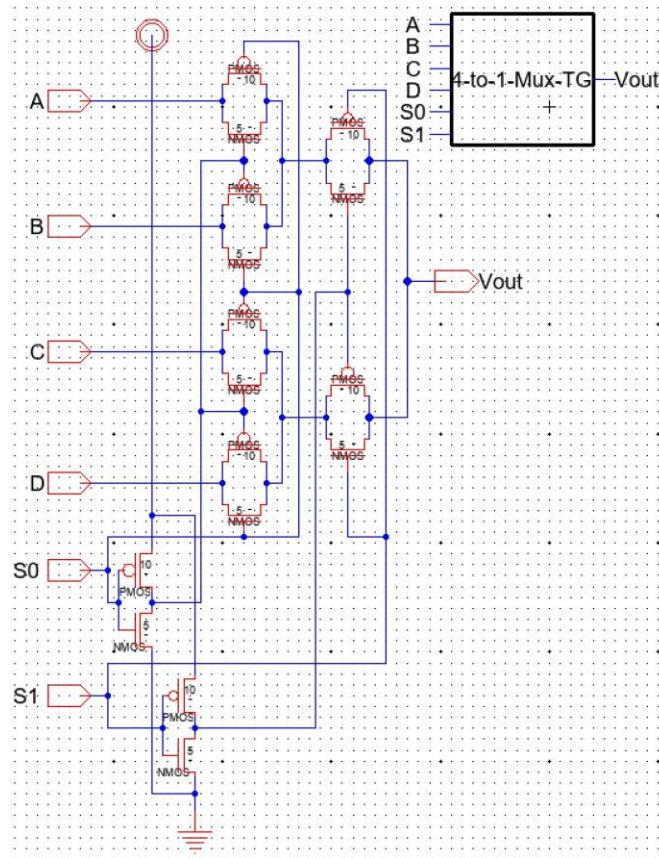


Figure 13: Schematic Design of a 4-to-1 Multiplexer Transmission Gate

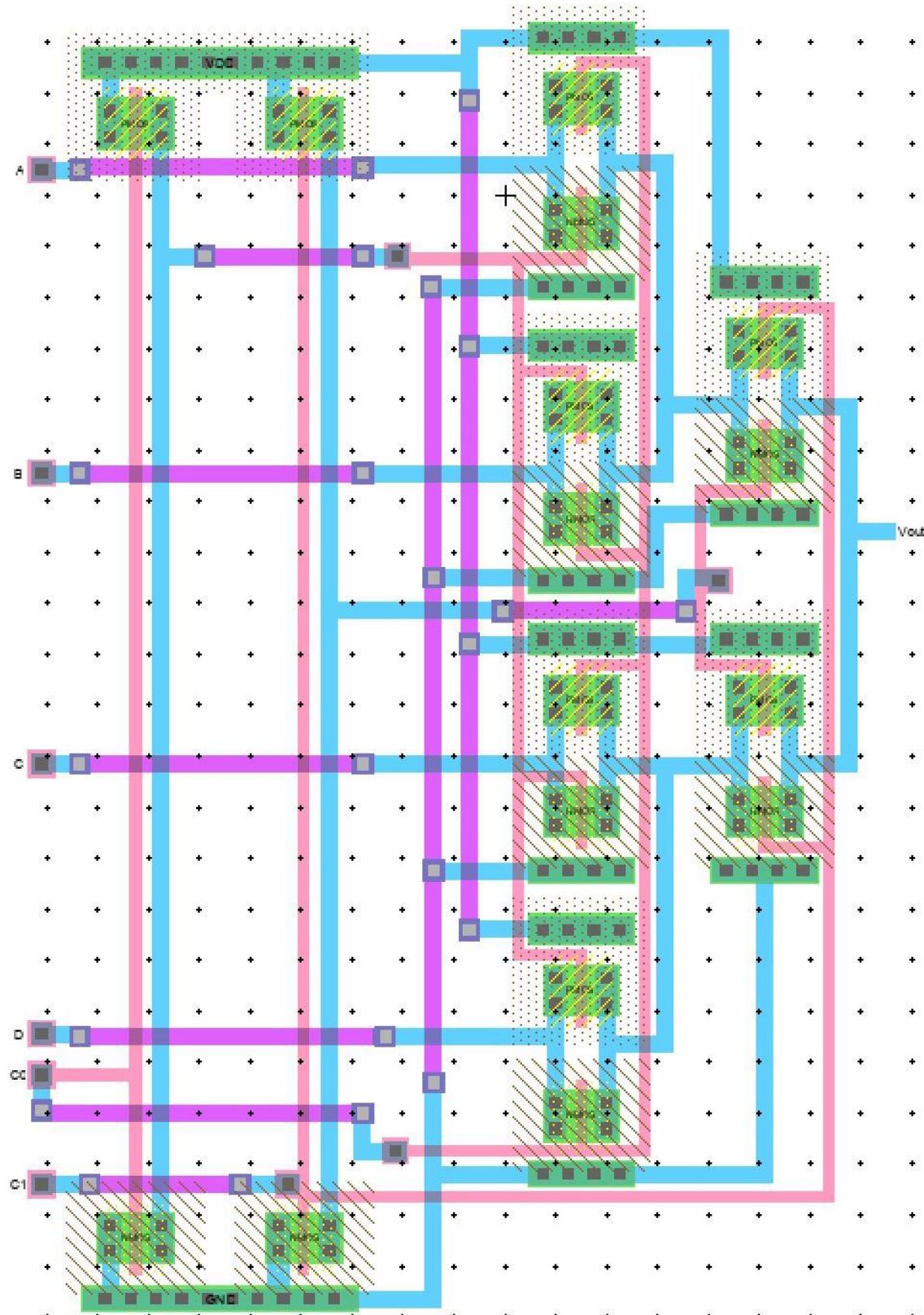


Figure 14.0: Layout Design of a 4-to-1 Multiplexer Transmission Gate

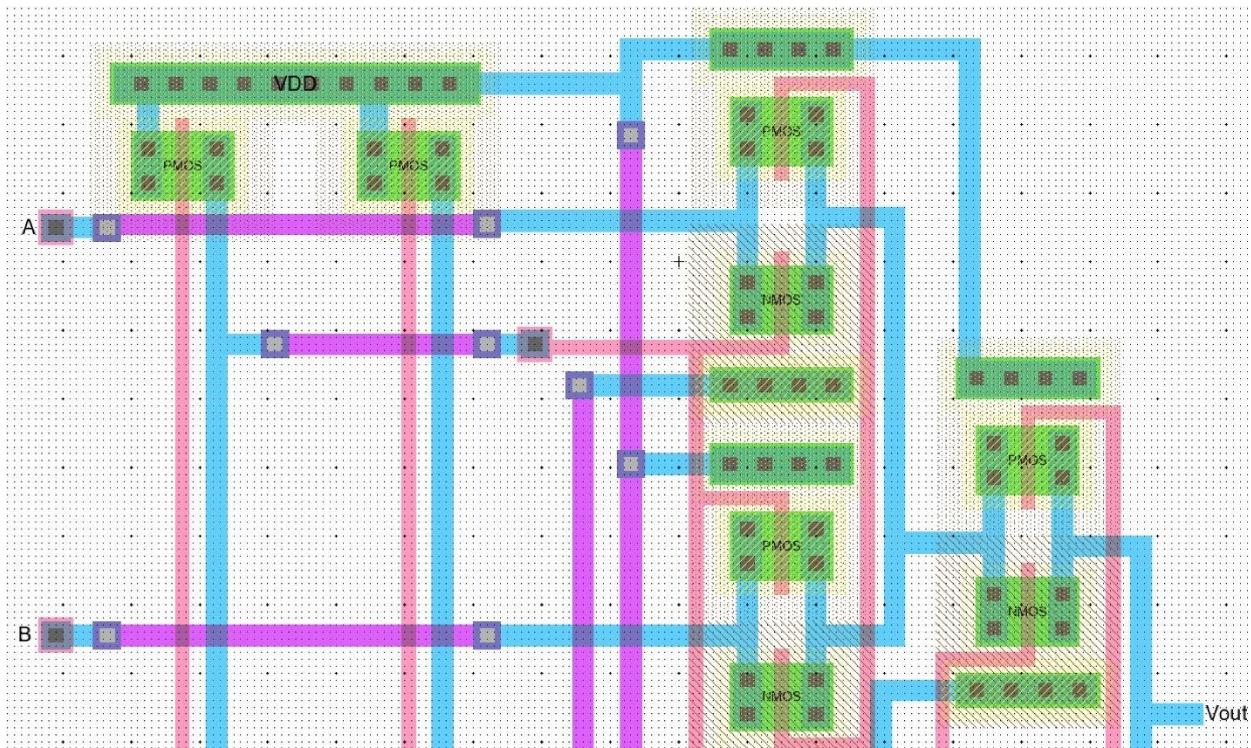


Figure 14.1: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Top)

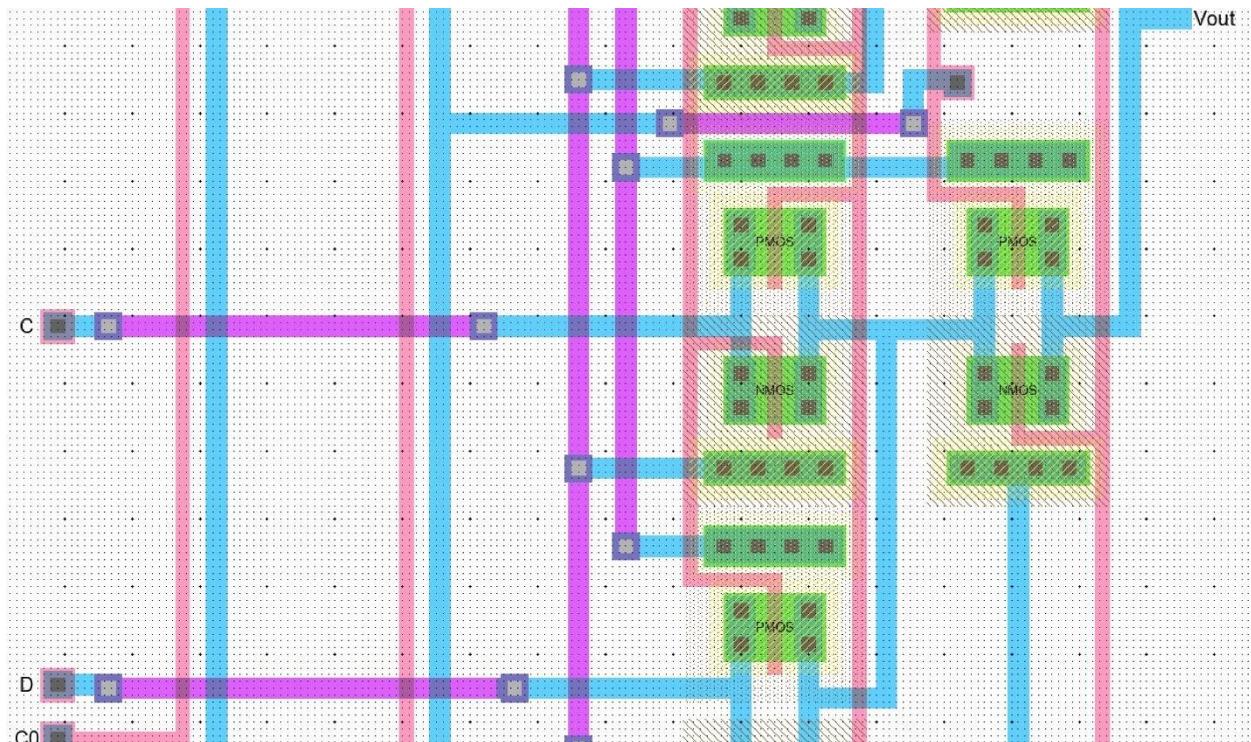


Figure 14.2: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Middle)

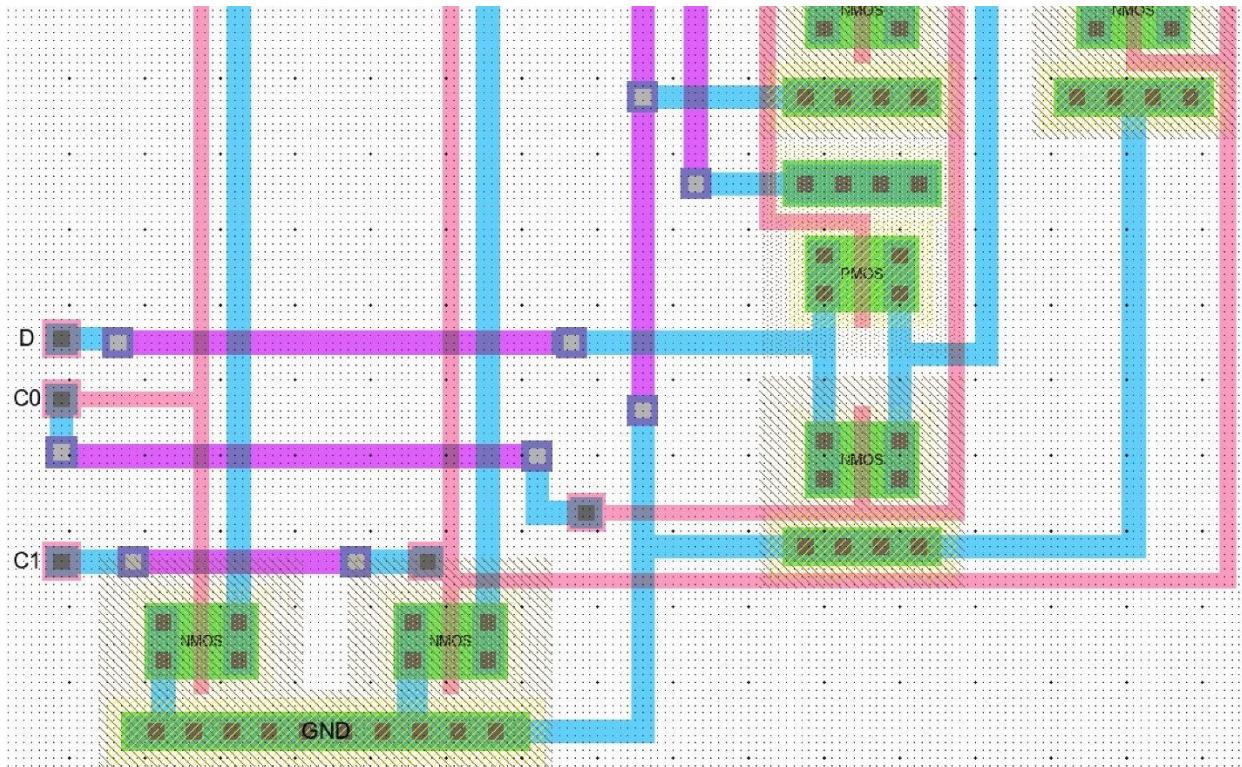


Figure 14.3: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Bottom)

Section 3: Electric Schematic:

We created a schematic of the conventional 16-to-1 Multiplexer by combining five 4-to-1 Multiplexers (Figure 11) together, using its icon. If there were any problems with the 4-to-1 Multiplexer, then we would have to go back to see the parts it was built from. In this case, the parts that it was built from are a two input AND gate, which becomes a three input AND gate, two input OR gate, which becomes a four input OR gate, and an inverter. It was combined by connecting the output of four 4-to-1 Multiplexer to the four inputs on another 4-to-1 Multiplexer. Figure 15 shows the schematic design that was built using Electric of the conventional 16-to-1 Multiplexer. Figure 16 shows the Design Rule Check (DRC) that was performed on the schematic for the conventional 16-to-1 Multiplexer; it indicates that there were no errors or warning with the schematic.

For the transmission gate 16-to-1 Multiplexer, it's created by combining five transmission gate 4-to-1 Multiplexer (Figure 13). It was combined by connecting the output of four transmission gate 4-to-1 Multiplexer to the four inputs on another transmission gate 4-to-1 Multiplexer. Figure 17 shows the schematic design that was built using Electric of the transmission gate 16-to-1 Multiplexer. Figure 18 shows the Design Rule Check (DRC) that was performed on the schematic for the transmission gate 16-to-1 Multiplexer; it indicates that there were no errors or warning with the schematic.

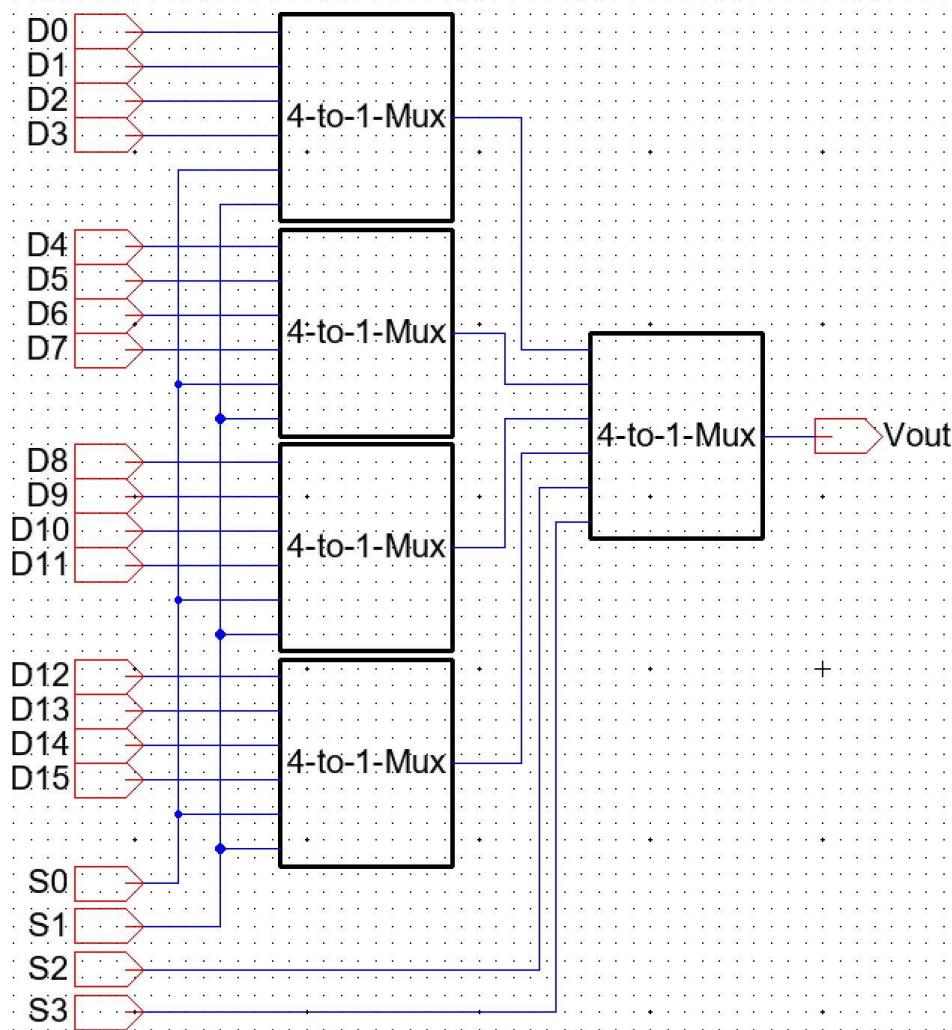


Figure 15: Schematic Design of a 16-to-1 Multiplexer

Electric Messages

```
=====
Checking schematic cell 'AND{sch}'
  No errors found
Checking schematic cell '3-AND{sch}'
  No errors found
Checking schematic cell 'OR{sch}'
  No errors found
Checking schematic cell '4-OR{sch}'
  No errors found
Checking schematic cell 'Inverter{sch}'
  No errors found
Checking schematic cell '4-to-1-Mux{sch}'
  No errors found
Checking schematic cell '16-to-1-Mux{sch}'
  No errors found
0 errors and 0 warnings found (took 0.031 secs)
```

Figure 16: Design Rule Check (DRC) of a 16-to-1 Multiplexer Schematic Design

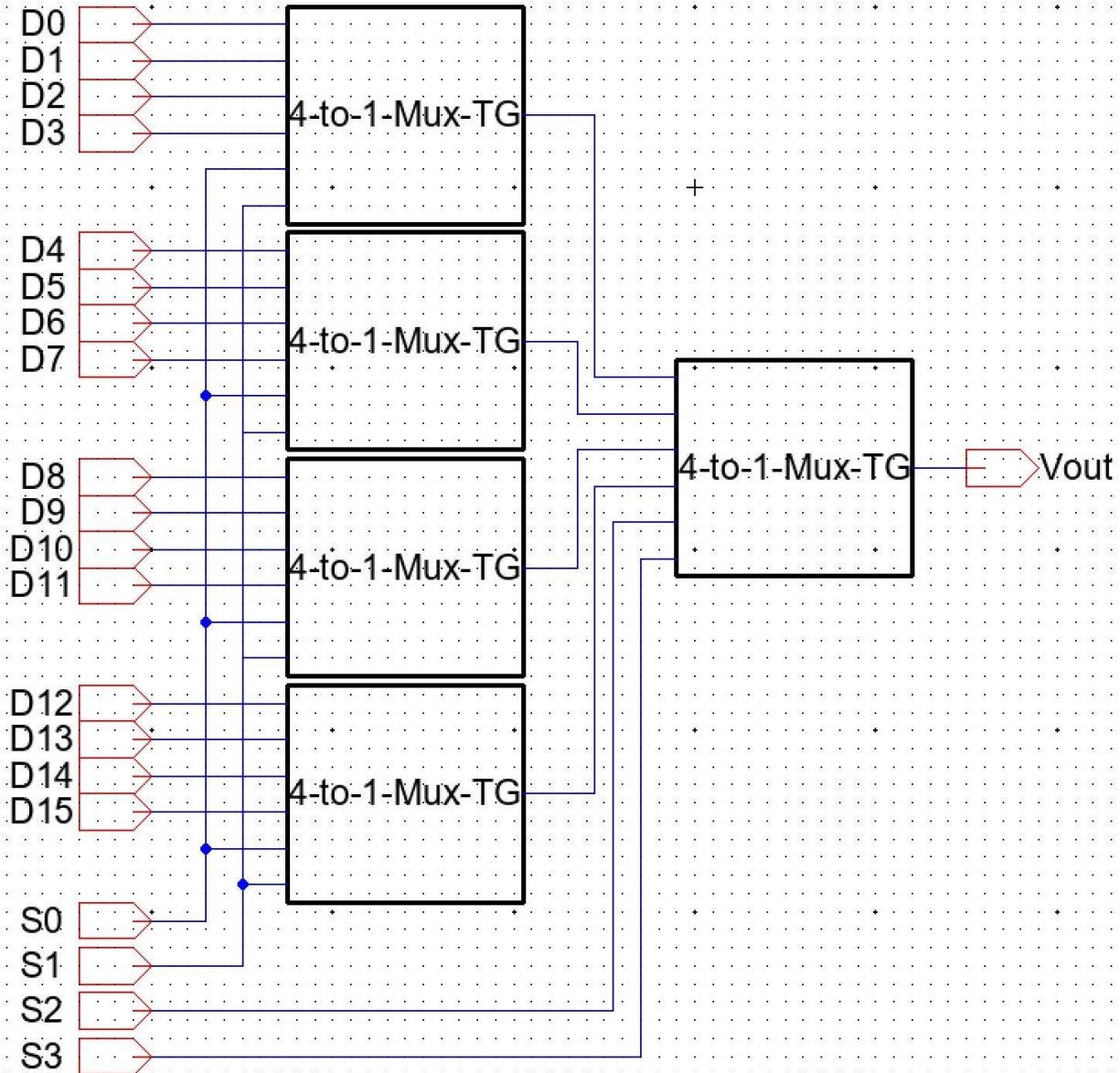


Figure 17: Schematic Design of a 16-to-1 Multiplexer Transmission Gate

Electric Messages

```
=====
9
Checking schematic cell '4-to-1-Mux-TG{sch}'
  No errors found
Checking schematic cell '16-to-1-Mux-TG{sch}'
  No errors found
0 errors and 0 warnings found (took 0.031 secs)
```

Figure 18: Design Rule Check (DRC) of a 16-to-1 Multiplexer Transmission Gate Schematic Design

Section 4: Electric Layout:

We created a layout of the conventional 16-to-1 Multiplexer by combining five 4-to-1 Multiplexers (Figure 12) together. If there were any problems with the 4-to-1 Multiplexer, then we would have to go back to see the parts it was built from. In this case, the parts that it was built from are a two input AND gate, which becomes a three input AND gate, two input OR gate, which becomes a four input OR gate, and an inverter. It was combined by connecting the output of four 4-to-1 Multiplexer to the four inputs on another 4-to-1 Multiplexer. Figure 19 shows the layout design that was built using Electric of the conventional 16-to-1 Multiplexer. There is an overview and a zoomed version of the layout since the overview isn't clear enough. In addition, if additional justifications are needed, refer to Figure 12. Figure 20 shows the Design Rule Check (DRC) and Well Check that was performed on the layout for the conventional 16-to-1 Multiplexer; it indicates that there were no errors or warning with the layout.

For the transmission gate 16-to-1 Multiplexer, it's created by combining five transmission gate 4-to-1 Multiplexer (Figure 14). It was combined by connecting the output of four transmission gate 4-to-1 Multiplexer to the four inputs on another transmission gate 4-to-1 Multiplexer. Figure 21 shows the layout design that was built using Electric of the transmission gate 16-to-1 Multiplexer. There is an overview and a zoomed version of the layout since the overview isn't clear enough. In addition, if additional justifications are needed, refer to Figure 14. Figure 22 shows the Design Rule Check (DRC) and Well Check that was performed on the layout for the transmission gate 16-to-1 Multiplexer; it indicates that there were no errors or warning with the layout.

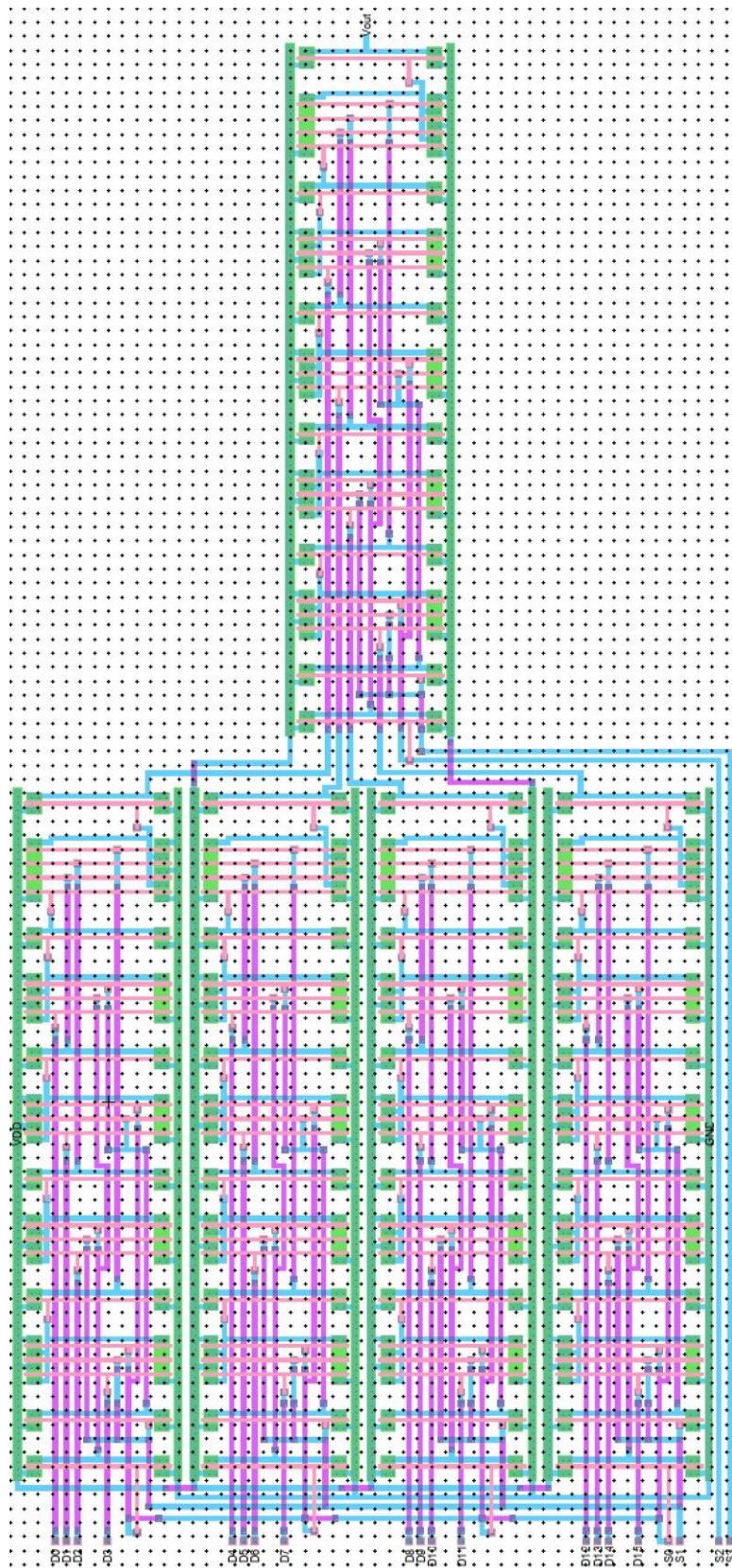


Figure 19.0: Layout Design of a 16-to-1 Multiplexer (Landscape)

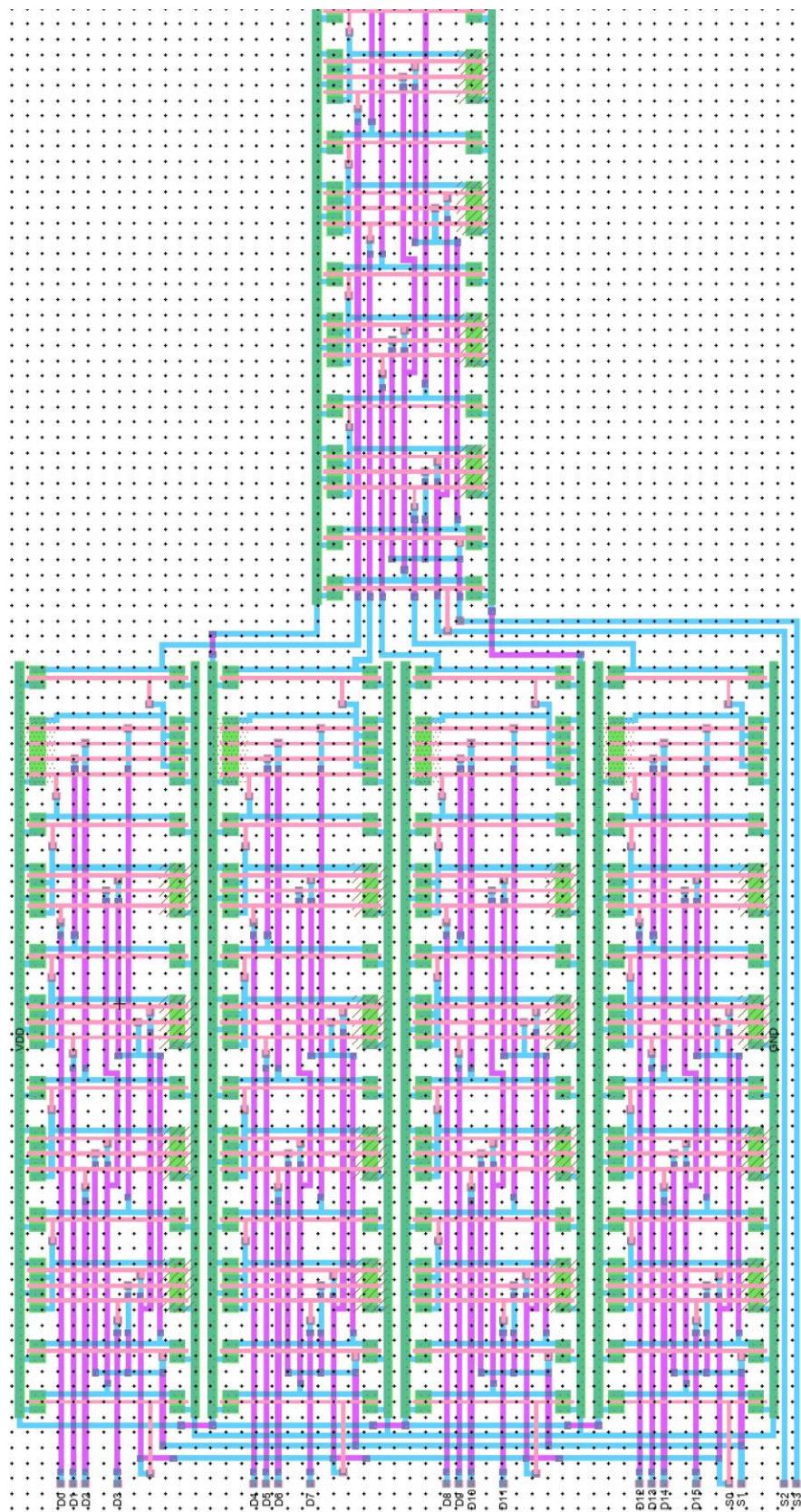


Figure 19.1: Layout Design of a 16-to-1 Multiplexer Zoomed (Landscape)

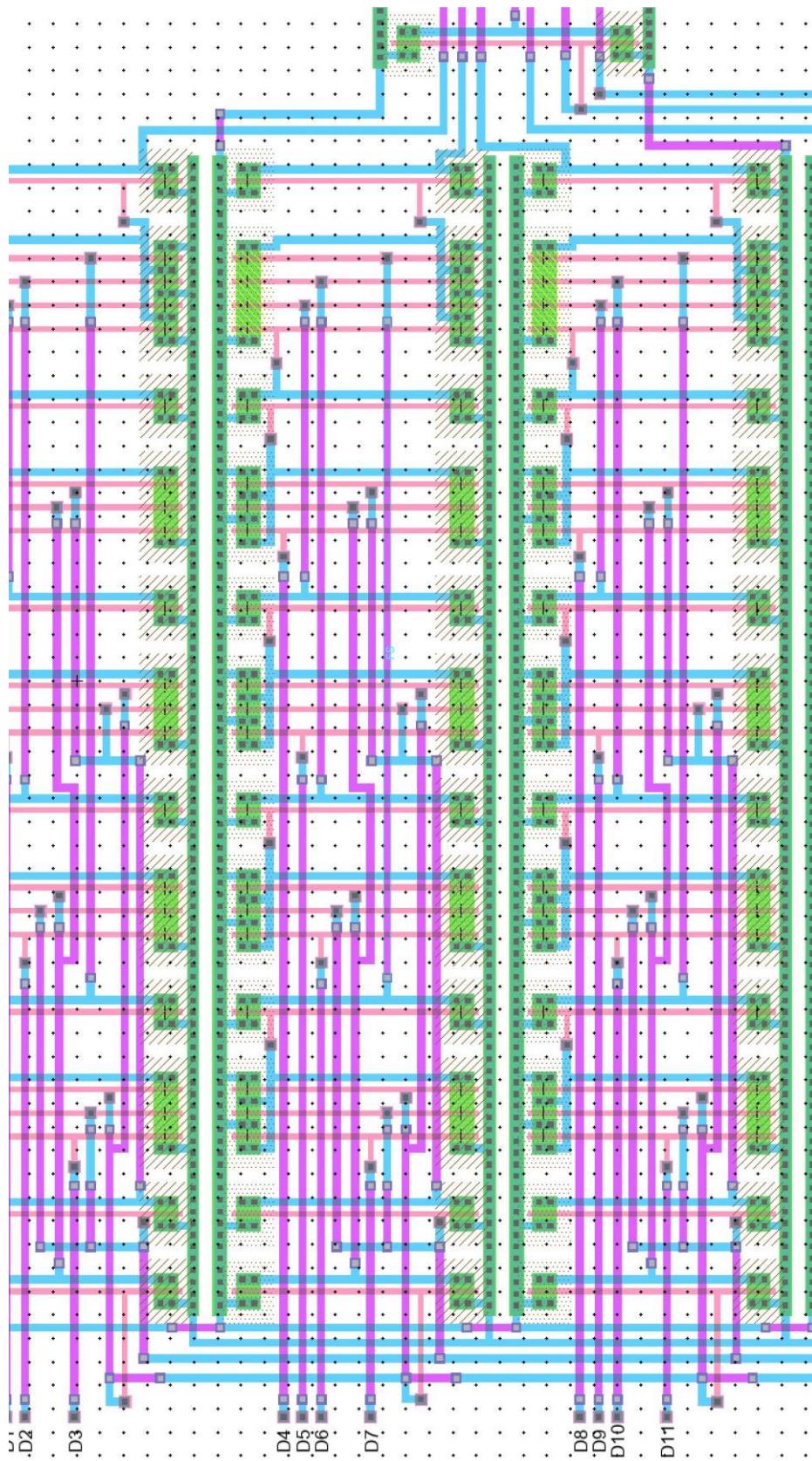


Figure 19.2: Layout Design of a 16-to-1 Multiplexer Zoomed (Landscape)

```
Electric Messages
=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.016 secs)
Found 368 networks
Checking cell '16-to-1-Mux{lay}'
    No errors/warnings found
0 errors and 0 warnings found (took 4.329 secs)
=====
Checking Wells and Substrates in '16-to-1-Mux:16-to-1-Mux{lay}' ...
    Geometry collection found 940 well pieces, took 0.101 secs
    Geometry analysis used 4 threads and took 0.022 secs
NetValues propagation took 0.0 secs
Checking short circuits in 10 well contacts
    Additional analysis took 0.0 secs
No Well errors found (took 0.123 secs)
```

Figure 20: Design Rule Check (DRC) and Well Check of a 16-to-1 Multiplexer Layout Design

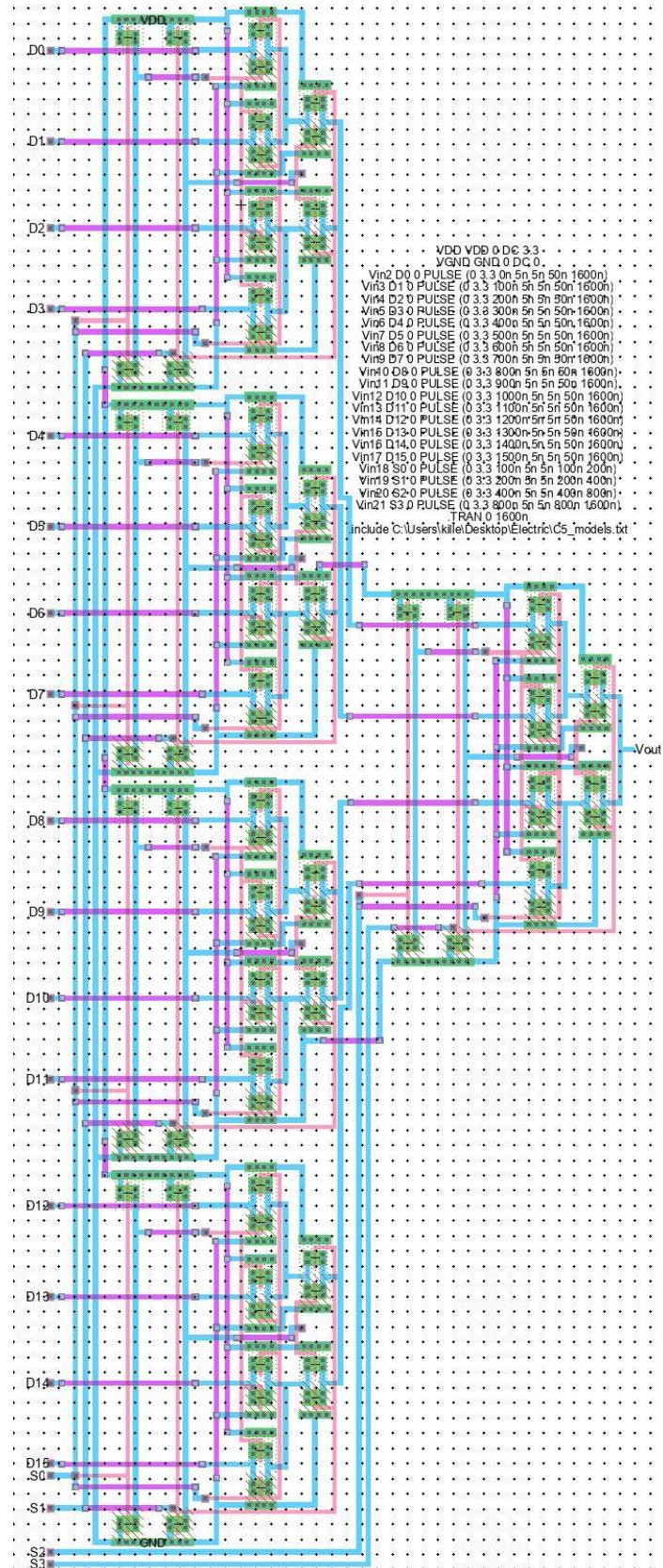


Figure 21.0: Layout Design of a Transmission Gate 16-to-1 Multiplexer

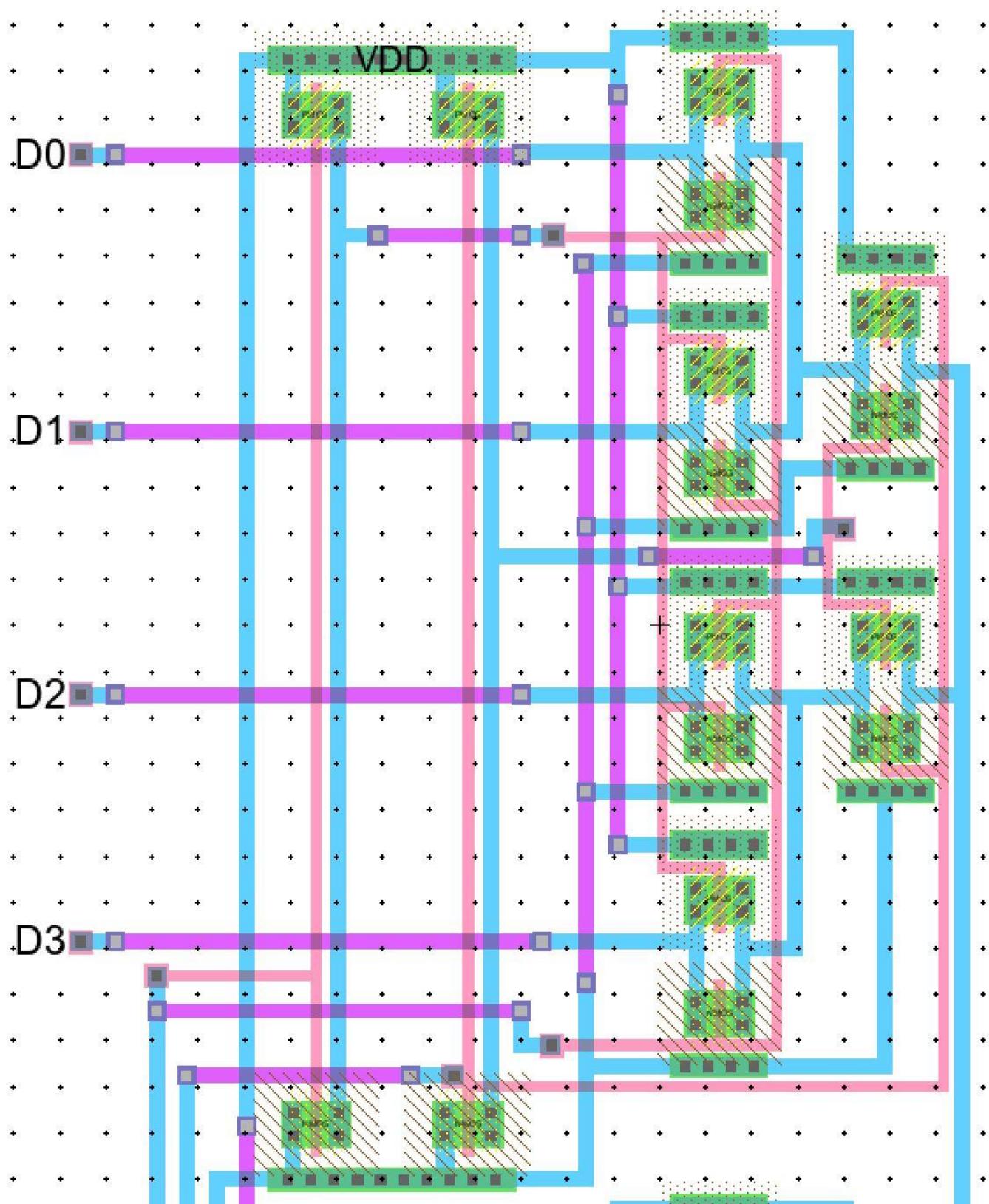


Figure 21.1: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Top)

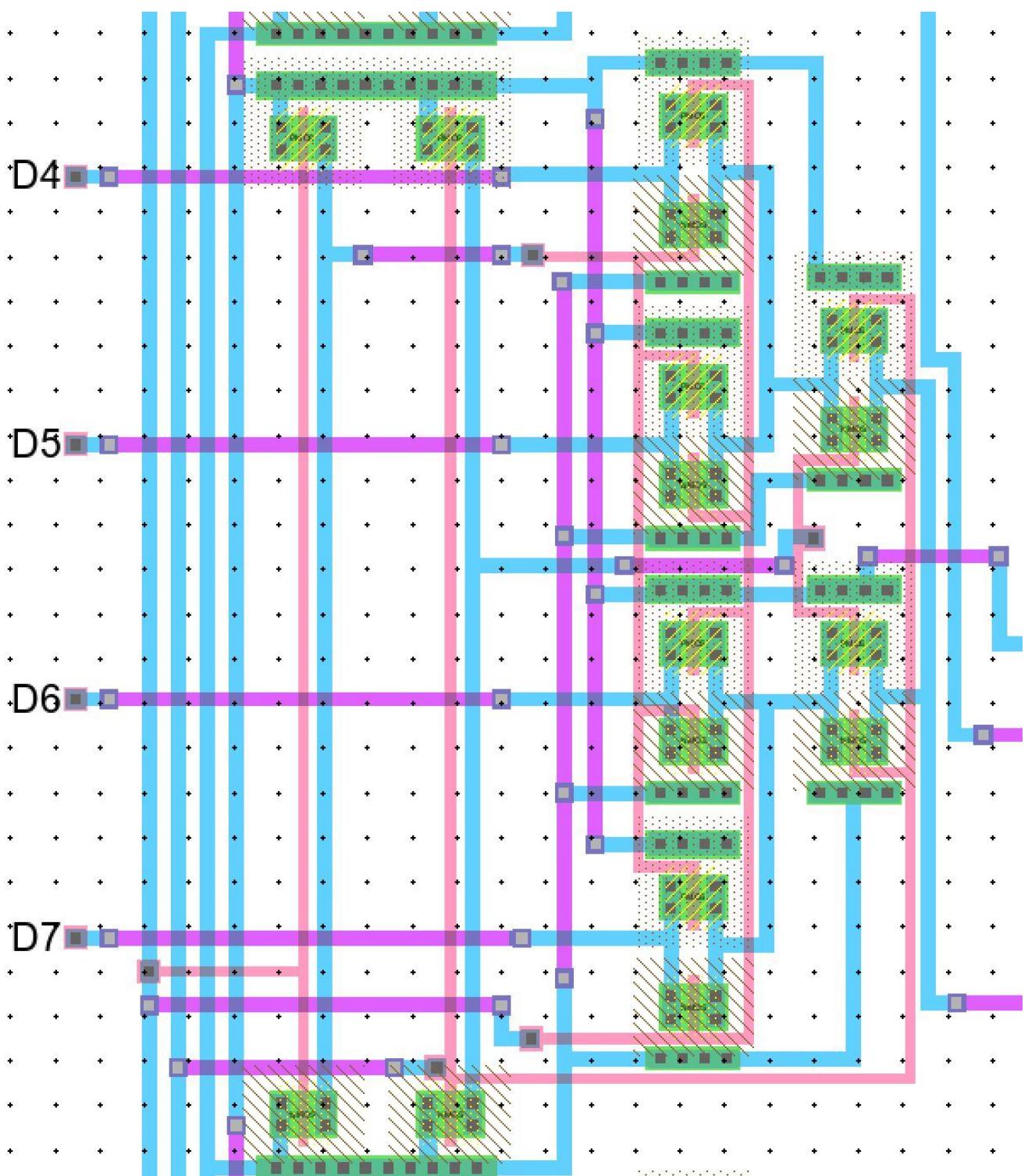


Figure 21.2: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Middle Left)

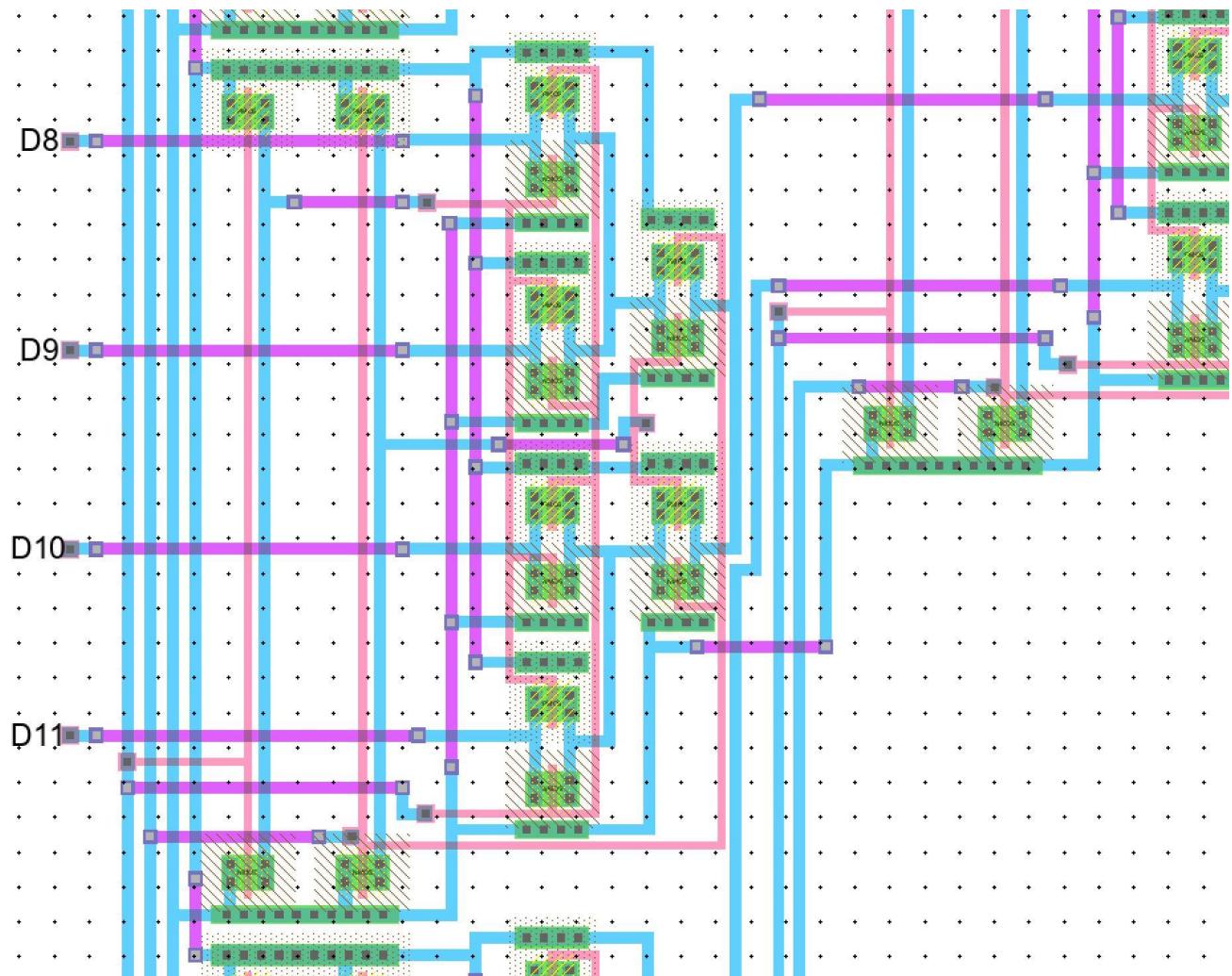


Figure 21.3: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Middle Left)

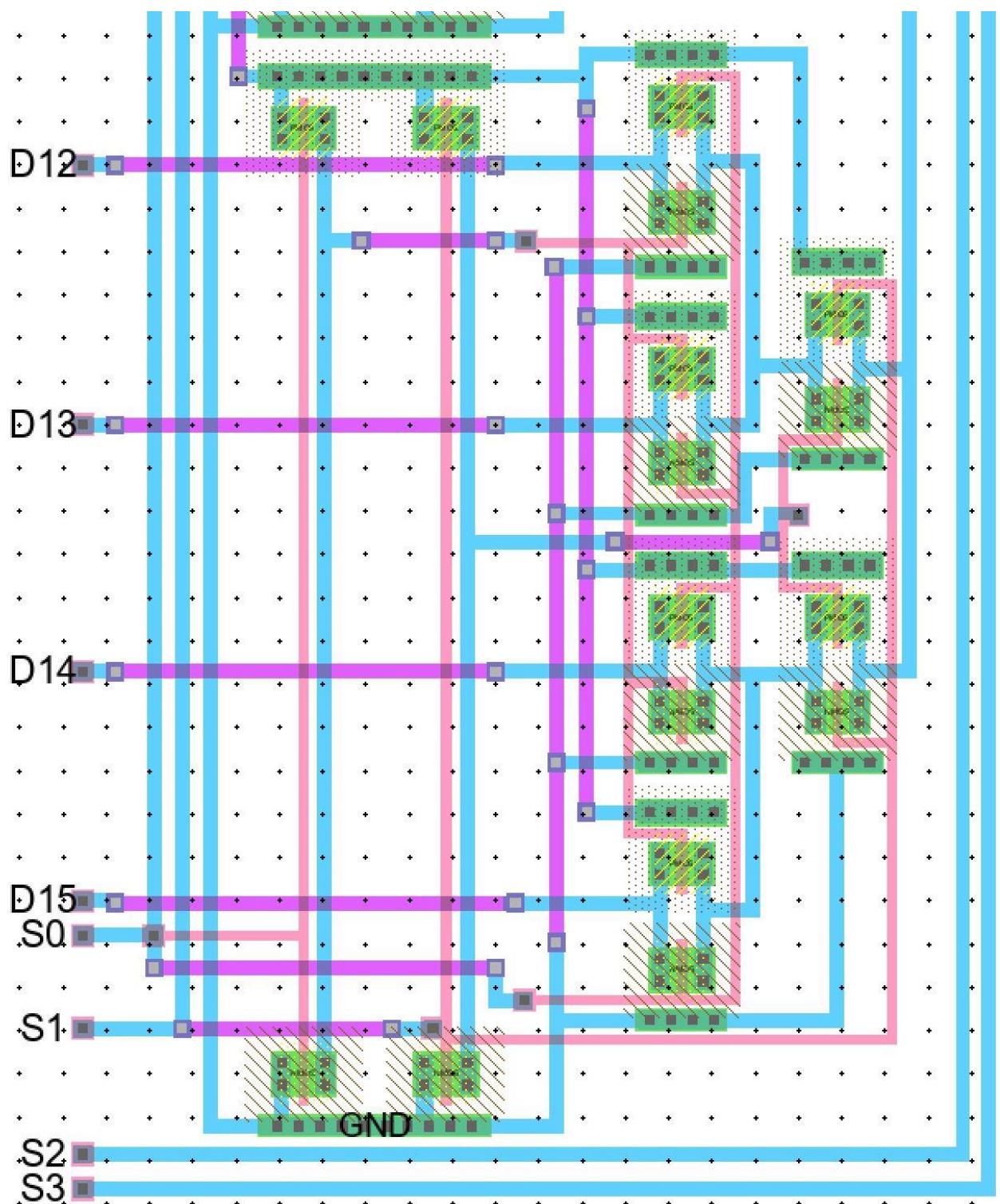


Figure 21.4: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Bottom)

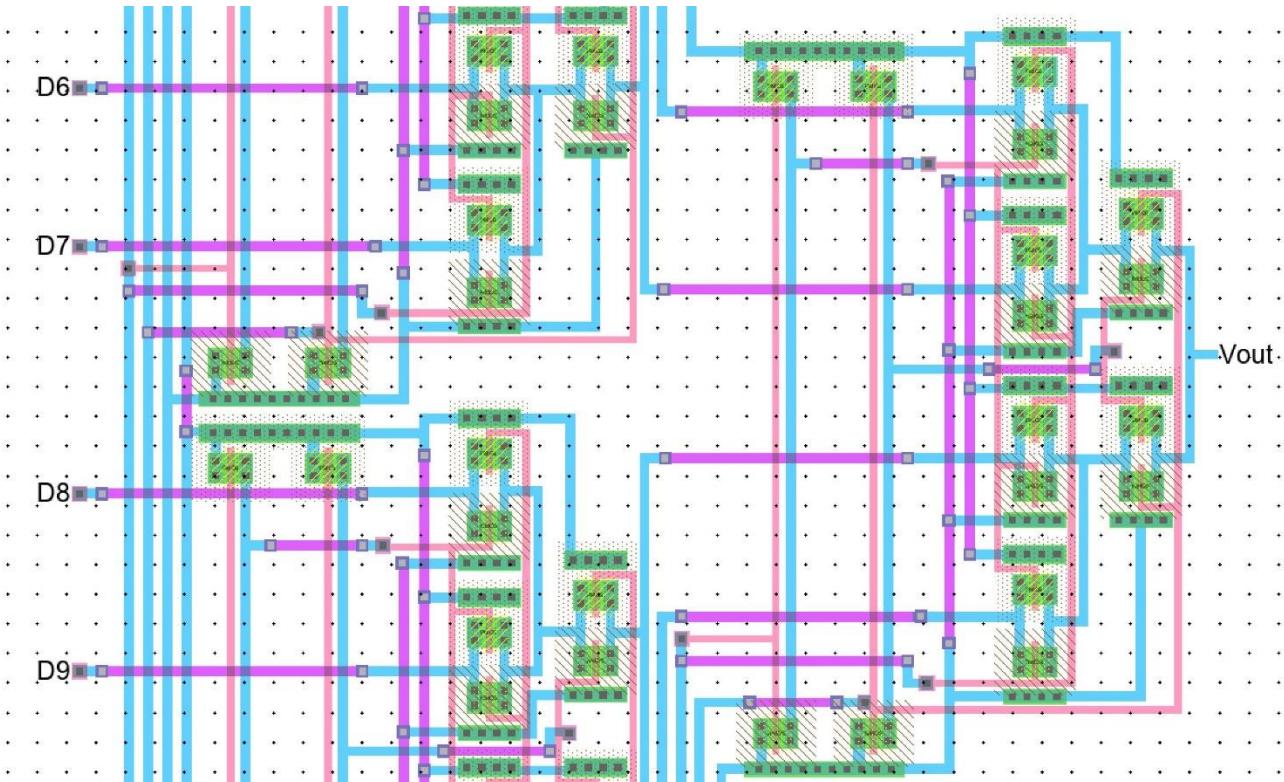


Figure 21.5: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Middle)

```

Electric Messages
=====
10
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 128 networks
Checking cell '16-to-1-Mux-TG{lay}'
    No errors/warnings found
0 errors and 0 warnings found (took 1.108 secs)
=====
11
Checking Wells and Substrates in '16-to-1-Mux:16-to-1-Mux-TG{lay}' ...
    Geometry collection found 470 well pieces, took 0.015 secs
    Geometry analysis used 4 threads and took 0.022 secs
    NetValues propagation took 0.0 secs
    Checking short circuits in 70 well contacts
        Additional analysis took 0.0 secs
    No Well errors found (took 0.037 secs)

```

Figure 22: Design Rule Check (DRC) and Well Check of a Transmission Gate 16-to-1 Multiplexer Layout Design

Section 5: IRSIM Simulations:

After creating the schematic and layout design of the 16-to-1 Multiplexer, waveforms were created using IRSIM. These waveforms were created by configuring the inputs, D0-D15, and S0-S3, so that it could test certain computations. The computations that it tested are the same between the schematic and layout. When setting in values for the inputs, the output would automatically update based on the inputs. We were able to verify the waveforms obtained from IRSIM were correct by matching it with the truth table on Table 1.

Section 5.1: Schematic:

For the schematic, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the selectors and counting the peaks for the one that's selected and comparing it with the output.

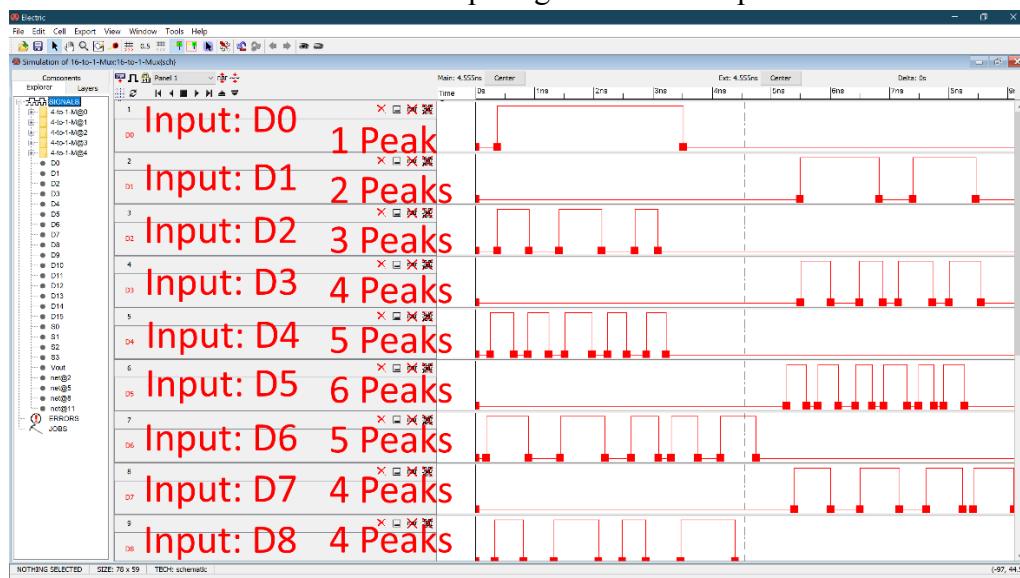


Figure 23.1: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer

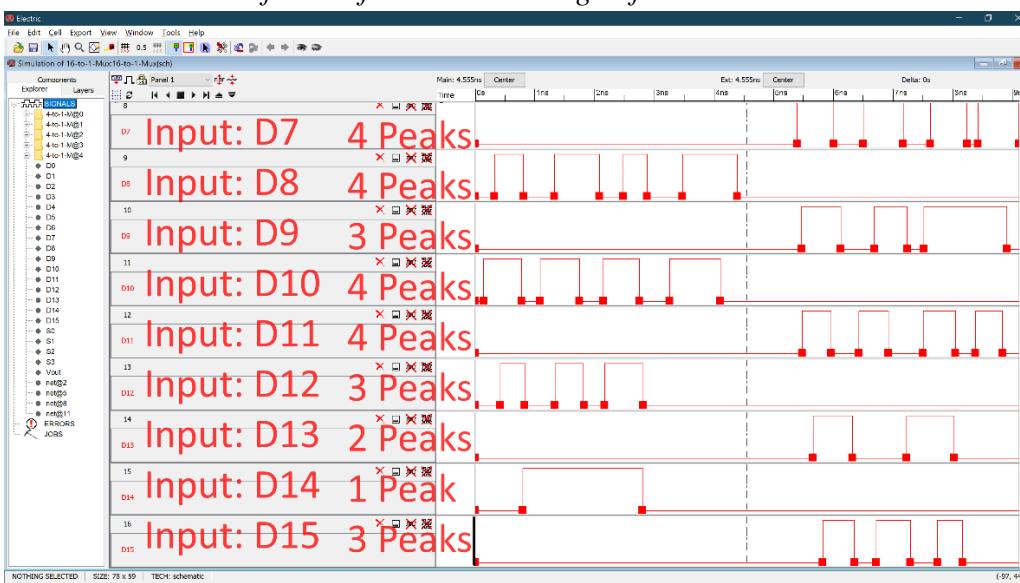


Figure 23.2: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer

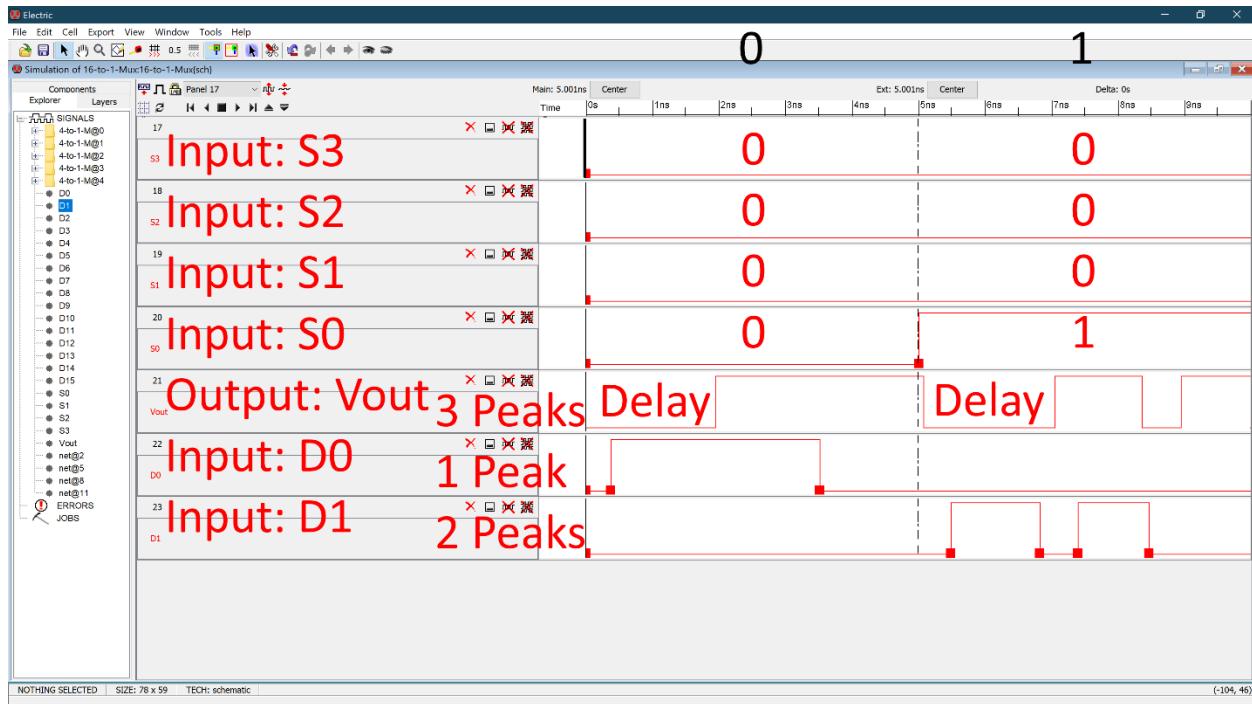


Figure 23.3: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer
(Selector at 0 and 1)

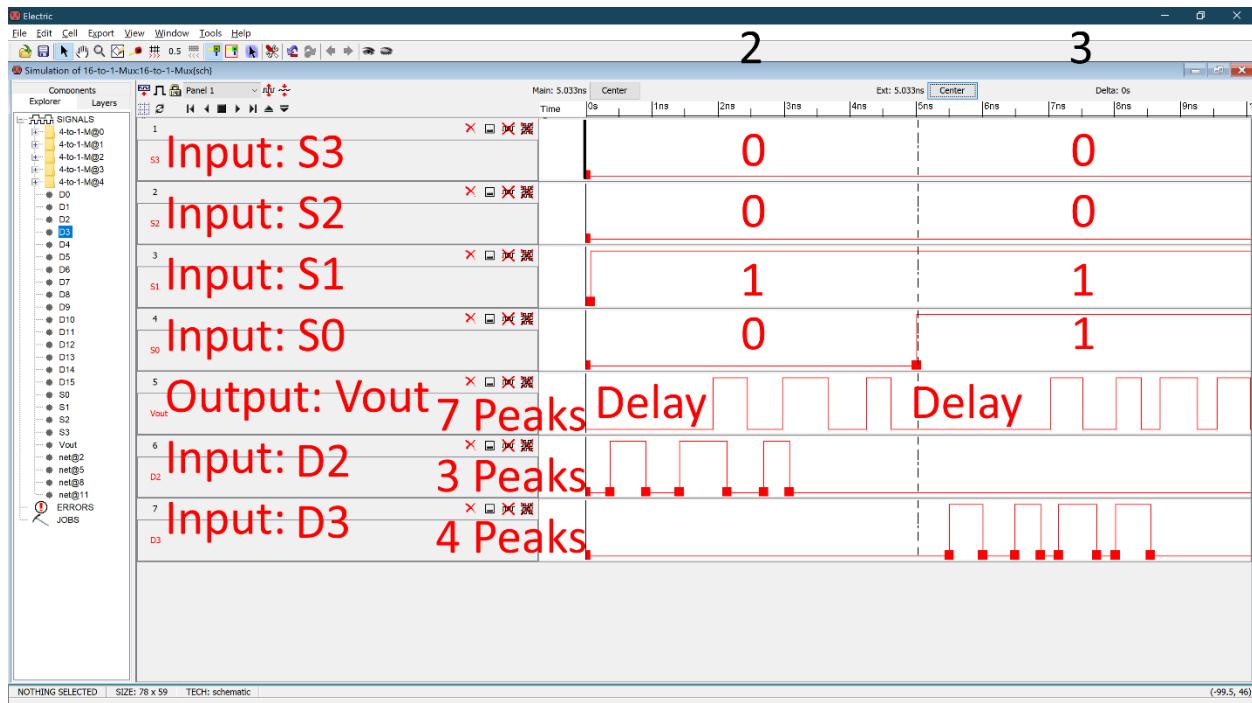


Figure 23.4: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer
(Selector at 2 and 3)

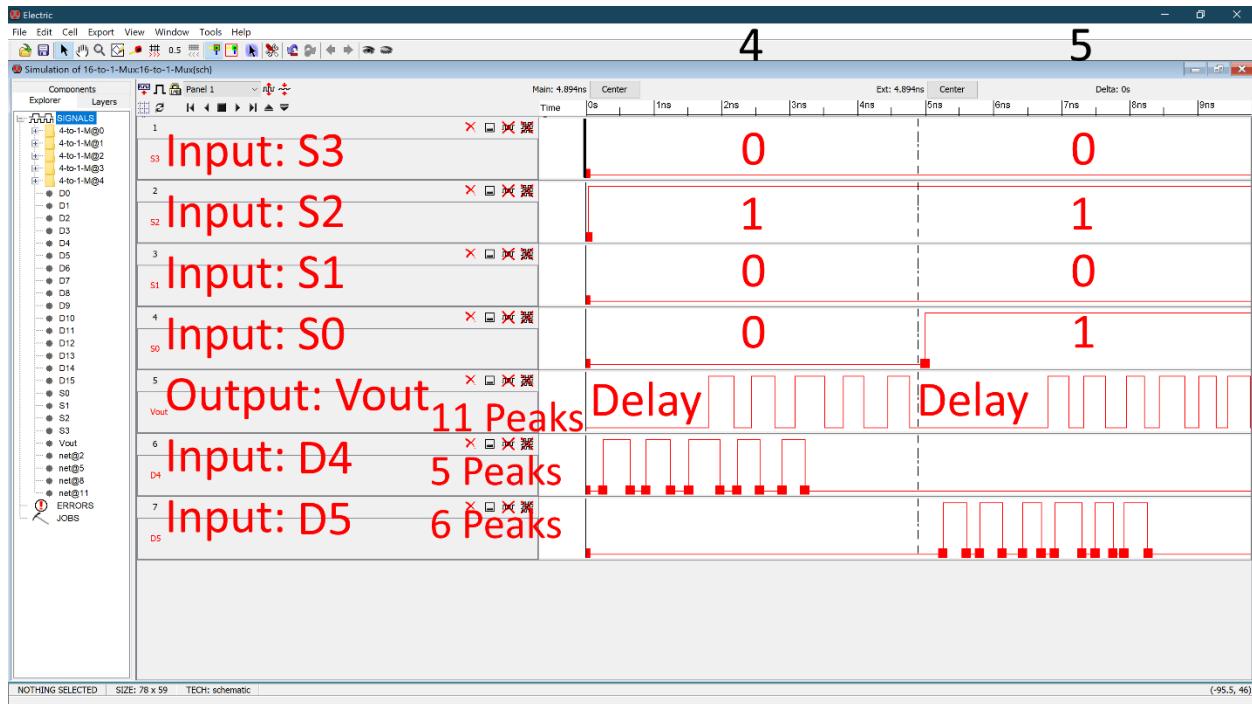


Figure 23.5: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer
(Selector at 4 and 5)

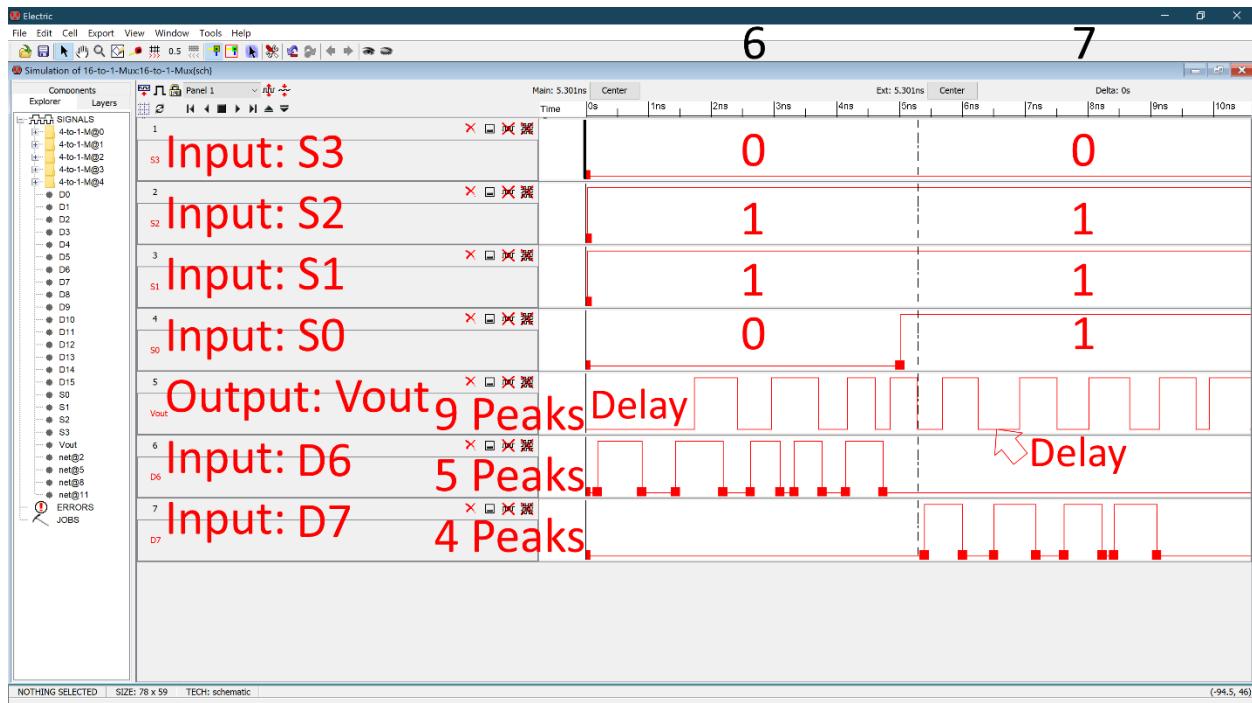


Figure 23.6: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer
(Selector at 6 and 7)

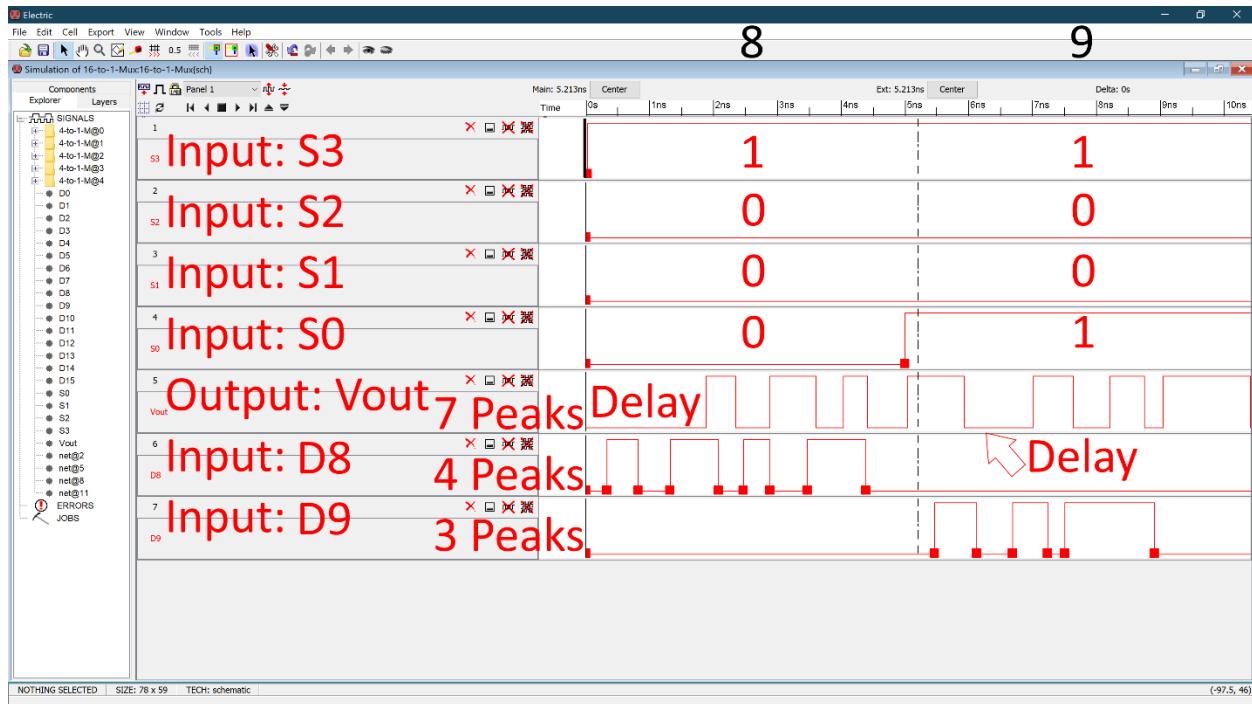


Figure 23.7: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer
(Selector at 8 and 9)

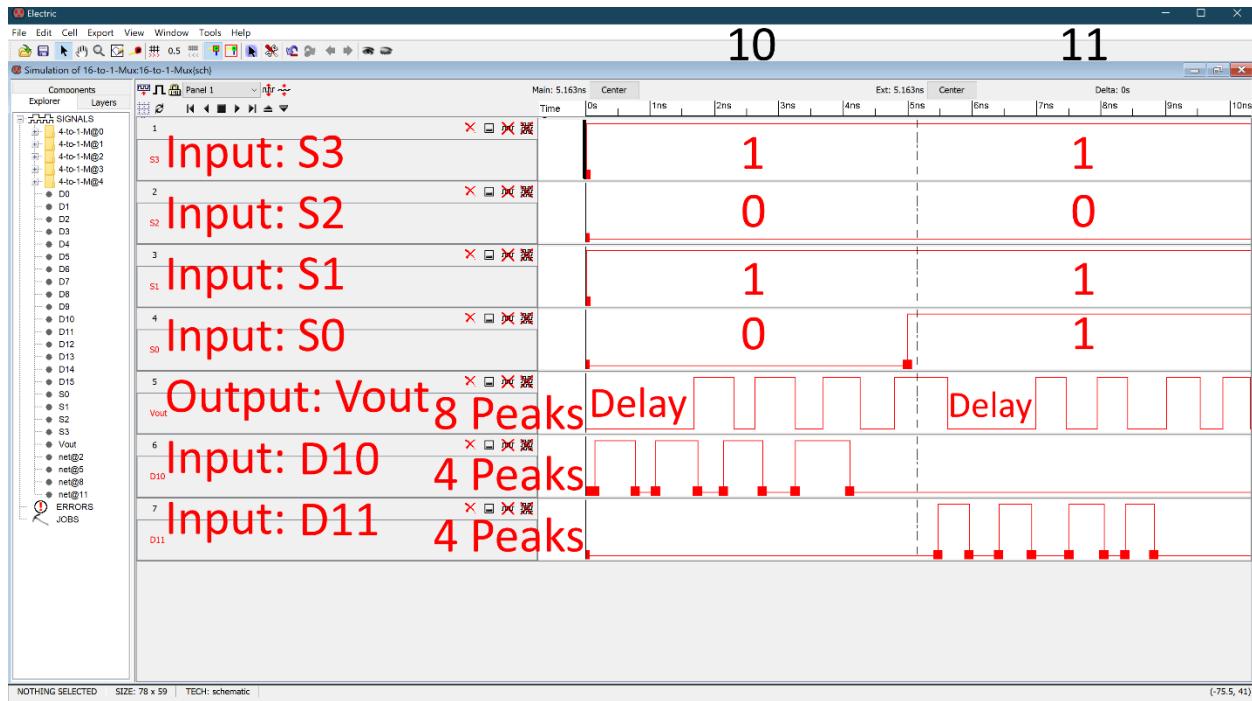


Figure 23.8: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer
(Selector at 10 and 11)

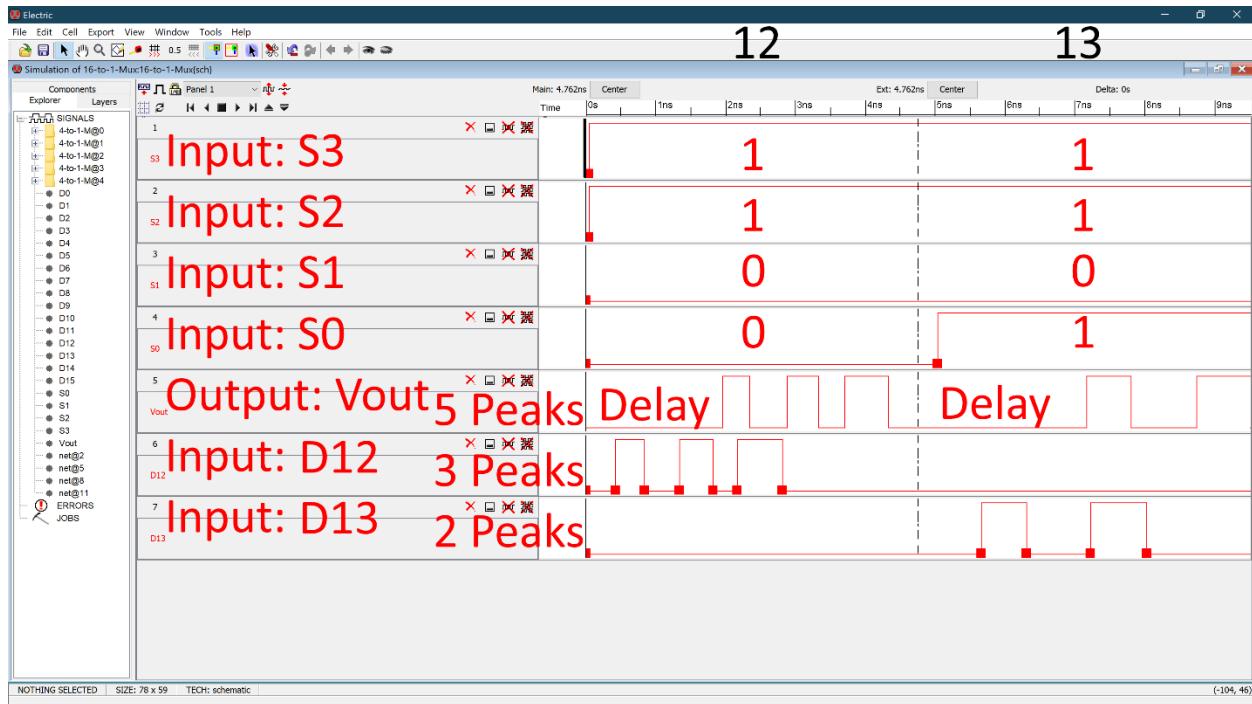


Figure 23.9: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer
(Selector at 12 and 13)

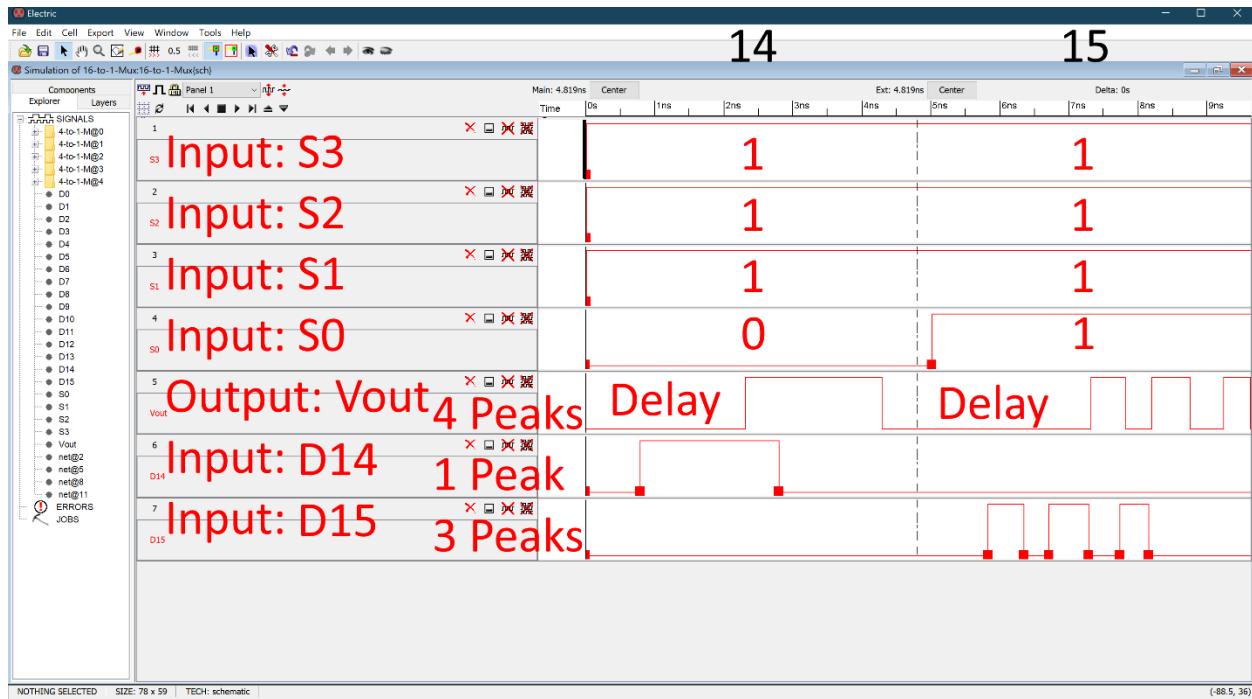


Figure 23.10: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer
(Selector at 14 and 15)

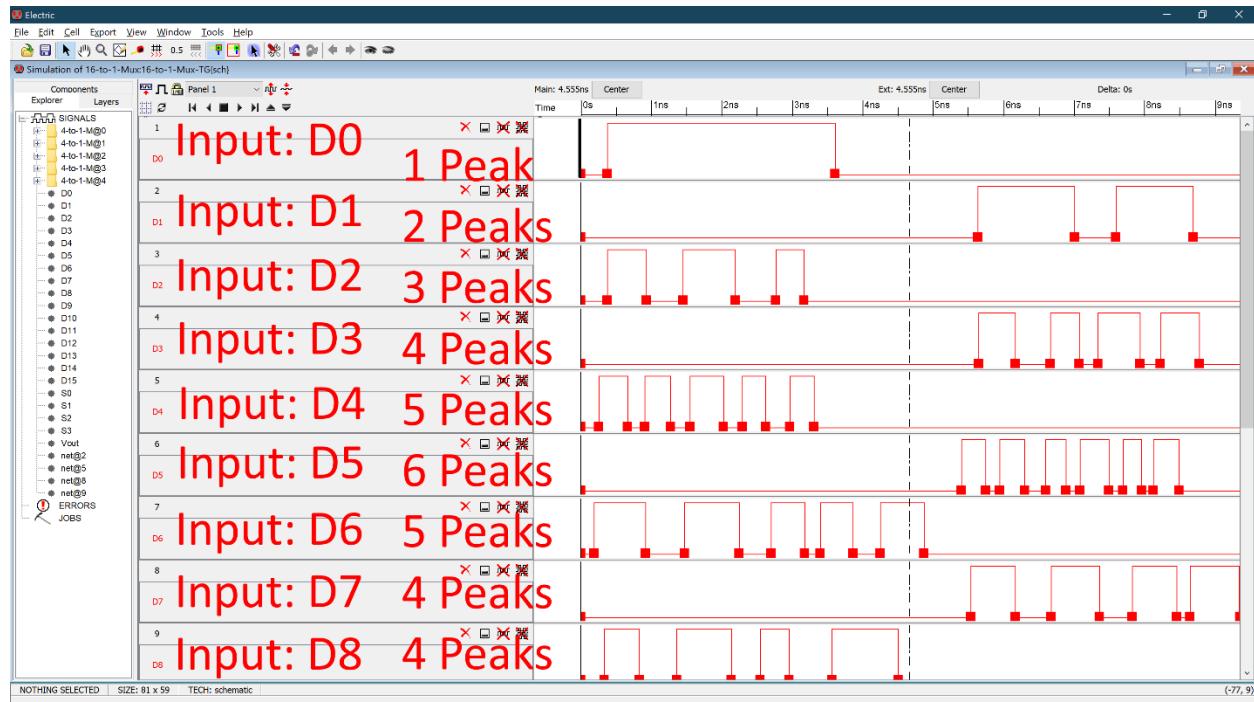


Figure 24.1: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer

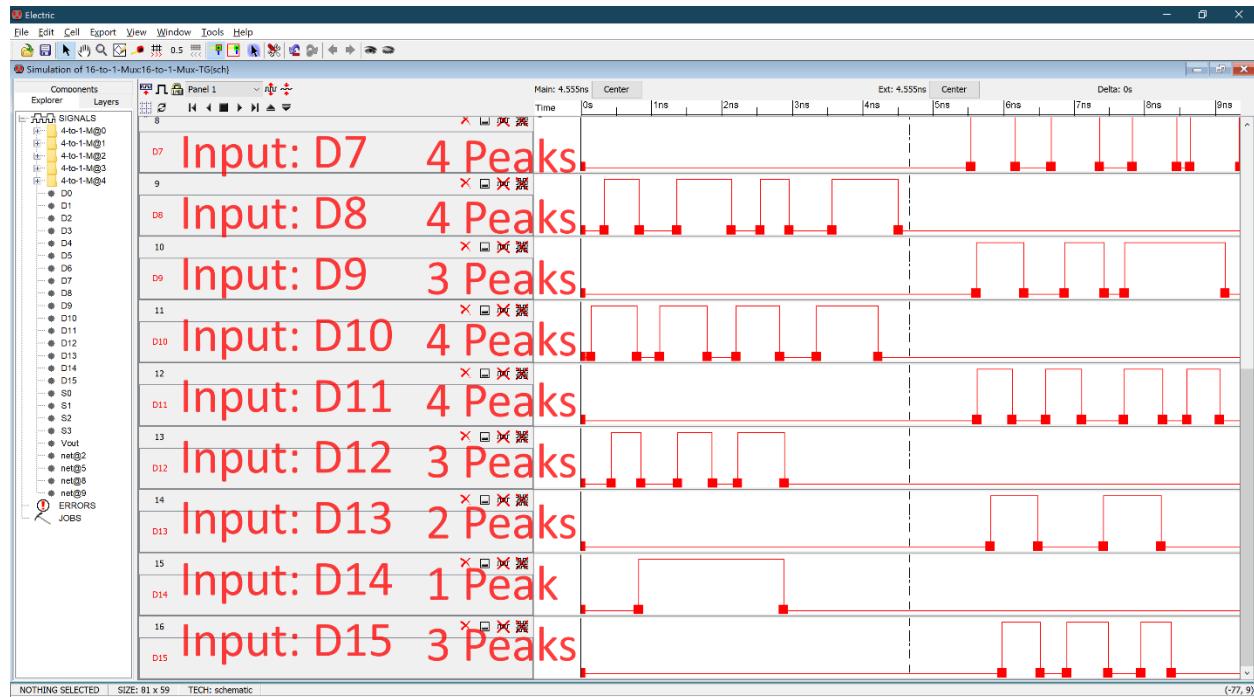


Figure 24.2: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer

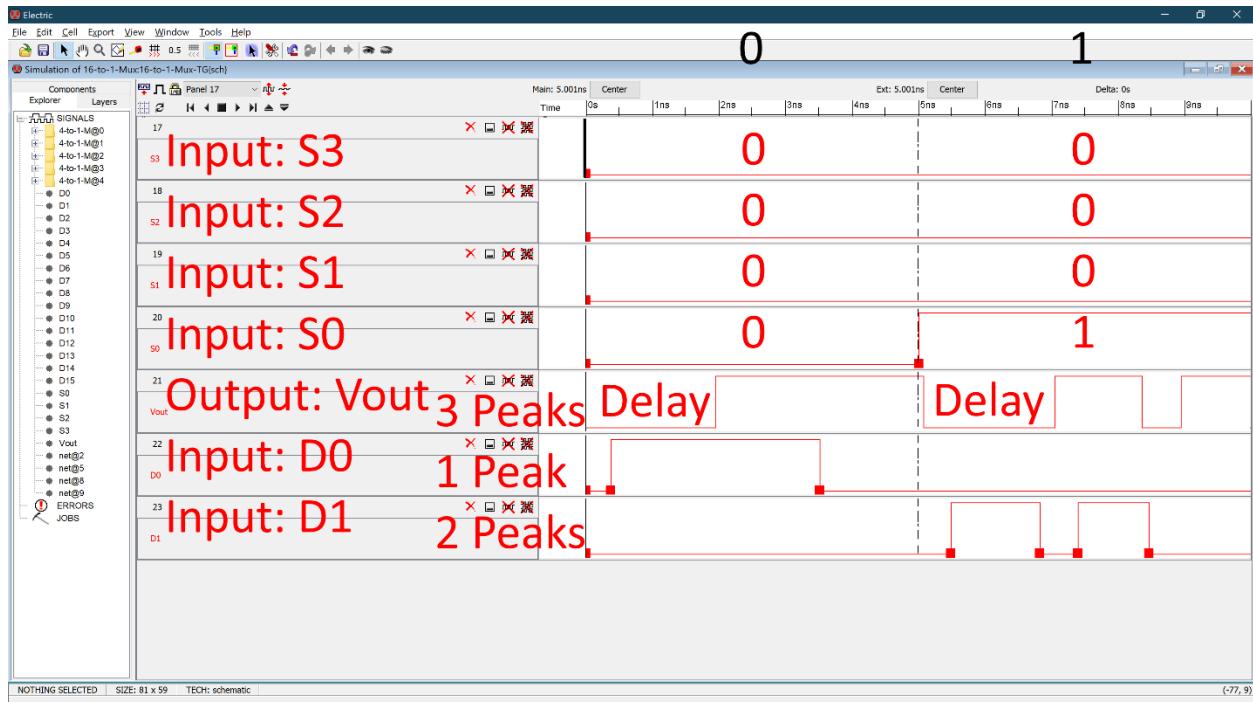


Figure 24.3: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 0 and 1)

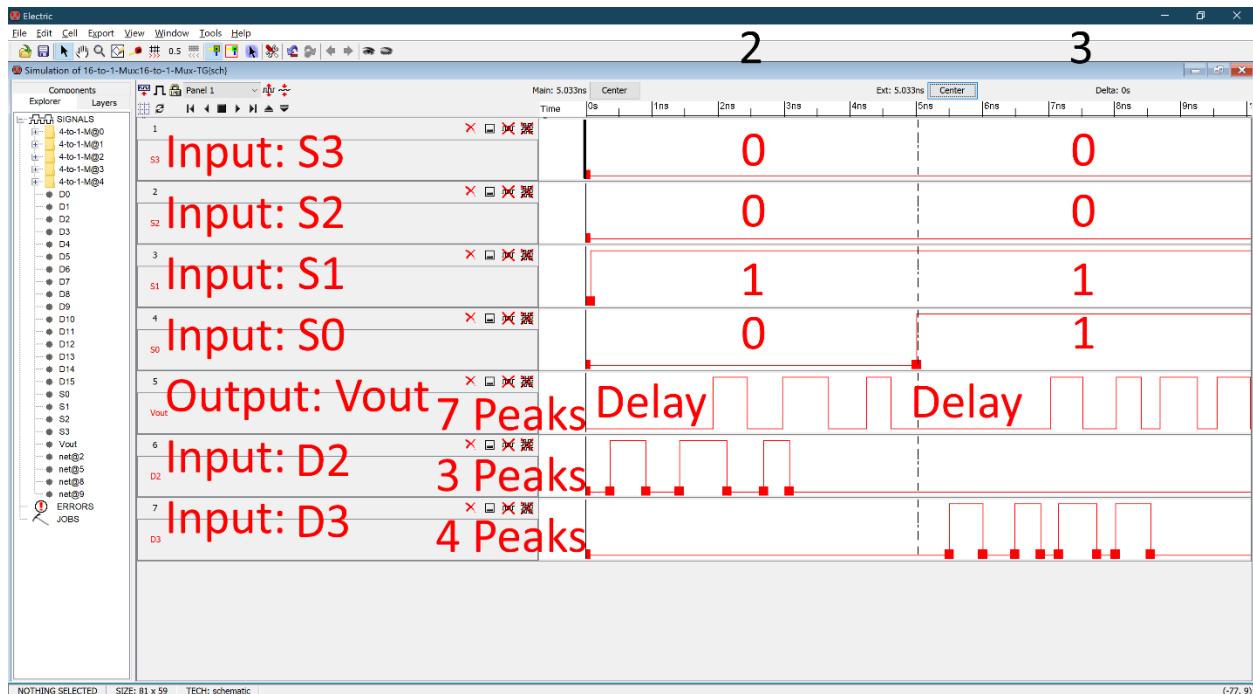


Figure 24.4: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 2 and 3)

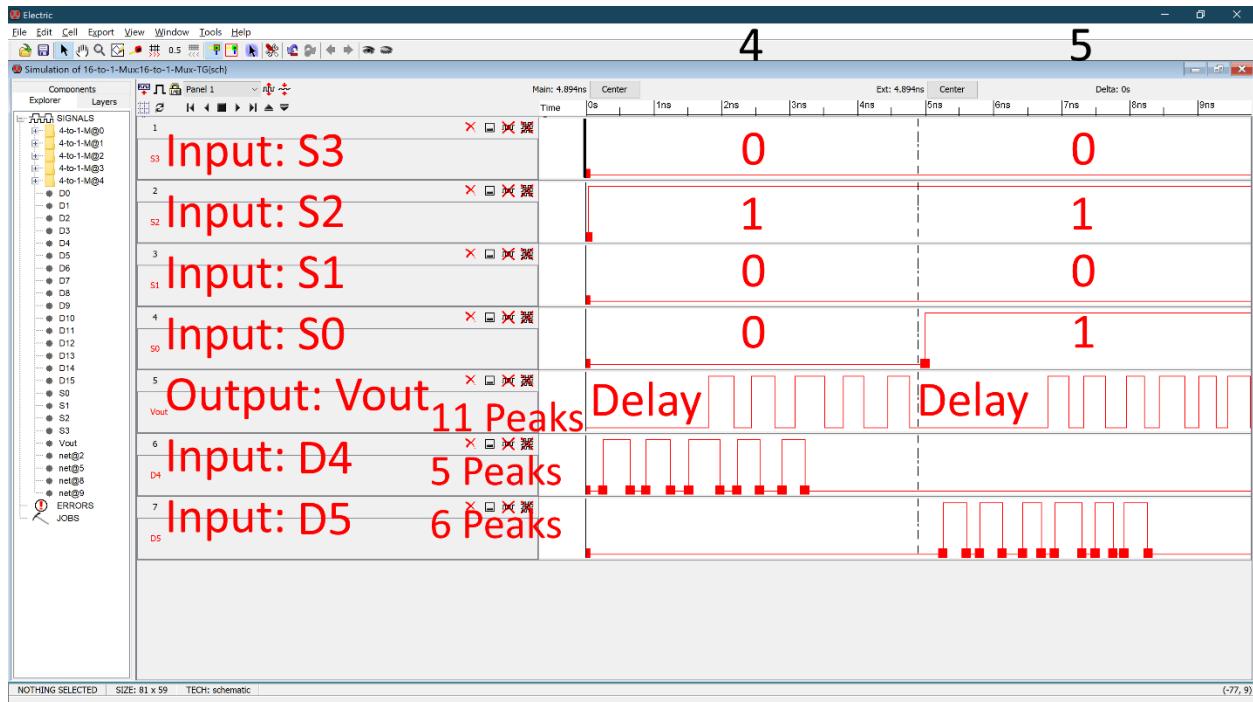


Figure 24.5: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 4 and 5)

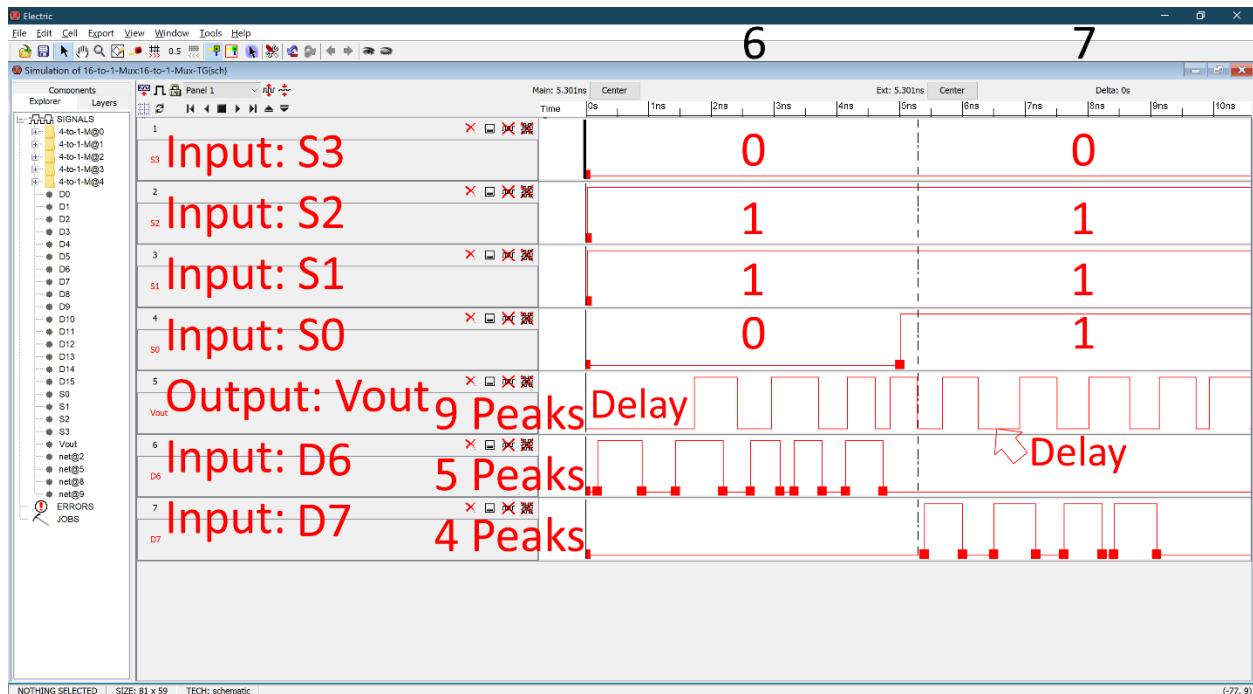


Figure 24.6: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 6 and 7)

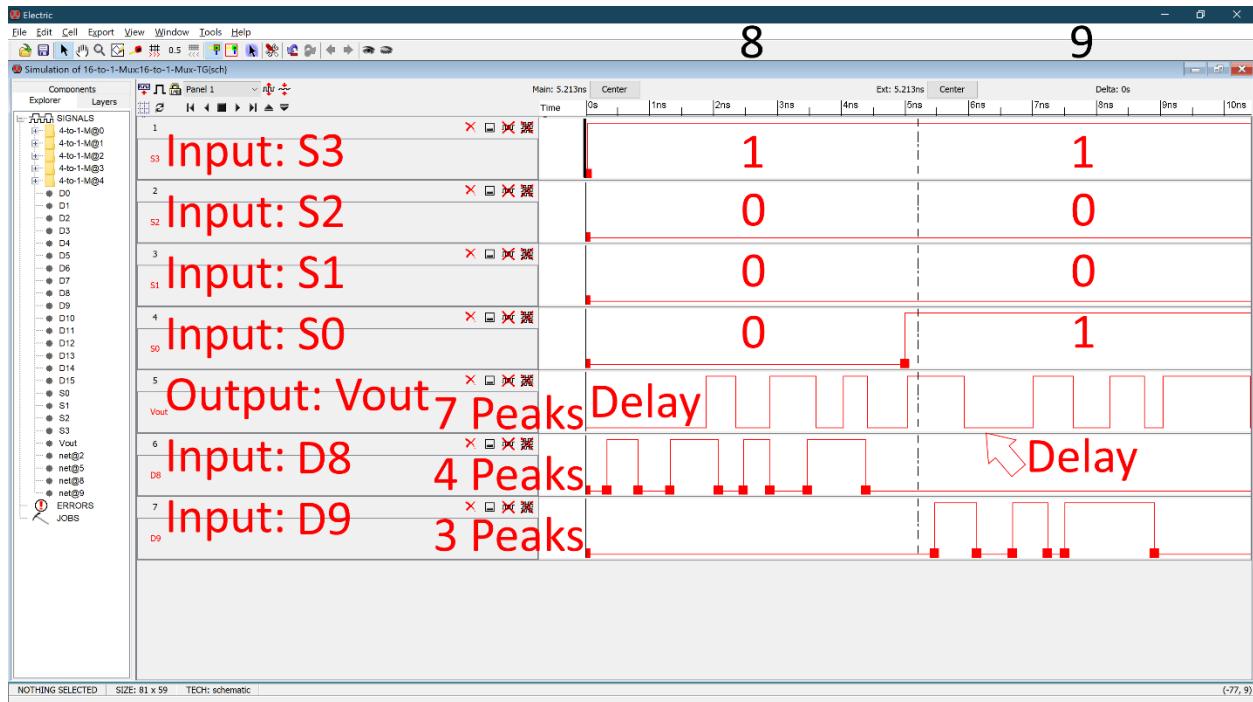


Figure 24.7: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 8 and 9)

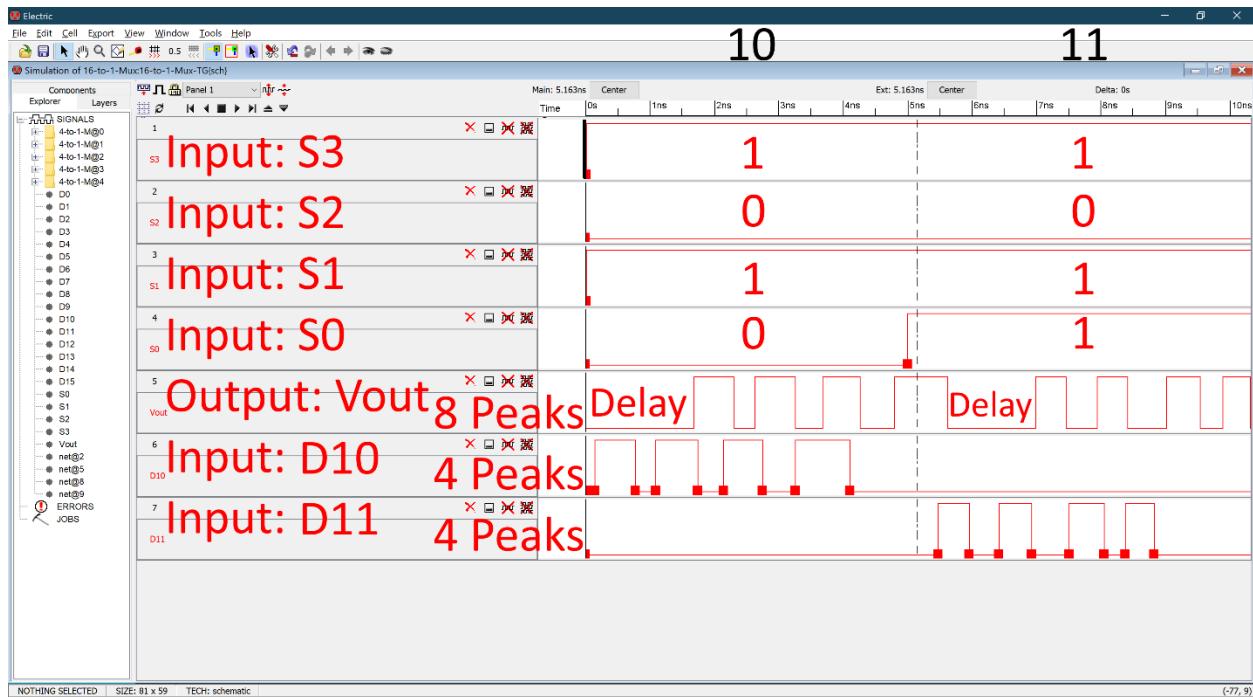


Figure 24.8: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 10 and 11)

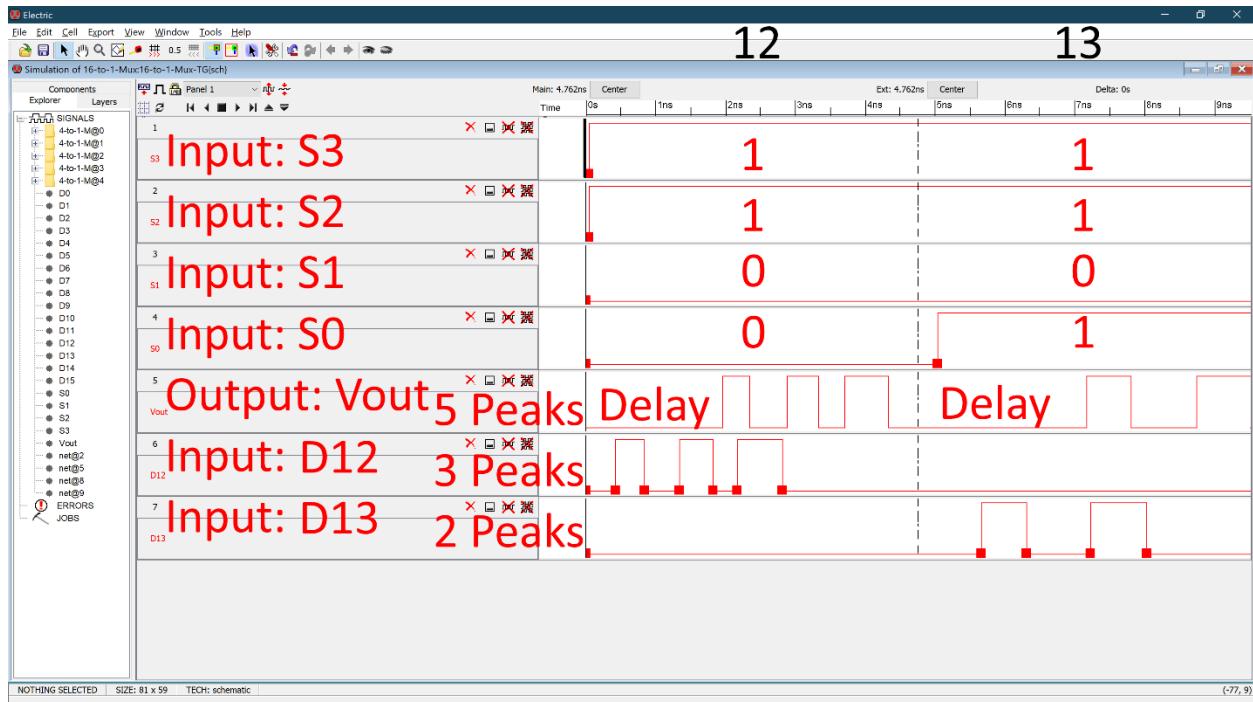


Figure 24.9: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 12 and 13)

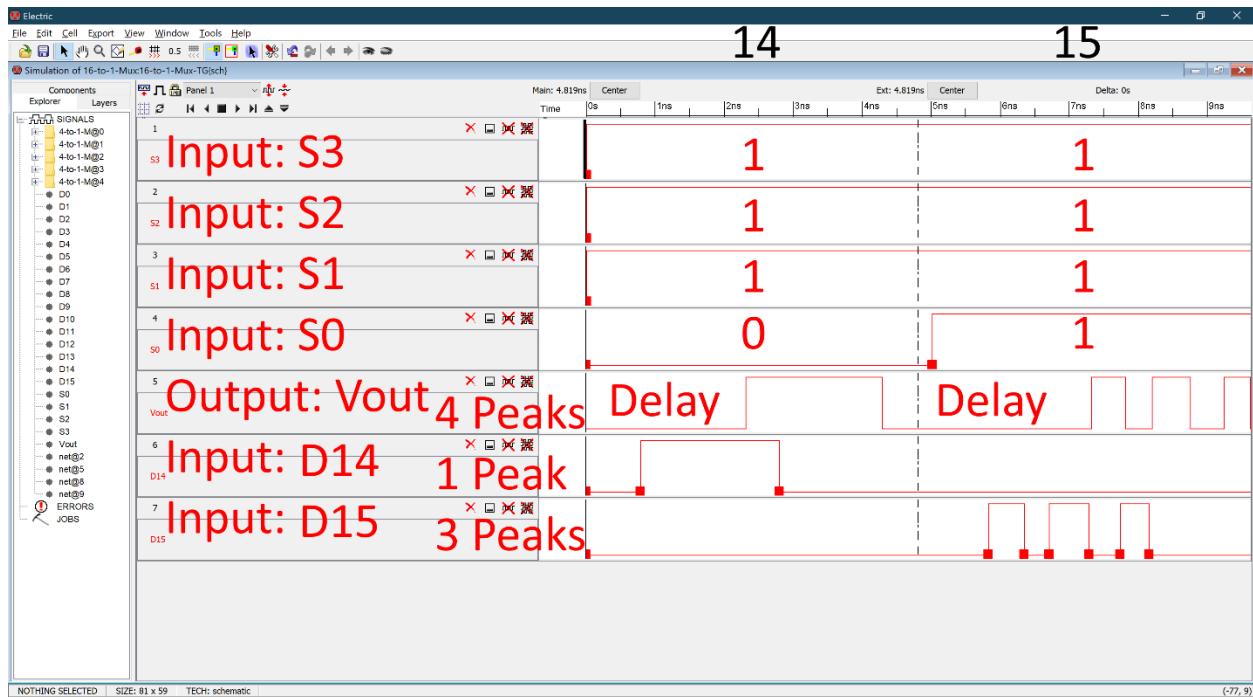


Figure 24.10: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 14 and 15)

Section 5.2: Layout:

For the layout, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the selectors and counting the peaks for the one that's selected and comparing it with the output.

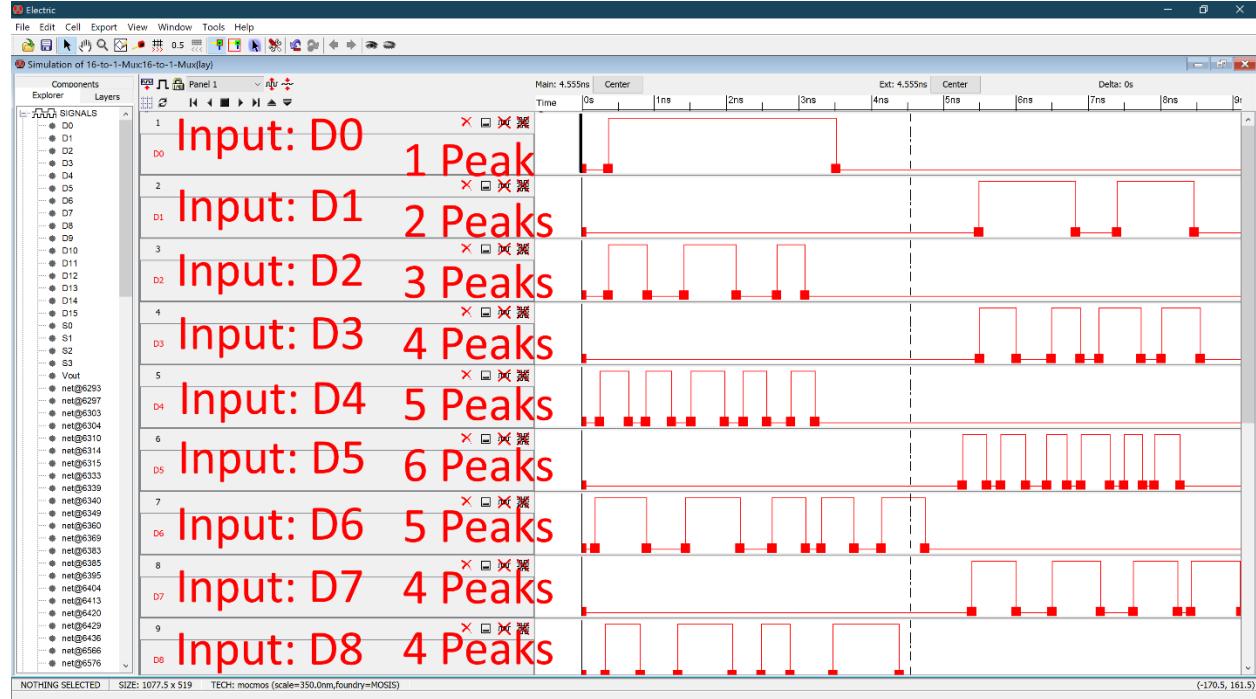


Figure 25.1: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer

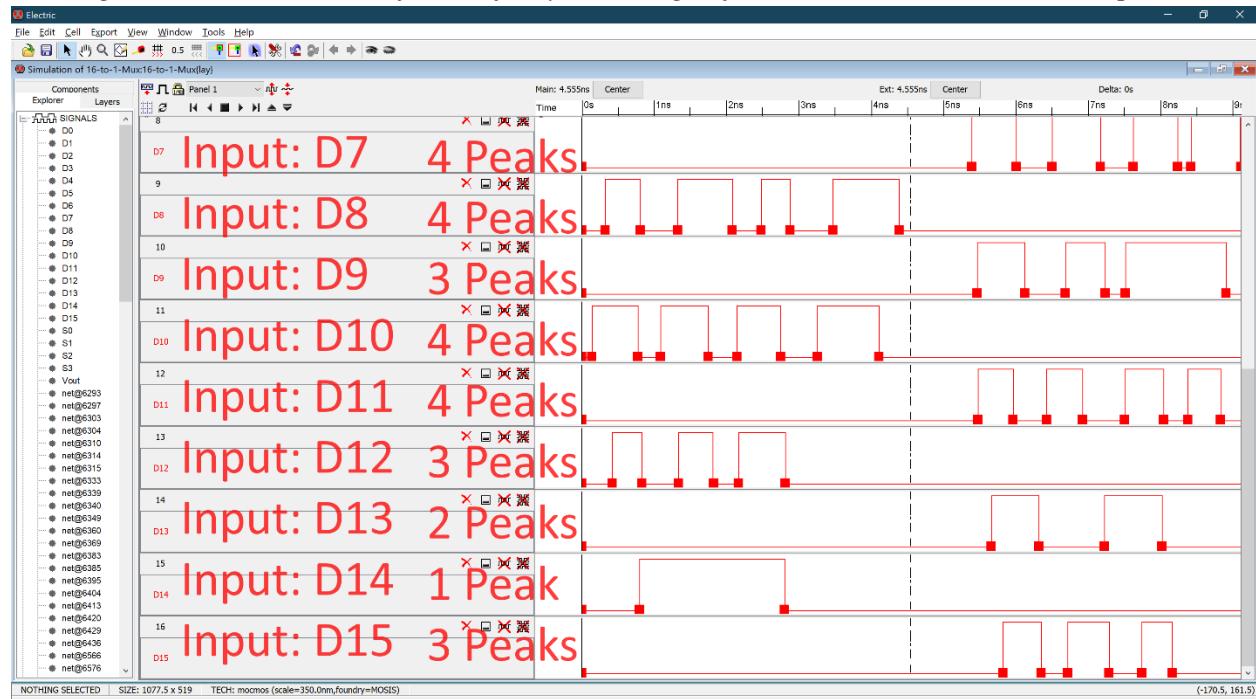


Figure 25.2: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer

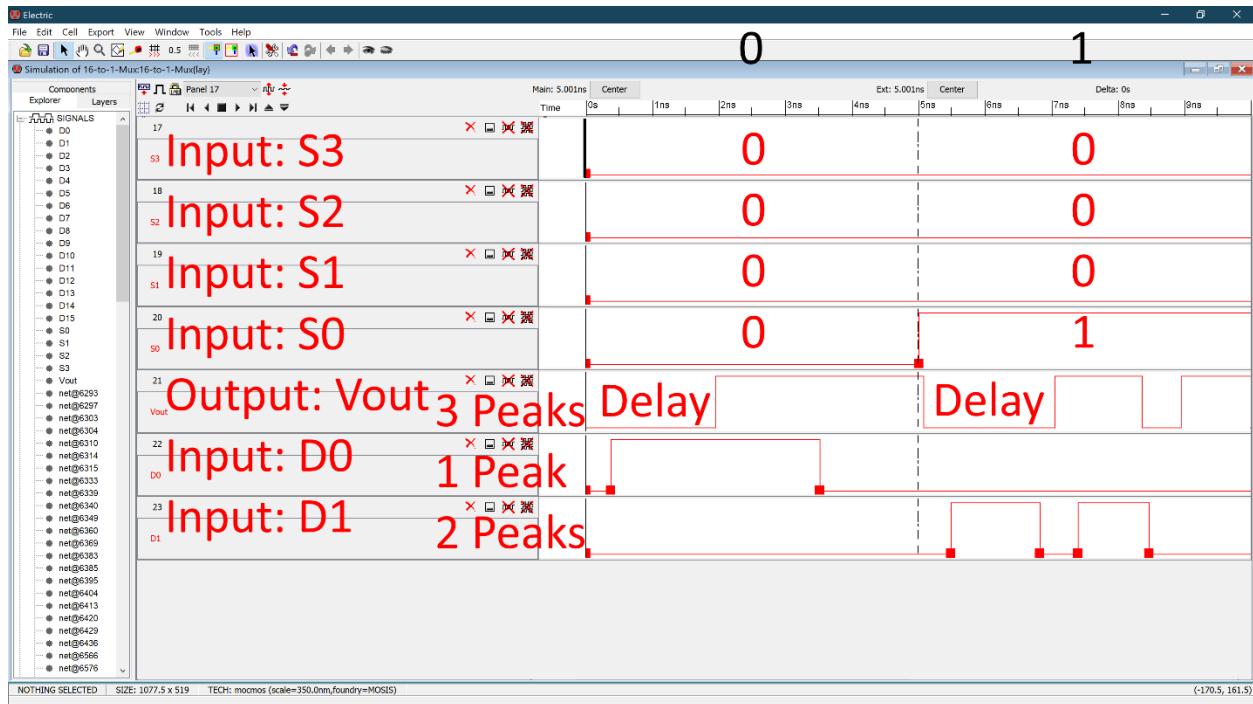


Figure 25.3: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer
(Selector at 0 and 1)

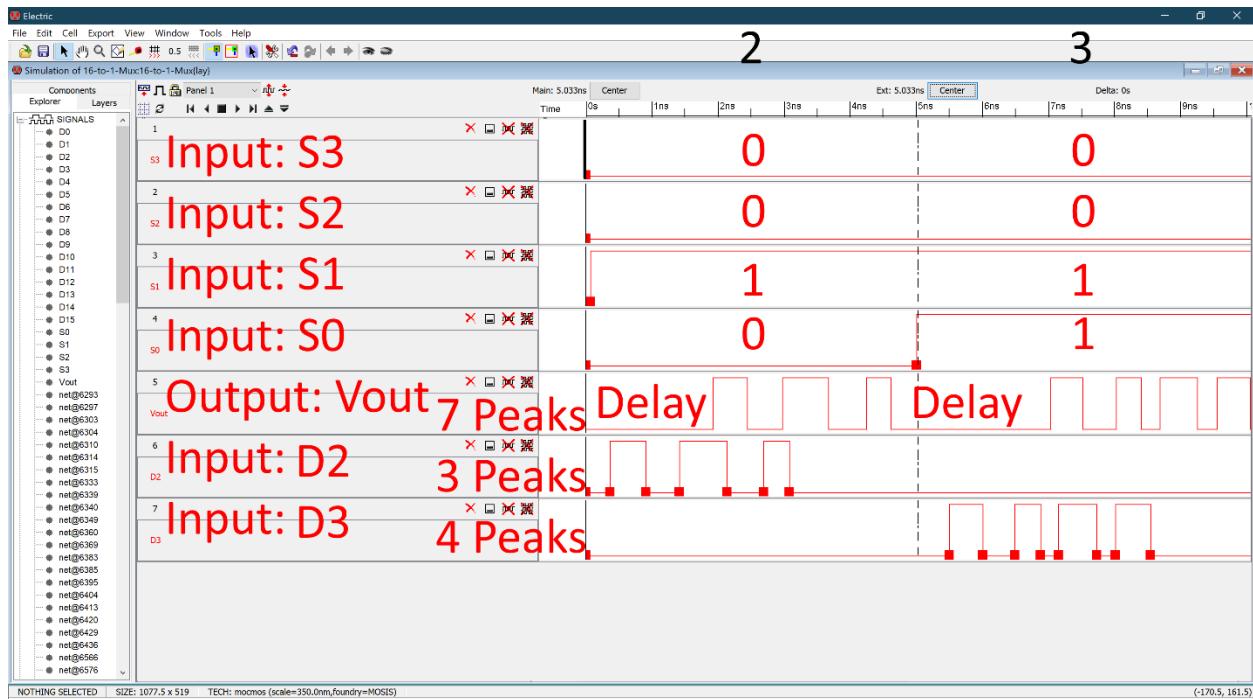


Figure 25.4: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer
(Selector at 2 and 3)

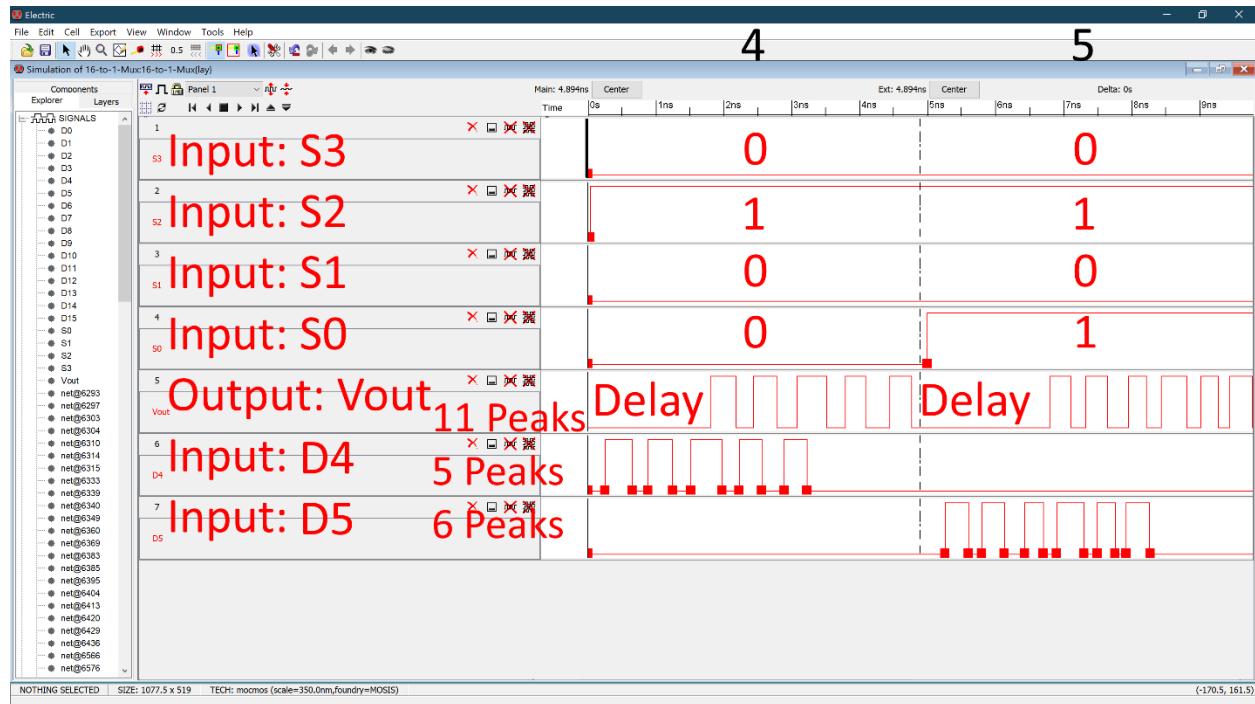


Figure 25.5: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer
(Selector at 4 and 5)

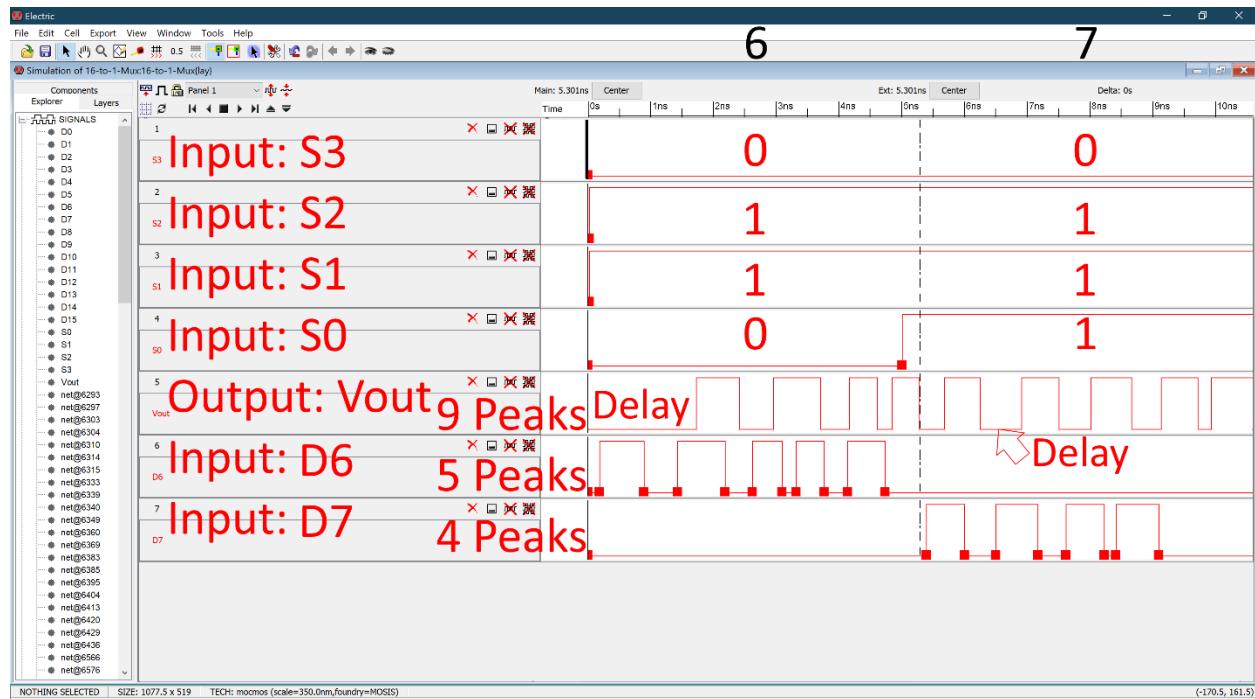


Figure 25.6: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer
(Selector at 6 and 7)

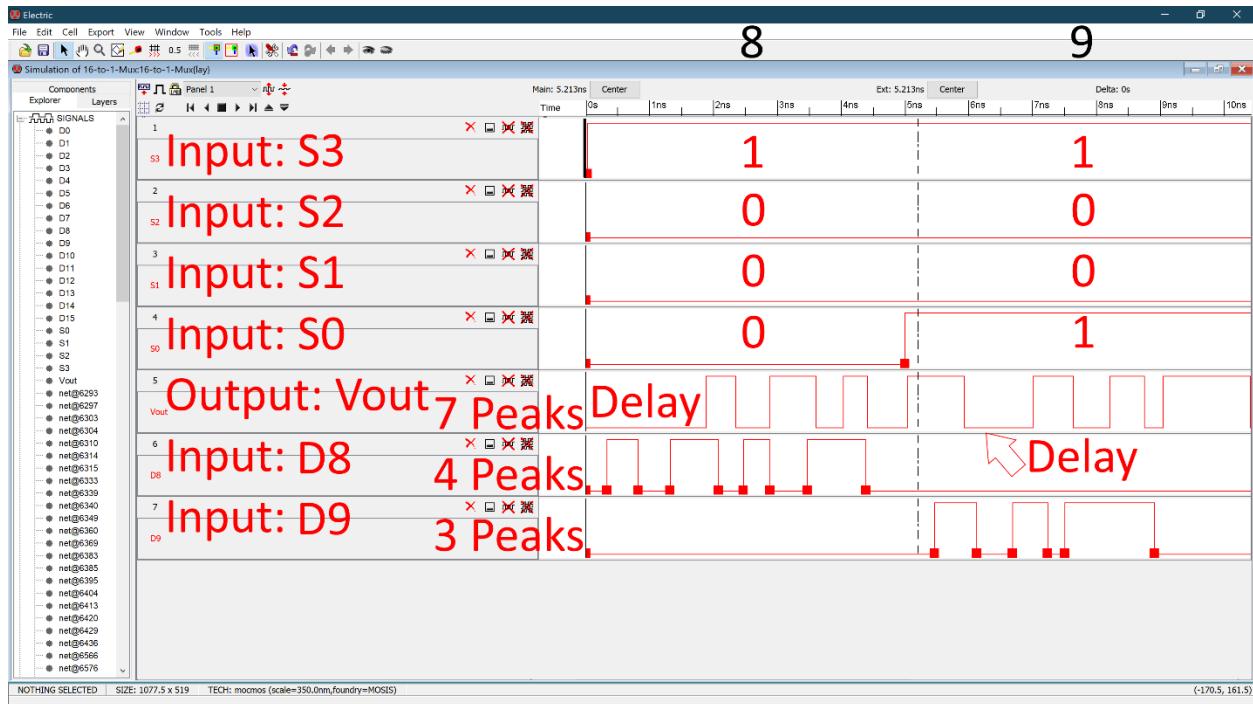


Figure 25.7: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer
(Selector at 8 and 9)

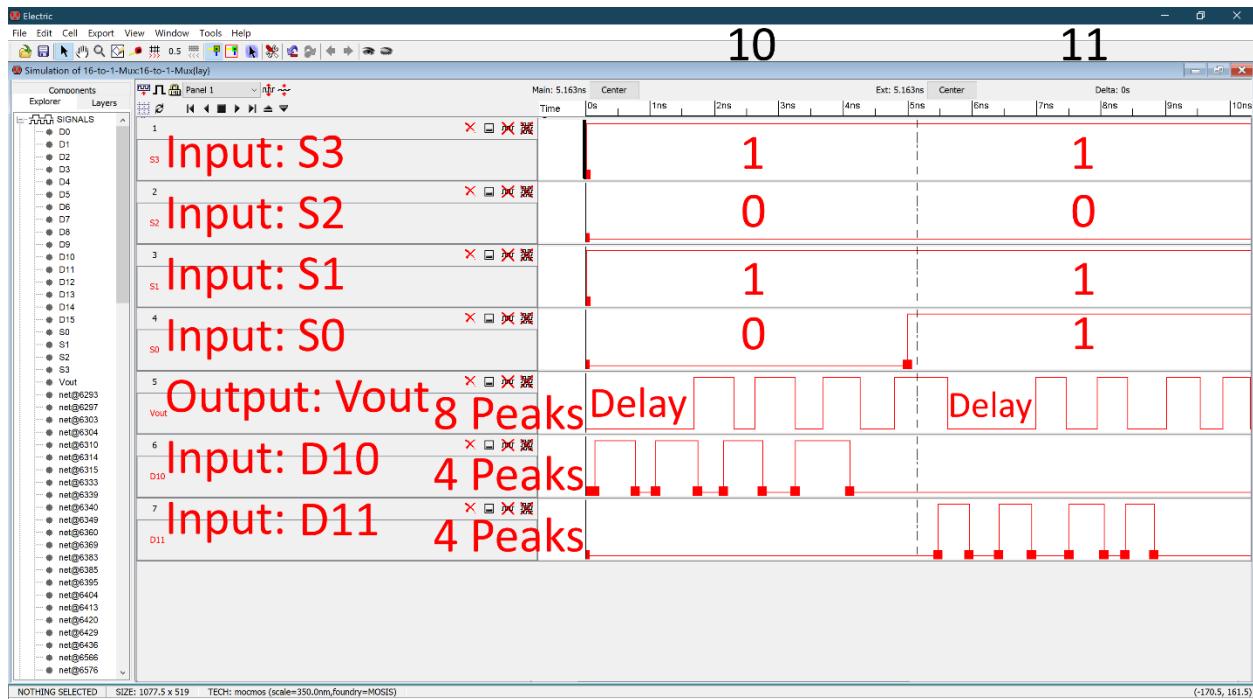


Figure 25.8: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer
(Selector at 10 and 11)

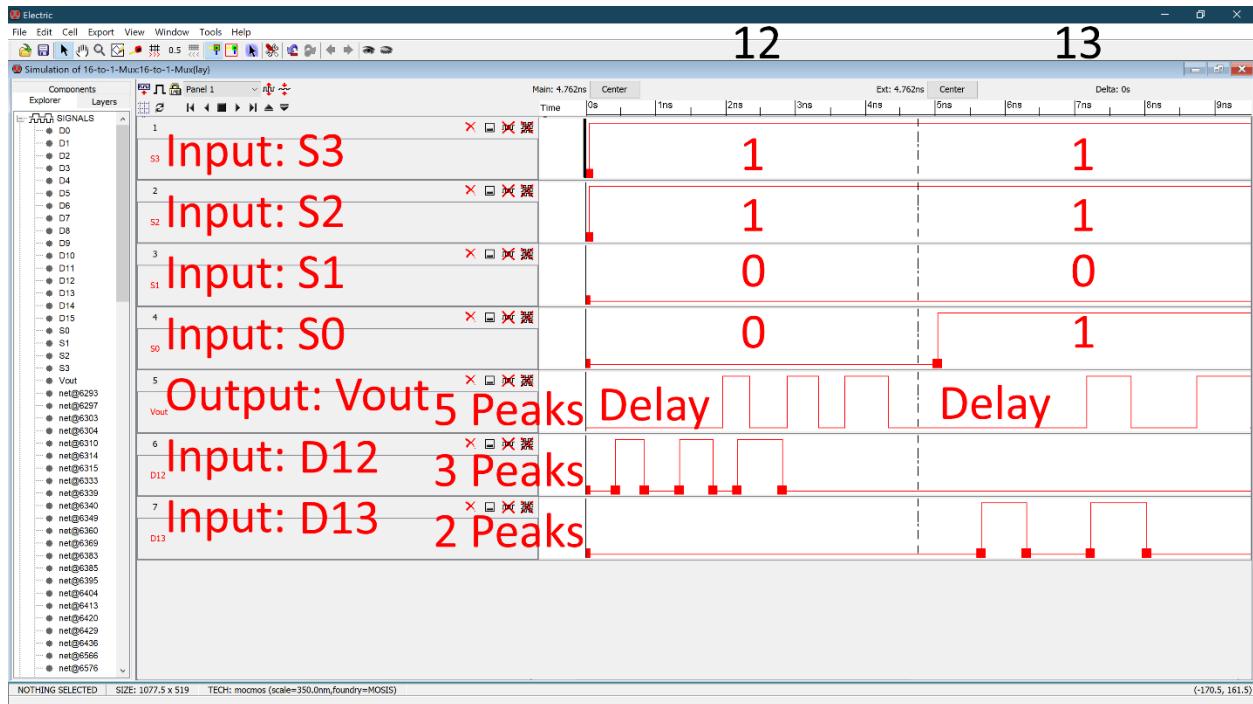


Figure 25.9: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer
(Selector at 12 and 13)

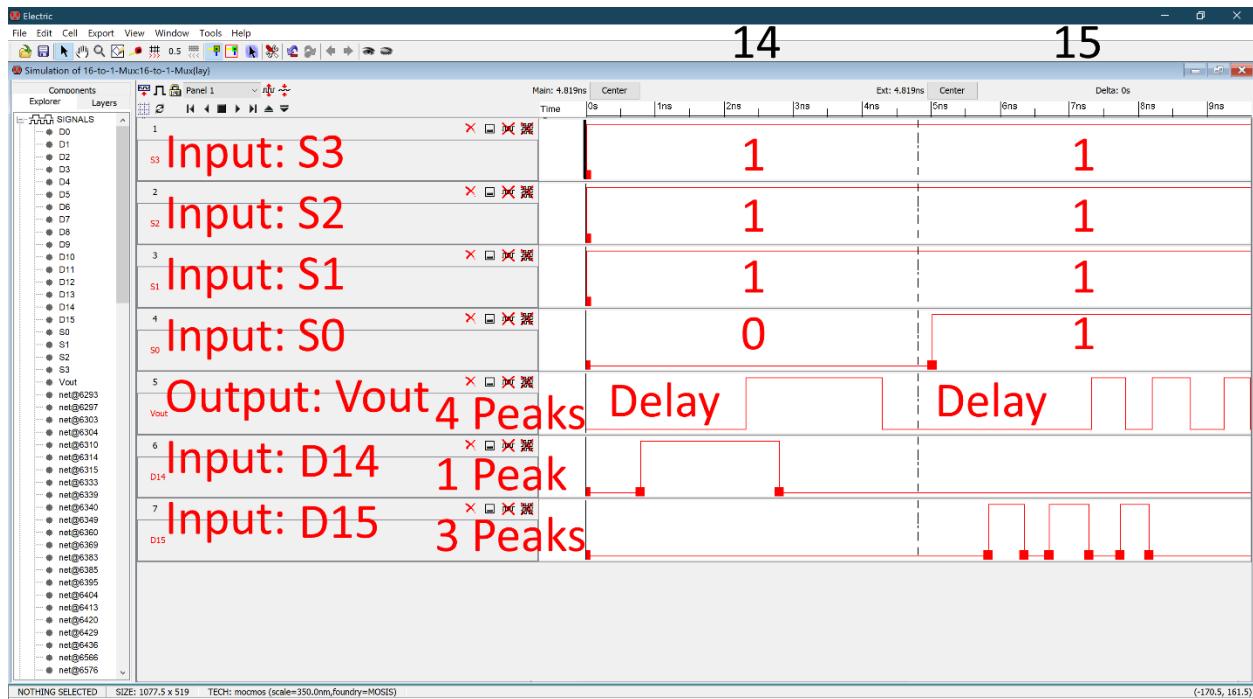


Figure 25.10: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer
(Selector at 14 and 15)

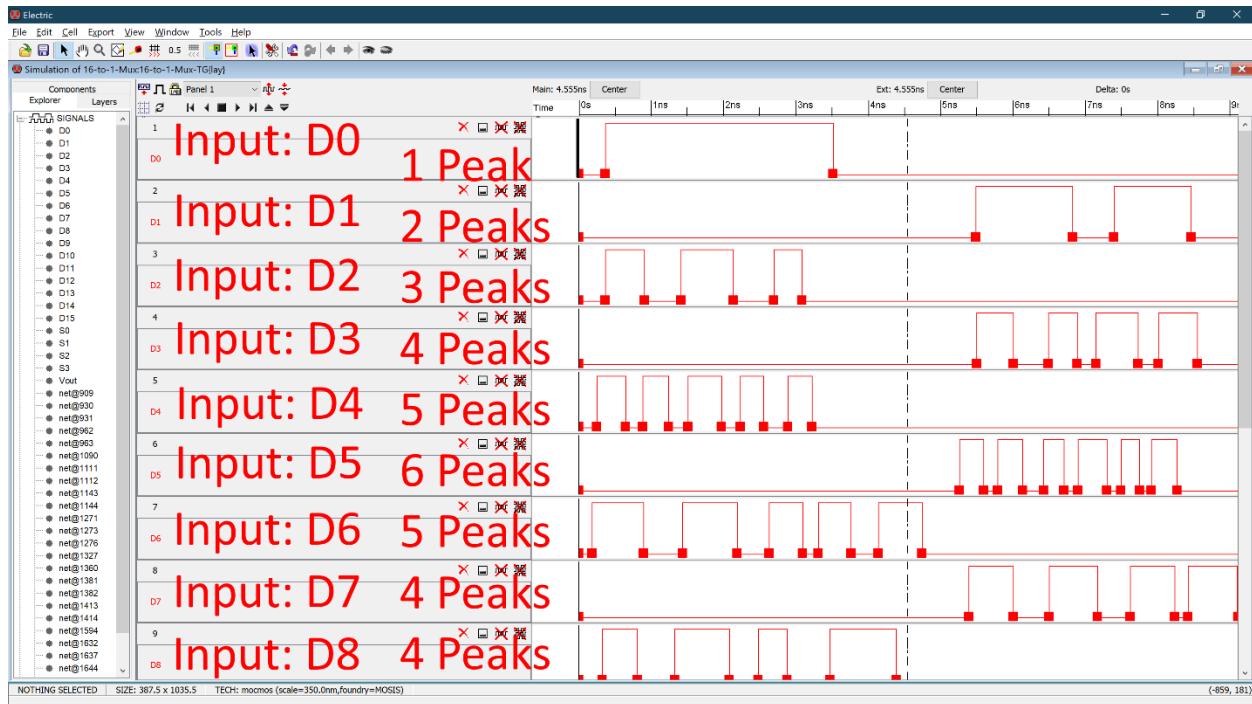


Figure 26.1: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer

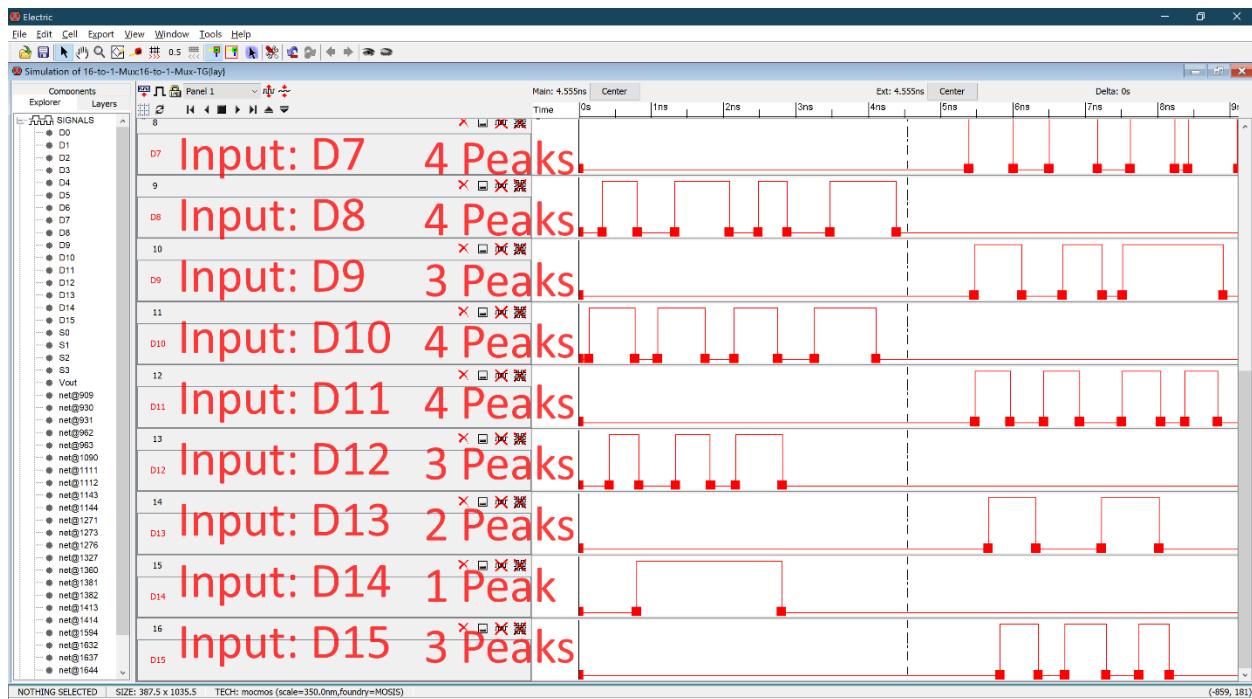


Figure 26.2: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer

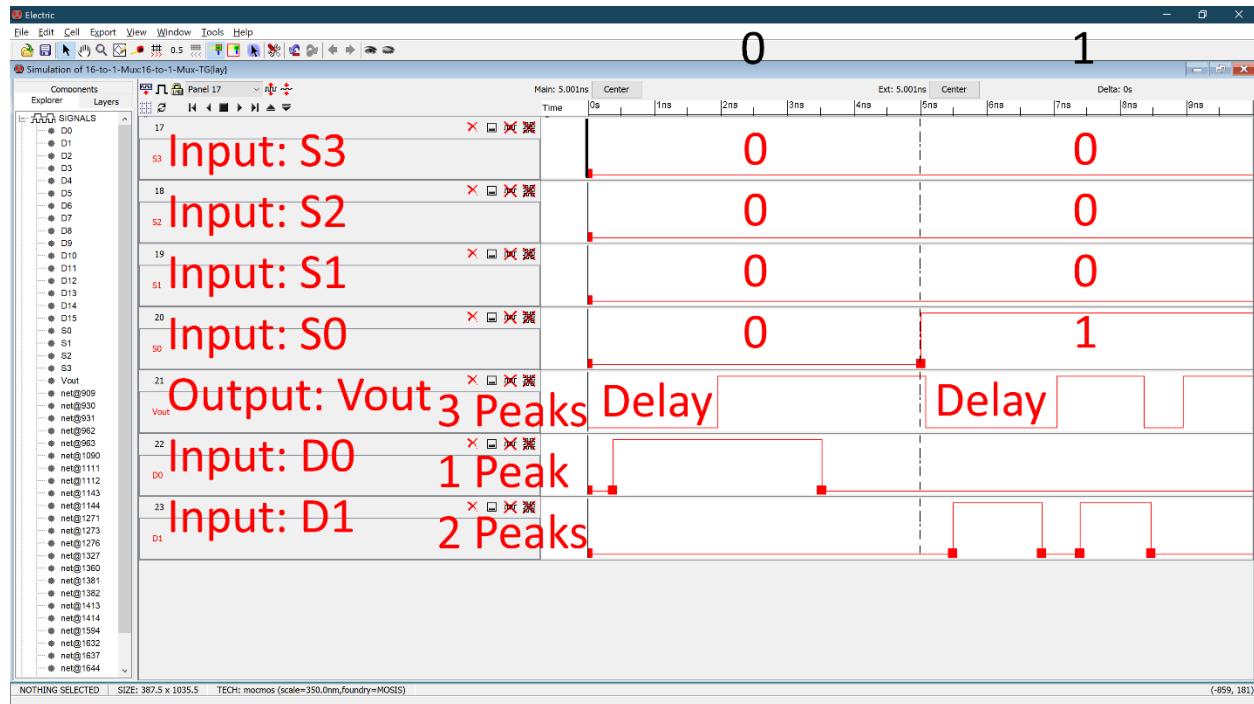


Figure 26.3: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 0 and 1)

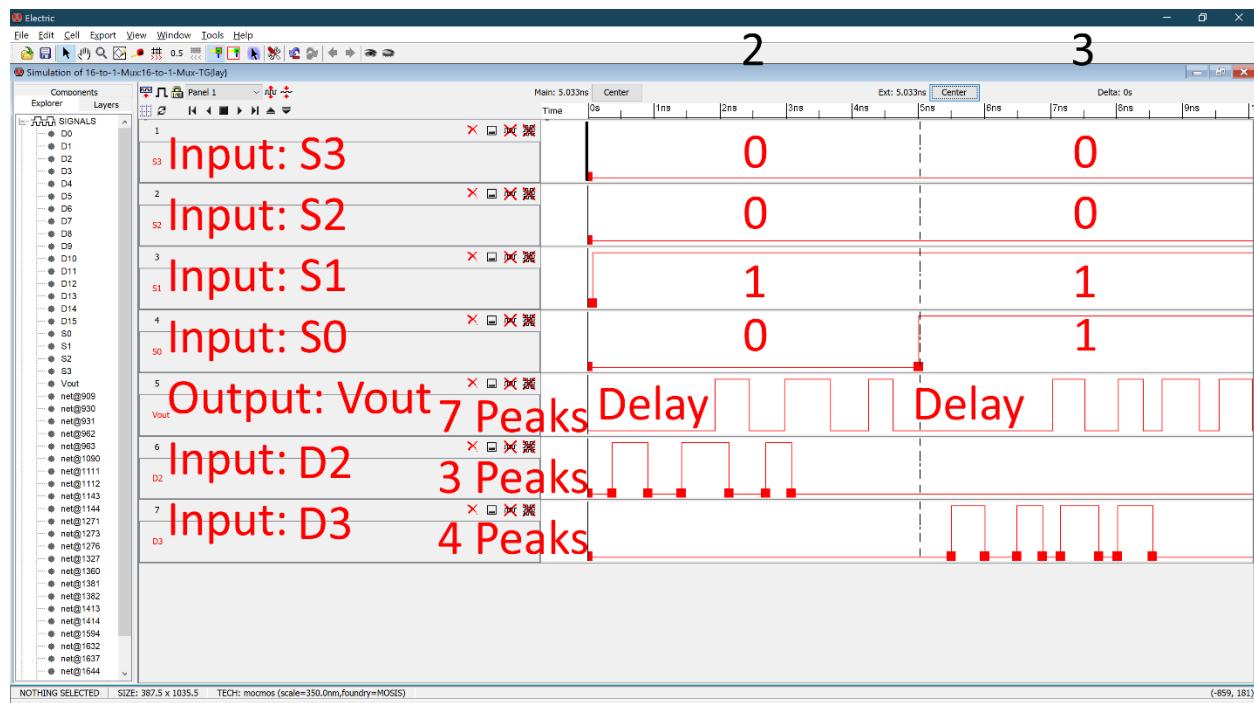


Figure 26.4: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 2 and 3)

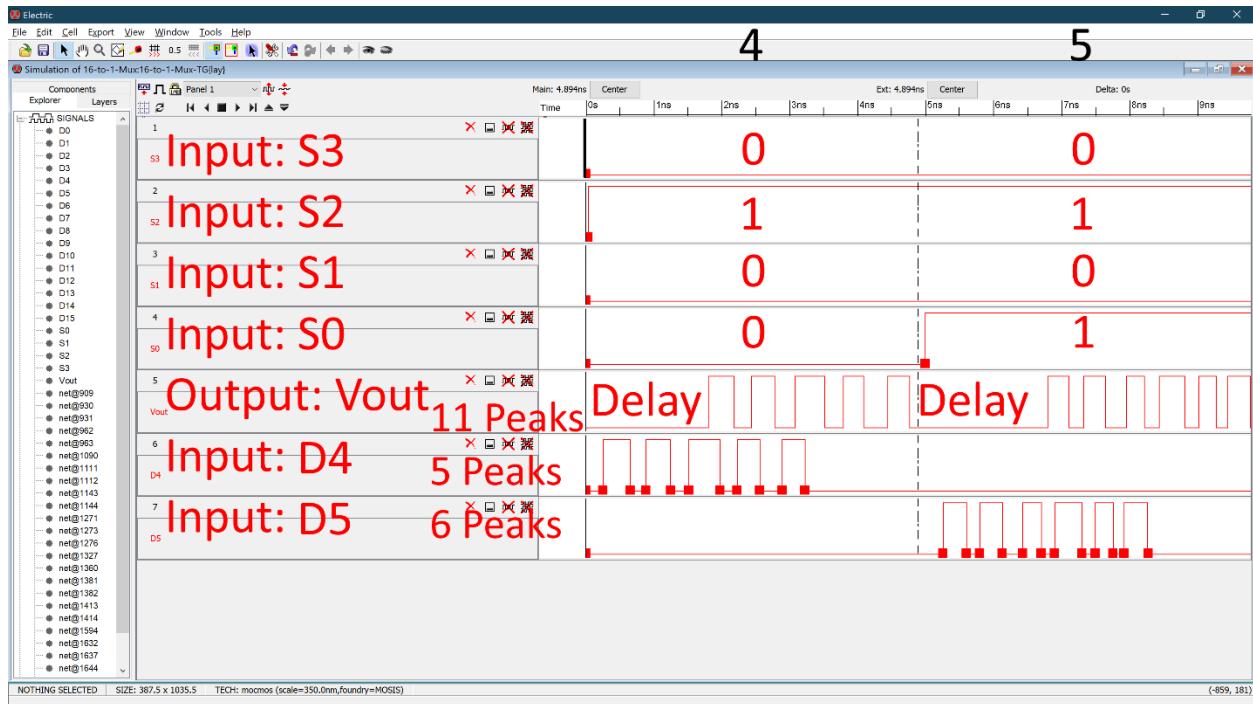


Figure 26.5: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 4 and 5)

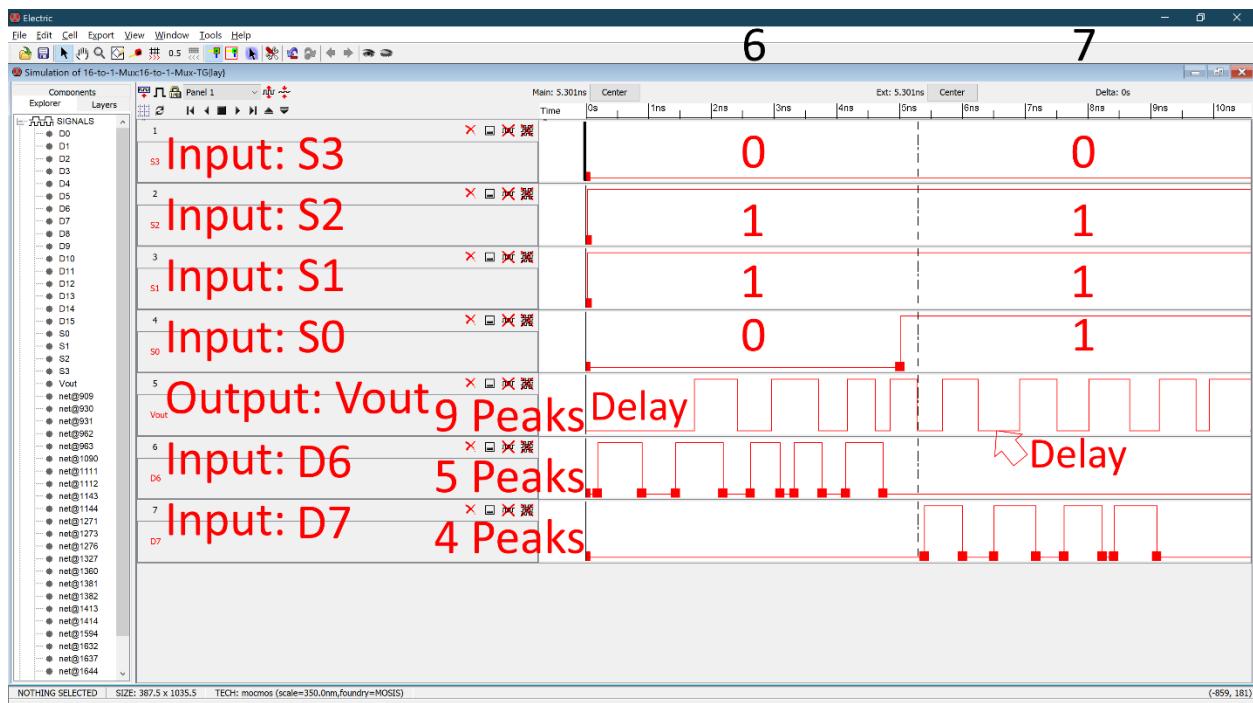


Figure 26.6: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 6 and 7)

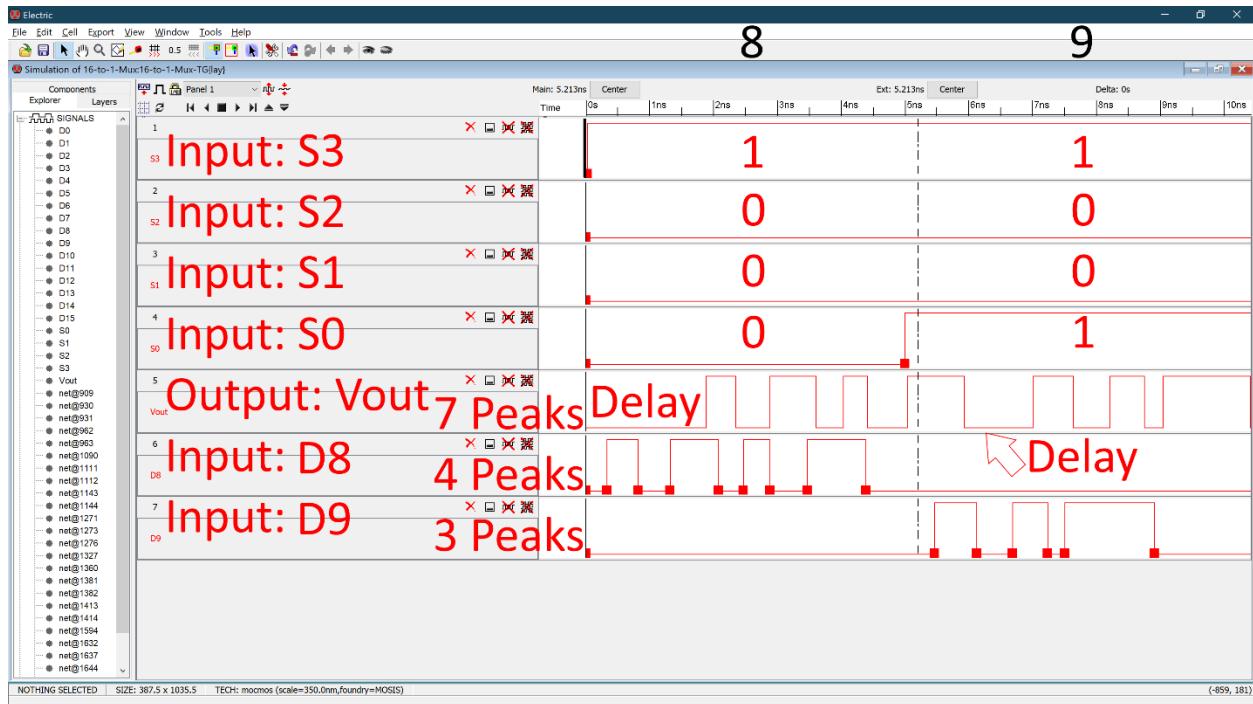


Figure 26.7: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer
(Selector at 8 and 9)

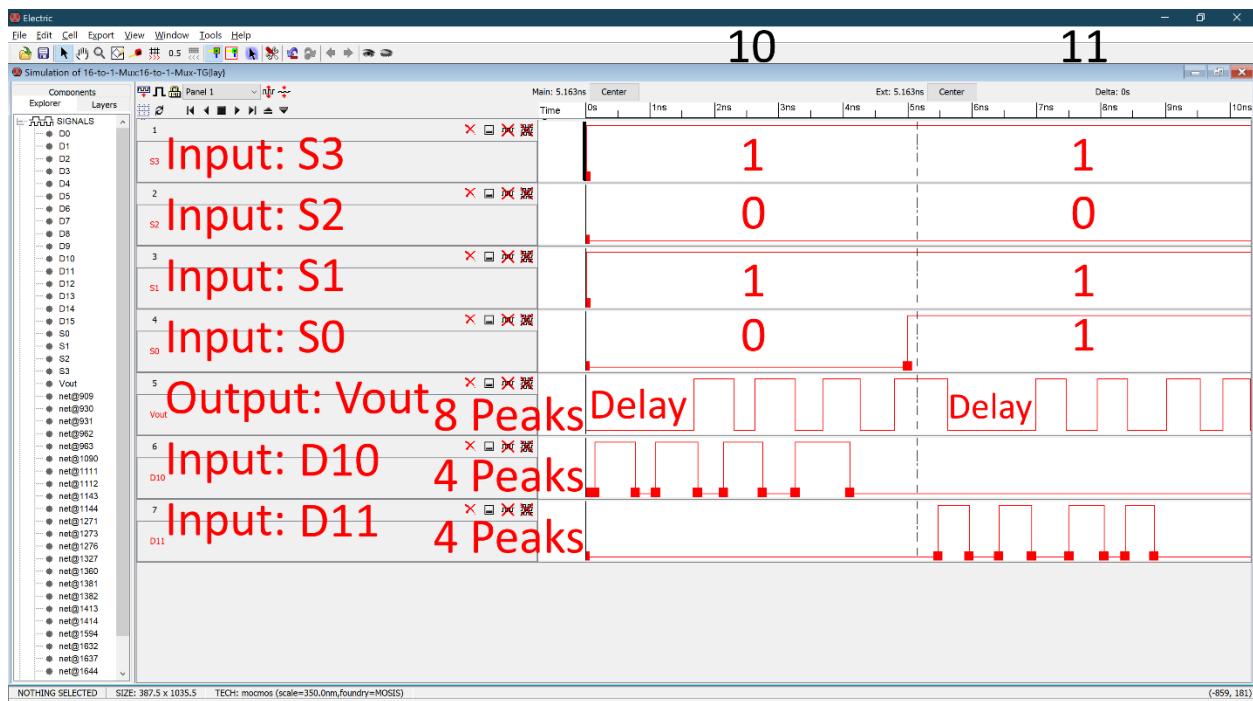


Figure 26.8: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer
(Selector at 10 and 11)

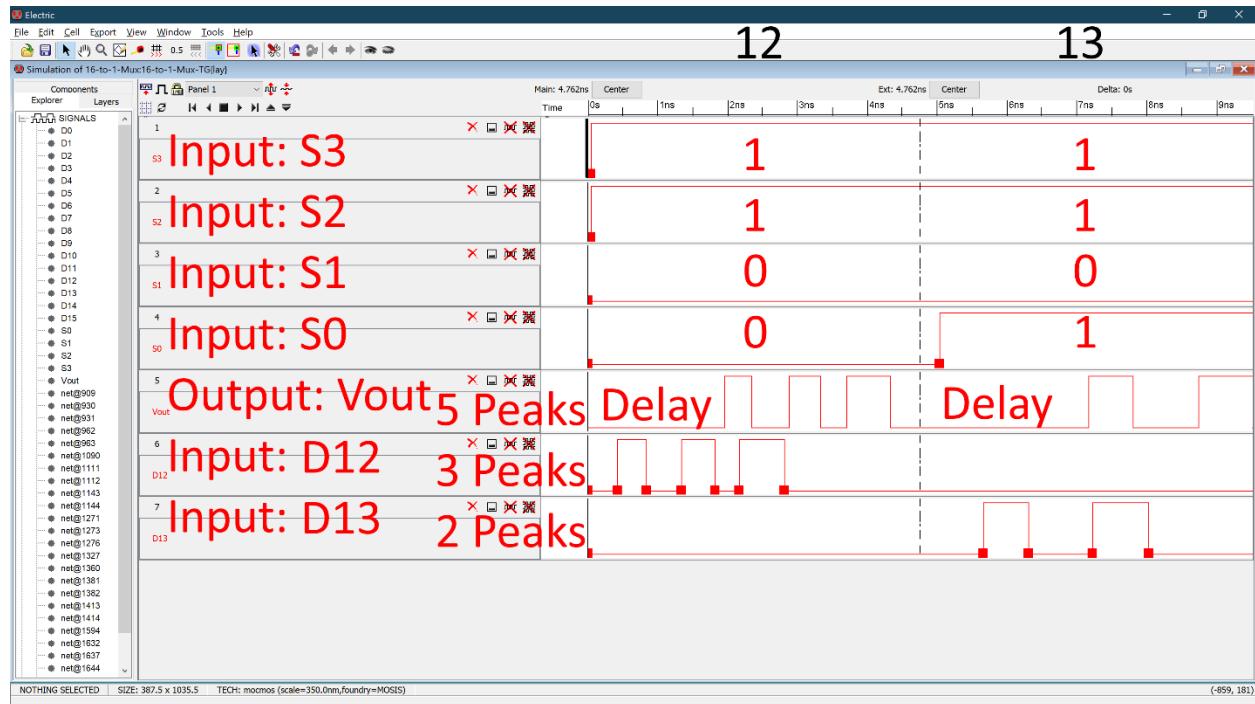


Figure 26.9: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 12 and 13)

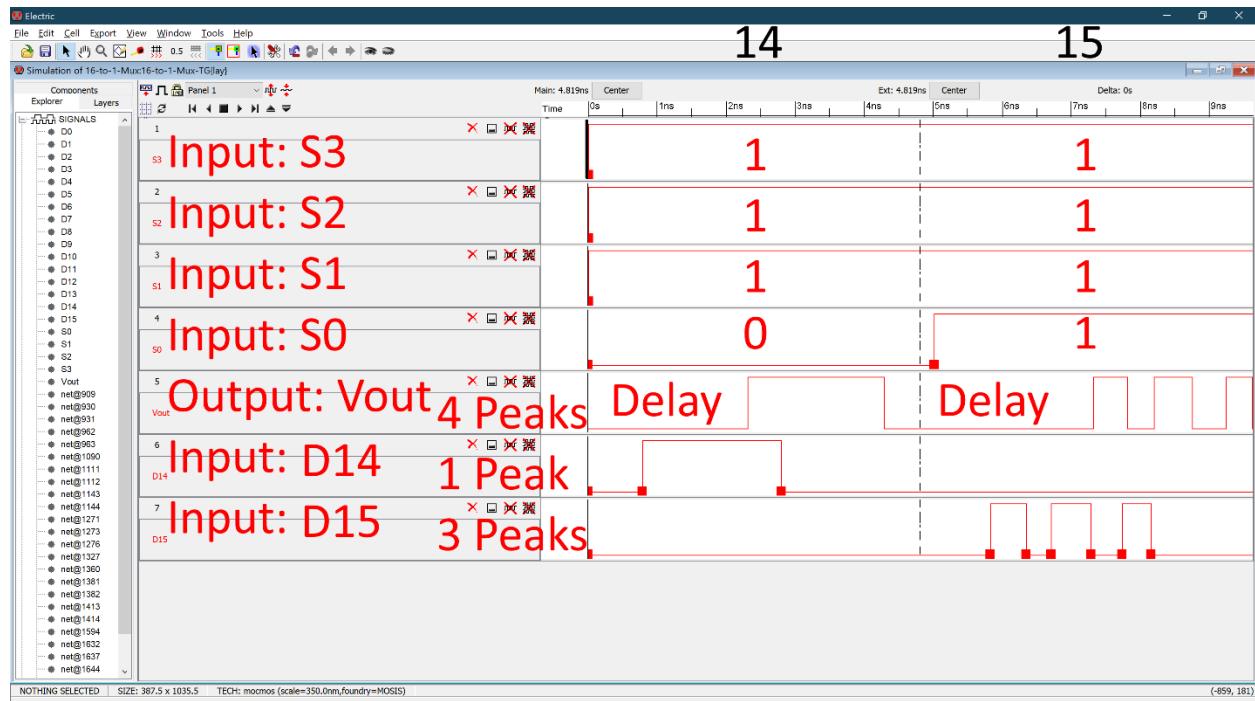


Figure 26.10: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 14 and 15)

Section 5.3: Comparison:

For IRSIM, by comparing Figure 23 (Conventional Schematic), Figure 24 (Transmission Gate Schematic), Figure 25 (Conventional Layout), and Figure 26 (Transmission Gate Layout) with each other, the way the output reacted given the certain inputs appears to be the same. In addition, with the inputs we gave, it gave us the appropriate outputs that we were looking for, so it confirms that our design is correct. The outputs that we were looking from could be seen by using the truth table on Table 1. The only noticeable difference between the figures would be the propagation delay, which could be seen on Table 6. Depending on the which design, each has its own different propagation delay.

In conclusion, IRSIM shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures were the rise time, fall time, and propagation delay. The differences can be viewed on Table 6, which has a summary of the measurements.

Section 6: LTSPICE Code and Parasitic Extractions:

The Spice Code that we wrote is shown on Figure 27. It provides certain values to the inputs so that it'll be able to produce a certain output. The computations that we tested set each input (D0-D15) high for 50 nanoseconds at different times, then back to low; in other words, 100 nanoseconds period, with rise time and fall time of 5 nanoseconds and 50% duty cycle. Each of the inputs were high at different times so they wouldn't be able to relate to each other. After that, we set tested all the computations for the selector (S0-S3), starting from 0 to 15. This way, it'll be able to output each individual input and show a wavelike output.

We ran LTSPICE on the conventional 16-to-1 Multiplexer Schematic, conventional 16-to-1 Multiplexer Layout, transmission gate 16-to-1 Multiplexer Schematic, and transmission gate 16-to-1 Multiplexer Layout and it generated a code underneath it. A sample of the Spice Deck and Parasitic Extractions that came from those designs are shown from Figure 28 to Figure 35.

```

VDD VDD 0 DC 3.3
VGND GND 0 DC 0
Vin2 D0 0 PULSE (0 3.3 0n 5n 5n 50n 1600n)
Vin3 D1 0 PULSE (0 3.3 100n 5n 5n 50n 1600n)
Vin4 D2 0 PULSE (0 3.3 200n 5n 5n 50n 1600n)
Vin5 D3 0 PULSE (0 3.3 300n 5n 5n 50n 1600n)
Vin6 D4 0 PULSE (0 3.3 400n 5n 5n 50n 1600n)
Vin7 D5 0 PULSE (0 3.3 500n 5n 5n 50n 1600n)
Vin8 D6 0 PULSE (0 3.3 600n 5n 5n 50n 1600n)
Vin9 D7 0 PULSE (0 3.3 700n 5n 5n 50n 1600n)
Vin10 D8 0 PULSE (0 3.3 800n 5n 5n 50n 1600n)
Vin11 D9 0 PULSE (0 3.3 900n 5n 5n 50n 1600n)
Vin12 D10 0 PULSE (0 3.3 1000n 5n 5n 50n 1600n)
Vin13 D11 0 PULSE (0 3.3 1100n 5n 5n 50n 1600n)
Vin14 D12 0 PULSE (0 3.3 1200n 5n 5n 50n 1600n)
Vin15 D13 0 PULSE (0 3.3 1300n 5n 5n 50n 1600n)
Vin16 D14 0 PULSE (0 3.3 1400n 5n 5n 50n 1600n)
Vin17 D15 0 PULSE (0 3.3 1500n 5n 5n 50n 1600n)
Vin18 S0 0 PULSE (0 3.3 100n 5n 5n 100n 200n)
Vin19 S1 0 PULSE (0 3.3 200n 5n 5n 200n 400n)
Vin20 S2 0 PULSE (0 3.3 400n 5n 5n 400n 800n)
Vin21 S3 0 PULSE (0 3.3 800n 5n 5n 800n 1600n)
TRAN 0 1600n
include C:\Users\kille\Desktop\Electric\C5_models.txt

```

Figure 27: Spice Code Written For LTSPICE

```
(Itpice XVI - [16-to-1-Mux.sp])  
File Edit View Simulator Tools Window Help  
16-to-1-Mux.sp 16-to-1Aux.sp  
*** SPICE deck for cell 16-to-1-Mux(sch) from library 16-to-1-Mux  
*** Created on Tue Oct 29, 2019 15:40:18  
*** Last revised on Sat Nov 09, 2019 10:46:45  
*** Written on Sun Nov 10, 2019 14:19:50 by Electric VLSI Design System, version 9.07  
*** Layout tech: mcmcos, foundry MOSIS  
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF  
  
*** SUBCIRCUIT 16-to-1-Mux AND FROM CELL AND(sch)  
.SUBCKT 16-to-1-Mux AND A B Vout  
** GLOBAL gnd  
** GLOBAL vdd  
Mmosm01 net#12 A net#10 gnd NMOS L=0.35U W=0.875U  
Mmosm02 net#10 B gnd gnd NMOS L=0.35U W=0.075U  
Mmosm03 Vout net#12 gnd gnd NMOS L=0.35U W=0.875U  
Mpmosm00 vdd A net#12 vdd PMOS L=0.35U W=1.75U  
Mpmosm01 vdd B net#12 vdd PMOS L=0.35U W=1.75U  
Mpmosm02 vdd net#12 Vout vdd PMOS L=0.35U W=1.75U  
.ENDS 16-to-1-Mux AND  
  
*** SUBCIRCUIT 16-to-1-Mux_3-AND FROM CELL 3-AND(sch)  
.SUBCKT 16-to-1-Mux_3-AND A B C Vout  
** GLOBAL gnd  
** GLOBAL vdd  
XAND#0 A B net#0 _16-to-1-Mux_AND  
XAND#1 net#0 C Vout 16-to-1-Mux_AND  
.ENDS 16-to-1-Mux_3-AND  
  
*** SUBCIRCUIT 16-to-1-Mux_OR FROM CELL OR(sch)  
.SUBCKT 16-to-1-Mux_OR A B Vout  
** GLOBAL gnd  
** GLOBAL vdd  
Mmosm00 Vout net#13 gnd gnd NMOS L=0.35U W=0.875U  
Mmosm01 net#13 A gnd gnd NMOS L=0.35U W=0.875U  
Mmosm02 net#13 B gnd gnd NMOS L=0.35U W=0.075U  
Mpmosm00 vdd A net#2 vdd PMOS L=0.35U W=1.75U  
Mpmosm01 net#2 B net#11 vdd PMOS L=0.35U W=1.75U  
Mpmosm02 vdd net#11 Vout vdd PMOS L=0.35U W=1.75U  
.ENDS 16-to-1-Mux_OR  
  
*** SUBCIRCUIT 16-to-1-Mux_4-OR FROM CELL 4-OR(sch)  
.SUBCKT 16-to-1-Mux_4-OR A B C D Vout  
** GLOBAL gnd  
** GLOBAL vdd  
XOR#0 A B net#7 16-to-1-Mux_OR  
XOR#1 net#7 net#0 Vout 16-to-1-Mux_OR  
XOR#2 C D net#0 16-to-1-Mux_OR  
.ENDS 16-to-1-Mux_4-OR
```

Figure 28: Generated Spice Deck of Conventional 16-to-1 Multiplexer Schematic

```

[Ltspace XVII - [16-to-1-Mux.sp]
File Edit View Simulator Tools Window Help
[Simulator] Simulation Type: [272.692 ns] Transient Analysis [85% done] Simulation Speed: 22,804 ns/iter [File: m412]

16-to-1-Mux.sp 16-to-1-Mux.sp

*** SPICE deck for cell 16-to-1-Mux(lay) from library 16-to-1-Mux
*** Created on Thu Nov 07, 2019 12:22:18
*** Last revised on Sat Nov 09, 2019 10:46:51
*** Written on Sun Nov 10, 2019 14:16:37 by Electric VLSI Design System, version 9.07
*** Layout tech: mcmos, foundry MOSIS
*** UC SPICE *** , MIN RESIST 4.0, MIN CAPAC 0.1FF
*** P-Active*: areacap=0.9FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sq
*** N-Active*: areacap=0.9FF/um^2, edgecap=0.0FF/um, res=1.0ohms/sq
*** PolyResonator1: areacap=0.1467FF/um^2, edgcap=0.0608FF/um, res=6.2ohms/sq
*** PolyResonator2: areacap=1.0FF/um^2, edgcap=0.0FF/um, res=50.0ohms/sq
*** Transistor-Poly: areacap=0.09FF/um^2, edgcap=0.0FF/um, res=2.5ohms/sq
*** Poly-Cut: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=2.2ohms/sq
*** Active-Cut: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=2.5ohms/sq
*** Metal-1: areacap=0.1209FF/um^2, edgcap=0.1104FF/um, res=0.078ohms/sq
*** Vial: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=1.0ohms/sq
*** Metal-2: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
*** Via2: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=0.9ohms/sq
*** Metal-3: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
*** Via3: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=0.8ohms/sq
*** Metal-4: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
*** Via4: areacap=0.05FF/um^2, edgcap=0.0FF/um, res=0.8ohms/sq
*** Metal-5: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
*** Via5: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=0.8ohms/sq
*** Metal-6: areacap=0.0423FF/um^2, edgcap=0.1273FF/um, res=0.036ohms/sq
*** Hi-Res: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=1.0ohms/sq

*** TOP LEVEL CELL: 16-to-1-Mux(lay)
Mnmos#460 gnd net#6395 net#6310 gnd NMOS L=0.35U W=1.75U AS=1.378P AD=6.931P PS=3.675U PD=17.068U
Mnmos#461 net#6311 net#62934 nmcos#8461 poly-left gnd gnd NMOS L=0.35U W=1.75U AS=1.378P AD=6.931P PS=3.675U PD=3.675U
Mnmos#462 net#6312 net#62934 nmcos#8462 poly-left gnd gnd NMOS L=0.35U W=1.75U AS=1.378P AD=6.931P PS=3.675U PD=5.775U
Mnmos#463 gnd net#63334 nmcos#8463 poly-left net#63110 and NMOS L=0.35U W=1.75U AS=1.378P AD=6.931P PS=3.675U PD=17.068U
Mnmos#464 net#6310 net#64042 nmcos#8464 poly-left gnd gnd NMOS L=0.35U W=1.75U AS=1.378P AD=6.931P PS=3.675U PD=3.675U
Mnmos#465 net#6309 net#65656 nmcos#8465 poly-left net#65566 gnd gnd NMOS L=0.35U W=1.75U AS=1.914P AD=6.931P PS=3.937U PD=17.068U
Mnmos#466 net#6566 net#6360#18 nmcos#8466 poly-left net#65576 gnd gnd NMOS L=0.35U W=1.75U AS=1.914P AD=1.914P PS=3.937U PD=3.937U
Mnmos#467 net#6359#3 contact#2359 metal-1-poly#silicon-1 net#62934#2 nmcos#8467 poly-right gnd gnd NMOS L=0.35U W=1.75U AS=6.931P AD=1.991P PS=17.068U PD=5.775U
Mnmos#468 net#6571 net#6315#15 nmcos#8468 poly-left net#62934#3 contact#2390 metal-1-poly#silicon-1 gnd NMOS L=0.35U W=1.75U AS=1.608P AD=1.914P PS=4.462U PD=3.937U
Mnmos#469 gnd D1#0 nmcos#8469 poly-left net#6303 gnd NMOS L=0.35U W=1.75U AS=1.914P AD=6.931P PS=3.937U PD=17.068U
Mnmos#470 net#6303 net#6315#15 nmcos#8470 poly-left net#6314#3 gnd NMOS L=0.35U W=1.75U AS=1.914P AD=1.914P PS=3.937U PD=3.937U
Mnmos#471 net#62934 nmcos#8471 poly-left gnd NMOS L=0.35U W=1.75U AS=1.914P AD=1.914P PS=3.937U PD=3.937U
Mnmos#472 gnd S1#2 nmcos#8472 poly-left net#6314#4 and NMOS L=0.35U W=1.75U AS=1.914P AD=1.914P PS=3.937U PD=5.775U
Mnmos#473 gnd D2#0 nmcos#8473 poly-left net#6313#3 and NMOS L=0.35U W=1.75U AS=1.914P AD=6.931P PS=3.937U PD=17.068U
Mnmos#474 net#6339 S1#2 nmcos#8474 poly-left net#6349#3 and NMOS L=0.35U W=1.75U AS=1.914P AD=1.914P PS=3.937U PD=3.937U
Mnmos#475 net#6333 net#6340#12 nmcos#8475 poly-right gnd gnd NMOS L=0.35U W=1.75U AS=6.931P AD=1.991P PS=17.068U PD=5.775U
Mnmos#476 net#6344 net#6360#2 nmcos#8476 poly-left net#6340# and NMOS L=0.35U W=1.75U AS=1.608P AD=1.914P PS=4.462U PD=3.937U
Mnmos#477 gnd D3#3 nmcos#8477 poly-left net#6429 gnd NMOS L=0.35U W=1.75U AS=1.914P AD=6.931P PS=3.937U PD=17.068U
Mnmos#478 net#6429 S1#1 nmcos#8478 poly-left net#6434 gnd NMOS L=0.35U W=1.75U AS=1.914P AD=1.914P PS=3.937U PD=3.937U
Mnmos#479 net#64044#4 contact#2430 metal-1-n-act net#6420#2 nmcos#479 poly-right gnd gnd NMOS L=0.35U W=1.75U AS=6.931P AD=1.991P PS=17.068U PD=5.775U
Mnmos#480 net#6433 S0#7 nmcos#480 poly-left net#6420#3 contact#2438 metal-1-poly#silicon-1 gnd NMOS L=0.35U W=1.75U AS=1.608P AD=1.914P PS=4.462U PD=3.937U

```

Figure 29: Generated Spice Deck of Conventional 16-to-1 Multiplexer Layout

```

* Spice XVI - [16-to-1-Mux.sp]
File Edit View Simulate Tools Window Help
16-to-1-Mux.sp 16-to-1-Mux.sp
* 16-to-1-Mux.sp
** Extracted Parasitic Capacitors ***
C0 net@6310 0 7.63tF
C1 net@63954#3contact@2359_metal-1-polysilicon-1 0 5.15fF
C2 net@6369 0 19.742tF
C3 net@6297 0 10.126fF
C4 net@6333#4contact@2373_metal-1-polysilicon-1 0 5.094fF
C5 net@6404#1contact@2374_metal-1-polysilicon-1 0 7.35fF
C6 net@6293#3contact@2390_metal-1-polysilicon-1 0 7.135fF
C7 D0#0contact@2369_metal-1-metal-2 0 7.022fF
C8 net@6360#3contact@2221_metal-1-polysilicon-1 0 20.552fF
C9 net@6311#4contact@2205_metal-1-polysilicon-1 0 11.324fF
C10 ns@6304 0 7.35fF
C11 D1#3contact@2393_metal-1-polysilicon-1 0 6.04fF
C12 S0#3contact@2405_metal-1-polysilicon-1 0 4.472fF
C13 net@6340 0 7.41fF
C14 D2#3contact@2409_metal-1-polysilicon-1 0 4.205fF
C15 net@6333 0 9.128fF
C16 S1 0 74.852fF
C17 net@6420#3contact@2438_metal-1-polysilicon-1 0 7.408fF
C18 D3 0 4.606fF
C19 net@6404#4contact@2430_metal-1-n-act 0 10.686fF
C20 S0 0 58.912fF
C21 net@6261#3contact@2440_metal-1-p-act 0 8.786fF
C22 D2 0 4.019fF
C23 D1 0 5.874fF
C24 D0 0 5.684fF
C25 net@6609 0 7.637fF
C26 net@6694#3contact@2477_metal-1-polysilicon-1 0 5.15fF
C27 net@6668 0 12.038fF
C28 net@6659 0 10.126fF
C29 net@6632#3contact@2491_metal-1-polysilicon-1 0 5.094fF
C30 net@6703#1contact@2492_metal-1-polysilicon-1 0 7.35fF
C31 net@6659#2#3contact@2505_metal-1-polysilicon-1 0 7.135fF
C32 D4#0#3contact@2506_metal-1-metal-2 0 7.022fF
C33 net@6659#4#3contact@2539_metal-1-polysilicon-1 0 20.552fF
C34 net@6614#1#3contact@2551_metal-1-polysilicon-1 0 11.324fF
C35 net@6603 0 7.35fF
C36 D5#3contact@2511_metal-1-polysilicon-1 0 6.04fF
C37 S0#2#1contact@2523_metal-1-polysilicon-1 0 4.472fF
C38 net@6639 0 7.41fF
C39 D6#3contact@2527_metal-1-polysilicon-1 0 4.205fF
C40 net@6632 0 9.128fF
C41 net@6719#3contact@2556_metal-1-polysilicon-1 0 7.408fF
C42 D7 0 4.606fF
C43 net@6703#4#4contact@2548_metal-1-n-act 0 10.686fF
C44 net@6668#3#4contact@2558_metal-1-p-act 0 8.786fF
C45 D6 0 4.019fF
C46 D5 0 5.874fF
C47 D4 0 5.684fF

```

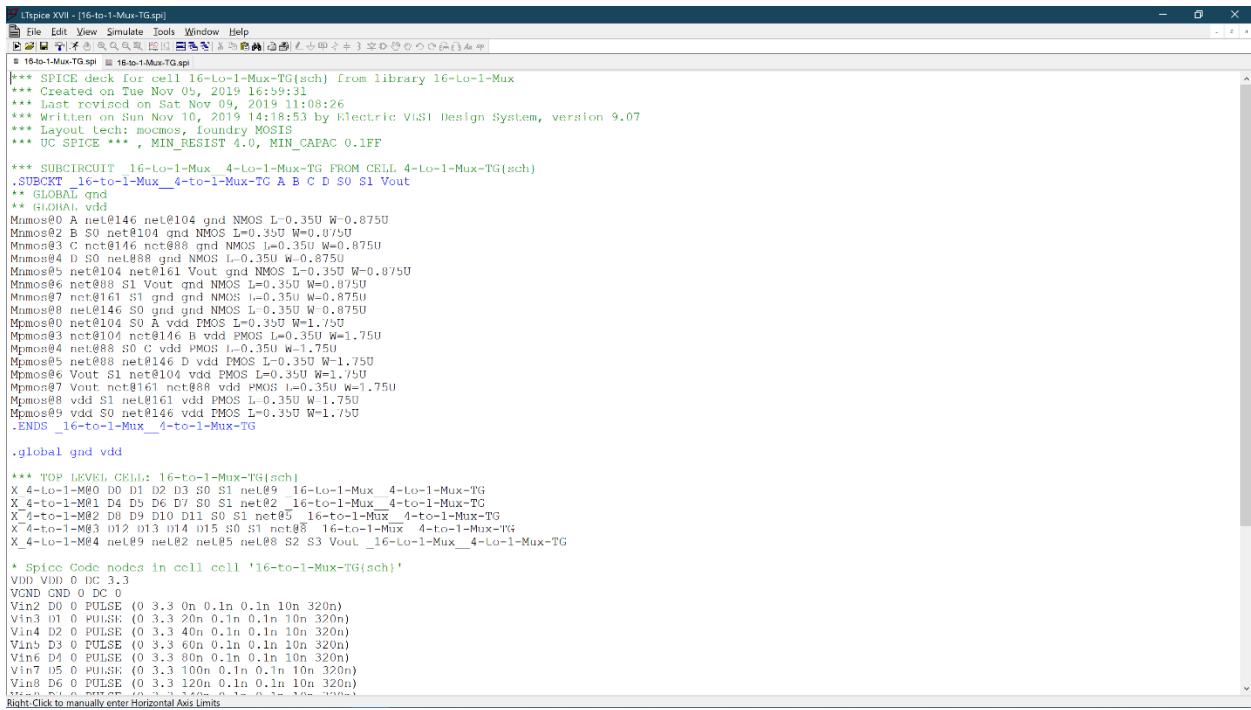
Figure 30: Extracted Parasitic Capacitors Sample of Conventional 16-to-1 Multiplexer Layout

```

* Spice XVI - [16-to-1-Mux.sp]
File Edit View Simulate Tools Window Help
16-to-1-Mux.sp 16-to-1-Mux.sp
* 16-to-1-Mux.sp
** Extracted Parasitic Resistors ***
R0 net@6293#1pin@1329_polySilicon-1 7.75
R1 net@6293#1pin@1329_polySilicon-1 net@6293#1pin@1329 polysilicon-1#0 9.623
R2 net@6293#1pin@1329_polySilicon-1#0 net@6293#1pin@1329 polysilicon-1#1 9.623
R3 net@6293#1pin@1329_polySilicon-1#1 net@6293#1pin@1329 polysilicon-1#2 9.623
R4 net@6293#1pin@1329_polySilicon-1#2 net@6293#1pin@1329 polysilicon-1#3 9.623
R5 net@6293#1pin@1329_polySilicon-1#3 net@6293#1pin@1329 polysilicon-1#4 9.623
R6 net@6293#1pin@1329_polySilicon-1#4 net@6293#1pin@1329 polysilicon-1#5 9.623
R7 net@6293#1pin@1329_polySilicon-1#5 net@6293#1pin@1329 polysilicon-1#6 9.623
R8 net@6293#1pin@1329_polySilicon-1#6 net@6293#1pin@1329 polysilicon-1#7 9.623
R9 net@6293#1pin@1329_polySilicon-1#7 net@6293#1pin@1329 polysilicon-1#8 9.623
R10 net@6293#1pin@1329_polySilicon-1#8 net@6293#1pin@1329 polysilicon-1#9 9.623
R11 net@6293#1pin@1329_polySilicon-1#9 net@6293#1pin@1329 polysilicon-1#10 9.623
R12 net@6293#1pin@1329_polySilicon-1#10 net@6293#1pin@1329 polysilicon-1#11 9.623
R13 net@6293#1pin@1329_polySilicon-1#11 net@6293#1pin@1329 polysilicon-1#12 9.623
R14 net@6293#1pin@1329_polySilicon-1#12 net@6293#1pin@1329 polysilicon-1#13 9.623
R15 net@6293#1pin@1329_polySilicon-1#13 net@6293#1pin@1329 polysilicon-1#14 9.623
R16 net@6293#1pin@1329_polySilicon-1#14 net@6293#1pin@1329 polysilicon-1#15 9.623
R17 net@6293#1pin@1329_polySilicon-1#15 net@6293#1pin@1329 polysilicon-1#16 9.623
R18 net@6293#1pin@1329_polySilicon-1#16 net@6293#1pin@1329 polysilicon-1#17 9.623
R19 net@6293#1pin@1329_polySilicon-1#17 net@6293#1pin@1329 polysilicon-1#18 9.623
R20 net@6293#1pin@1329_polySilicon-1#18 net@6293#1pin@1329 polysilicon-1#19 9.623
R21 net@6293#1pin@1329_polySilicon-1#19 net@6293#1pin@1329 polysilicon-1#20 9.623
R22 net@6293#1pin@1329_polySilicon-1#20 net@6293#1pin@1329 polysilicon-1#21 9.623
R23 net@6293#1pin@1329_polySilicon-1#21 net@6293#1pin@1329 polysilicon-1#22 9.623
R24 net@6293#1pin@1329_polySilicon-1#22 net@6293#1pin@1329 polysilicon-1#23 9.623
R25 net@6293#3#3contact@2390_metal-1-polysilicon-1 net@6293#3#3contact@2390_metal-1-polysilicon-1#0 8.68
R26 net@6293#3#3contact@2390_metal-1-polysilicon-1#0 net@6293#3#3contact@2390_metal-1-polysilicon-1#1 8.68
R27 net@6293#3#3contact@2390_metal-1-polysilicon-1#1 net@6293#3#3contact@2390_metal-1-polysilicon-1#2 8.68
R28 net@6293#3#3contact@2390_metal-1-polysilicon-1#2 net@6293#3#3contact@2390_metal-1-polysilicon-1#3 8.68
R29 net@6293#3#3contact@2390_metal-1-polysilicon-1#3 net@6293#1pin@1329 polysilicon-1 8.68
R30 net@6297 0
R31 D1#0nnmos@465 poly-left#0 D1#0nnmos@469 poly-left#0 9.953
R32 D1#0nnmos@469 poly-left#0 D1#0nnmos@469 poly-left#1 9.953
R33 D1#0nnmos@469 poly-left#1 D1#0nnmos@469 poly-left#2 9.953
R34 D1#0nnmos@469 poly-left#2 D1#0nnmos@469 poly-left#3 9.953
R35 D1#0nnmos@469 poly-left#3 D1#0nnmos@469 poly-left#4 9.953
R36 D1#0nnmos@469 poly-left#4 D1#0nnmos@469 poly-left#5 9.953
R37 D1#0nnmos@469 poly-left#5 D1#0nnmos@469 poly-left#6 9.953
R38 D1#0nnmos@469 poly-left#6 D1#0nnmos@469 poly-left#7 9.953
R39 D1#0nnmos@469 poly-left#7 D1#0nnmos@469 poly-left#8 9.953
R40 D1#0nnmos@469 poly-left#8 D1#0nnmos@469 poly-left#9 9.953
R41 D1#0nnmos@469 poly-left#9 D1#0nnmos@469 poly-left#10 9.953
R42 D1#0nnmos@469 poly-left#10 D1#0nnmos@469 poly-left#11 9.953
R43 D1#0nnmos@469 poly-left#11 D1#0nnmos@469 poly-left#12 9.953
R44 D1#0nnmos@469 poly-left#12 D1#0nnmos@469 poly-left#13 9.953
R45 D1#0nnmos@469 poly-left#13 D1#0nnmos@469 poly-left#14 9.953
R46 D1#0nnmos@469 poly-left#14 D1#0nnmos@469 poly-left#15 9.953

```

Figure 31: Extracted Parasitic Resistors Sample of Conventional 16-to-1 Multiplexer Layout



```

16-to-1-Mux-TG.sp1 16-to-1-Mux-TG.sch
File Edit View Simulate Tools Window Help
16-to-1-Mux-TG.sch 16-to-1-Mux-TG.sp1
16-to-1-Mux-TG.sch
*** SPICE deck for cell 16-To-1-Mux-TG(sch) from library 16-To-1-Mux
*** Created on Tue Nov 05, 2019 16:59:31
*** Last revised on Sat Nov 09, 2019 11:08:26
*** Written on Sun Nov 10, 2019 14:18:53 by Electric VLSI Design System, version 9.07
*** Layout Tech: moscos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** SUBCIRCUIT 16-To-1-Mux 4-To-1-Mux-TG FROM CELL 4-To-1-Mux-TG(sch)
.SUBCKT _16-to-1-Mux_4-to-1-Mux-TG A B C D S0 S1 Vout
** GLOBAL gnd
** GND_VDD_VSS

Mmosc80 A net@146 net@104 and NMOS L=0.35U W=0.875U
Mmosc82 B S0 net@104 and NMOS L=0.35U W=0.875U
Mmosc83 C net@146 net@88 and NMOS L=0.35U W=0.875U
Mmosc84 D S0 net@88 and NMOS L=0.35U W=0.875U
Mmosc85 net@104 net@161 Vout gnd NMOS L=0.35U W=0.875U
Mmosc86 net@88 S1 Vout gnd NMOS L=0.35U W=0.875U
Mmosc87 net@161 S1 gnd gnd NMOS L=0.35U W=0.875U
Mmosc88 net@146 S0 gnd gnd NMOS L=0.35U W=0.875U
Mmosc89 net@104 S0 vdd PMOS L=0.35U W=1.75U
Mmosc90 net@104 net@146 B vdd PMOS L=0.35U W=1.75U
Mmosc91 net@88 S0 C vdd PMOS L=0.35U W=1.75U
Mmosc92 net@146 S0 D vdd PMOS L=0.35U W=1.75U
Mmosc93 net@146 S0 E vdd PMOS L=0.35U W=1.75U
Mmosc94 net@146 S0 F vdd PMOS L=0.35U W=1.75U
Mmosc95 net@146 S0 G vdd PMOS L=0.35U W=1.75U
Mmosc96 Vout S1 net@161 vdd PMOS L=0.35U W=1.75U
Mmosc97 Vout net@161 net@88 vdd PMOS L=0.35U W=1.75U
Mmosc98 vdd S1 net@161 vdd PMOS L=0.35U W=1.75U
Mmosc99 vdd S0 net@146 vdd PMOS L=0.35U W=1.75U
.ENDS _16-to-1-Mux_4-to-1-Mux-TG

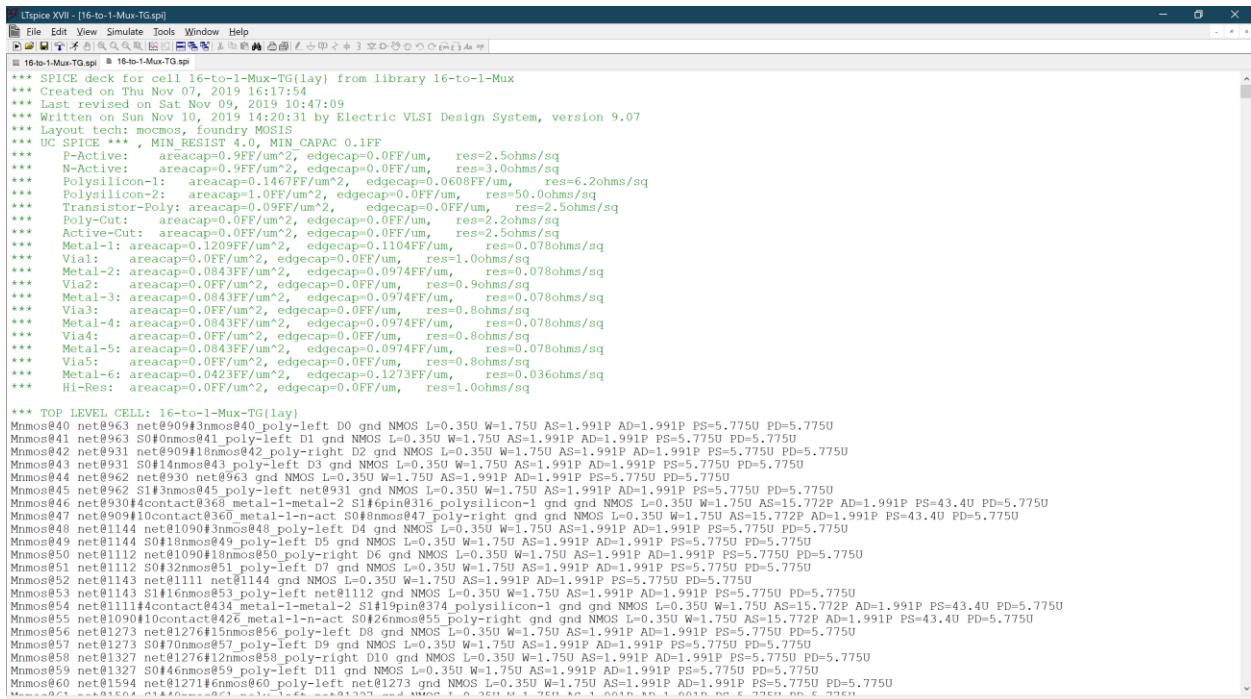
.global gnd vdd

*** TOP LEVEL CELL: 16-to-1-Mux-TG(sch)
X 4-to-1-M80 D0 D1 D2 D3 S0 S1 net@9 net@161 16-To-1-Mux 4-To-1-Mux-TG
X 4-to-1-M81 D0 D1 D2 D3 S0 S1 net@2 16-To-1-Mux 4-To-1-Mux-TG
X 4-to-1-M82 D0 D1 D2 D3 S0 S1 net@3 16-To-1-Mux 4-To-1-Mux-TG
X 4-to-1-M83 D12 D13 D14 D15 S0 S1 net@8 16-To-1-Mux 4-To-1-Mux-TG
X 4-to-1-M84 net@9 net@2 net@5 S2 S3 Vout _16-to-1-Mux_4-to-1-Mux-TG

* Spice Code nodes in cell cell '16-to-1-Mux-TG(sch)'
VDD VDD 0 DC 3.3
VDD GND 0 DC 0
Vin2 D0 0 PULSE (0 3.3 0n 0.1n 10n 320n)
Vin3 D1 0 PULSE (0 3.3 20n 0.1n 10n 320n)
Vin4 D2 0 PULSE (0 3.3 40n 0.1n 10n 320n)
Vin5 D3 0 PULSE (0 3.3 60n 0.1n 10n 320n)
Vin6 D4 0 PULSE (0 3.3 80n 0.1n 10n 320n)
Vin7 D5 0 PULSE (0 3.3 100n 0.1n 10n 320n)
Vin8 D6 0 PULSE (0 3.3 120n 0.1n 10n 320n)
Vin9 D7 0 PULSE (0 3.3 140n 0.1n 10n 320n)
Vin10 D8 0 PULSE (0 3.3 160n 0.1n 10n 320n)
Vin11 D9 0 PULSE (0 3.3 180n 0.1n 10n 320n)
Vin12 D10 0 PULSE (0 3.3 200n 0.1n 10n 320n)
Vin13 D11 0 PULSE (0 3.3 220n 0.1n 10n 320n)
Vin14 D12 0 PULSE (0 3.3 240n 0.1n 10n 320n)
Vin15 D13 0 PULSE (0 3.3 260n 0.1n 10n 320n)
Vin16 D14 0 PULSE (0 3.3 280n 0.1n 10n 320n)
Vin17 D15 0 PULSE (0 3.3 300n 0.1n 10n 320n)
Right-Click to manually enter Horizontal Axis limits

```

Figure 32: Generated Spice Deck of Transmission Gate 16-to-1 Multiplexer Schematic



```

16-to-1-Mux-TG.sp1 16-to-1-Mux-TG.lay
File Edit View Simulate Tools Window Help
16-to-1-Mux-TG.lay 16-to-1-Mux-TG.sp1
16-to-1-Mux-TG.lay
*** SPICE deck for cell 16-to-1-Mux-TG(lay) from library 16-to-1-Mux
*** Created on Thu Oct 07, 2019 16:17:54
*** Last revised on Sat Nov 09, 2019 10:47:09
*** Written on Sun Nov 10, 2019 14:20:31 by Electric VLSI Design System, version 9.07
*** Layout Tech: moscos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

P-Active: areacap=0.9FF/um^2, edgcap=0.0FF/um, res=2.5ohms/sq
N-Active: areacap=0.9FF/um^2, edgcap=0.0FF/um, res=3.0ohms/sq
PolySilicon-1: areacap=0.1467FF/um^2, edgcap=0.0608FF/um, res=6.2ohms/sq
PolySilicon-2: areacap=1.0FF/um^2, edgcap=0.0FF/um, res=50.0ohms/sq
Transistor-Poly: areacap=0.09FF/um^2, edgcap=0.0FF/um, res=2.5ohms/sq
Poly-Cut: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=2.0ohms/sq
Active-Cut: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=2.5ohms/sq
Metal-1: areacap=0.0943FF/um^2, edgcap=0.104FF/um, res=0.078ohms/sq
Metal-2: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.100ohms/sq
Via1: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=0.078ohms/sq
Metal-3: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
VIA2: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
Metal-4: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
VIA3: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
Metal-5: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
VIA4: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
Metal-6: areacap=0.0843FF/um^2, edgcap=0.0974FF/um, res=0.078ohms/sq
VIA5: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=0.8ohms/sq
Metal-7: areacap=0.0843FF/um^2, edgcap=0.1273FF/um, res=0.036ohms/sq
Metal-8: areacap=0.0423FF/um^2, edgcap=0.0423FF/um, res=0.07750
Metal-9: areacap=0.0FF/um^2, edgcap=0.0FF/um, res=1.0ohms/sq

*** TOP LEVEL CELL: 16-to-1-Mux-TG(lay)
Mmosc80 net@9963 net@90943nmos#840 poly-left D0 and NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc81 net@9963 S0#nmos#841 poly-left D1 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc82 net@9931 net@8909418nmos#842 poly-right D0 and NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc83 net@9931 S0#14nmos#843 poly-left D3 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc84 net@9963 net@9931 net@9963 S1#nmos#845 poly-left net@9931 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc85 net@99304contact#368 metal-1-metal-2 S1#6pin316 polysilicon-1 qnd qnd NMOS L=0.35U W=1.75U AS=15.772P AD=1.991P PS=43.4U PD=5.775U
Mmosc86 net@9909110contact#360 metal-1-n-act S0#nmos#847 poly-right qnd qnd NMOS L=0.35U W=1.75U AS=15.772P AD=1.991P PS=43.4U PD=5.775U
Mmosc87 net@991144 net@90943nmos#848 poly-left D4 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc88 net@991144 S0#14nmos#849 poly-left D5 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc89 net@99112 S0#10nmos#850 poly-right D6 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc90 net@99112 S0#43nmos#851 poly-left D7 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc91 net@99113 S0#11nmos#852 poly-left net@1111 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc92 net@99113 S1#16nmos#853 poly-left net@1112 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc93 net@991114#4contact#843A metal-1-metal-2 S1#19pin374 polysilicon-1 qnd qnd NMOS L=0.35U W=1.75U AS=15.772P AD=1.991P PS=43.4U PD=5.775U
Mmosc94 net@991114#4contact#843A metal-1-n-aact S0#26nmos#855 poly-right qnd qnd NMOS L=0.35U W=1.75U AS=15.772P AD=1.991P PS=43.4U PD=5.775U
Mmosc95 net@991114#4contact#842A metal-1-n-aact S0#26nmos#856 poly-left D8 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc96 net@1273 net@1276#15nmos#856 poly-left D8 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc97 net@1273 S0#70nmos#857 poly-left D9 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc98 net@1327 net@1276#12nmos#858 poly-right D10 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc99 net@1327 S0#46nmos#859 poly-left D11 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U
Mmosc99 net@1594 net@1271#6nmos#860 poly-left net@1273 qnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U

```

Figure 33: Generated Spice Deck of Transmission Gate 16-to-1 Multiplexer Layout

```

Topice XVI - [16-to-1-Mux-TG.spi]
File Edit View Simulate Tools Window Help
16-to-1-Mux-TG.spi 16-to-1-Mux-TG.spi
** Extracted Parasitic Capacitors ***
C0 net#8963 0 9.104fF
C1 D0 0 7.118fF
C2 D1 0 6.994fF
C3 net#8931 0 8.084fF
C4 D2 0 7.043fF
C5 D3 0 7.02fF
C6 net#8962 0 11.492fF
C7 net#8930#4contact#8360_metal-1-metal-2 0 14.629fF
C8 net#8909#5contact#8366_metal-1-metal-2 0 8.259fF
C9 net#8909#6contact#8360_metal-1-n-act 0 4.714fF
C10 S0#4contact#8362_metal-1-metal-2 0 10.295fF
C11 S1#4contact#8362_metal-1-metal-2 0 0.013fF
C12 net#8174 0 9.107fF
C13 D4 0 7.118fF
C14 D5 0 6.994fF
C15 net#8112 0 8.084fF
C16 D6 0 7.043fF
C17 D7 0 7.02fF
C18 net#8143 0 17.199fF
C19 net#81111#4contact#834_metal-1-metal-2 0 14.629fF
C20 net#81090#5contact#8432_metal-1-metal-2 0 8.259fF
C21 C0#4contact#8346_metal-1-n-act 0 4.714fF
C22 S0#4contact#8426_metal-1-metal-2 0 16.052fF
C23 S1#21contact#8434_metal-1-metal-2 0 15.152fF
C24 net#81273 0 9.104fF
C25 D8 0 7.118fF
C26 D9 0 6.994fF
C27 net#81327 0 8.084fF
C28 D10 0 7.043fF
C29 D11 0 7.02fF
C30 net#81594 0 16.809fF
C31 net#81271 0 14.629fF
C32 net#81275 0 12.259fF
C33 net#81276#4contact#8492_metal-1-n-act 0 4.714fF
C34 S0#36contact#8494_metal-1-metal-2 0 16.819fF
C35 S1#29contact#8504_metal-1-metal-2 0 15.194fF
C36 net#81414 0 9.104fF
C37 D12 0 7.118fF
C38 D13 0 6.994fF
C39 net#81382 0 8.084fF
C40 D14 0 7.043fF
C41 D15 0 7.02fF
C42 net#81413 0 11.492fF
C43 net#81381#4contact#8566_metal-1-metal-2 0 14.629fF
C44 net#81381#5contact#8564_metal-1-metal-2 0 8.259fF
C45 net#81369#10contact#8558_metal-1-n-act 0 4.714fF
C46 S0 0 11.814fF
C47 C1 0 10.602fF
C48 C2 0 10.602fF

```

Figure 34: Extracted Parasitic Capacitors Sample of Transmission Gate 16-to-1 Multiplexer Layout

```

Topice XVI - [16-to-1-Mux-TG.spi]
File Edit View Simulate Tools Window Help
16-to-1-Mux-TG.spi 16-to-1-Mux-TG.spi
** Extracted Parasitic Resistors ***
R0 S0#4mos#841_poly-left#0 S0#0mos#841_poly-left#0 9.688
R1 S0#4mos#841_poly-left#1 S0#0mos#841_poly-left#1 9.688
R2 S0#4mos#841_poly-left#1 S0#0mos#841_poly-left#2 9.688
R3 S0#0mos#841_poly-left#2 S0#1pin@333 polysilicon-1 9.688
R4 net#8909#0 net#8909#1 9.858
R5 net#8909#1 net#8909#2 9.858
R6 net#8909#2 net#8909#3 9.858
R7 net#8909#3 net#8909#4 9.858
R8 net#8909#4 net#8909#5 9.858
R9 net#8909#4 net#8909#6 9.858
R10 net#8909#5 net#8909#6 9.858
R11 net#8909#6 net#8909#7 9.858
R12 net#8909#7 net#8909#8 9.858
R13 net#8909#8 net#8909#9 9.858
R14 net#8909#9 net#8909#10 9.858
R15 net#8909#10 net#8909#11 9.858
R16 net#8909#11 net#8909#12 9.858
R17 net#8909#12 net#8909#13 9.858
R18 net#8909#13 net#8909#14 9.858
R19 net#8909#14 net#8909#15 9.858
R20 net#8909#15 net#8909#16 9.858
R21 net#8909#16 net#8909#17 9.858
R22 net#8909#17 net#8909#18 9.858
R23 net#8909#18 net#8909#19 9.858
R24 net#8909#19 net#8909#20 9.858
R25 net#8909#20 net#8909#21 9.858
R26 net#8909#21 net#8909#22 9.858
R27 net#8909#22 net#8909#23 9.858
R28 net#8909#23 net#8909#1pin@330 polysilicon-1 9.858
R29 net#8909#2pmos#841_poly-left#net#8909#2pmos#841_poly-left#0 9.688
R30 net#8909#2pmos#841_poly-left#0 net#8909#2pmos#841_poly-left#1 9.688
R31 net#8909#2pmos#841_poly-left#1 net#8909#2pmos#841_poly-left#2 9.688
R32 net#8909#2pmos#841_poly-left#2 net#8909 9.688
R33 net#8909#3mos#840_poly-left#net#8909#3mos#840_poly-left#0 9.688
R34 net#8909#3mos#840_poly-left#0 net#8909#3mos#840_poly-left#1 9.688
R35 net#8909#3mos#840_poly-left#1 net#8909#3mos#840_poly-left#2 9.688
R36 net#8909#3mos#840_poly-left#2 net#8909#4pin@339 polysilicon-1 9.688
R37 net#8909 net#8909#1 9.743
R38 net#8909#0 net#8909#1 9.743
R39 net#8909#1 net#8909#2 9.743
R40 net#8909#2 net#8909#3 9.743
R41 net#8909#3 net#8909#4 9.743
R42 net#8909#4 net#8909#5 9.743
R43 net#8909#5 net#8909#4pin@338 polysilicon-1 9.743
R44 net#8909#5contact#8366_metal-1-metal-2 net#8909#5contact#8366_metal-1-metal-2#0 9.3
R45 net#8909#5contact#8366_metal-1-metal-2#0 net#8909#5contact#8366_metal-1-metal-2#1 9.3
R46 net#8909#5contact#8366_metal-1-metal-2#1 net#8909#5contact#8366_metal-1-metal-2#2 9.3
R47 net#8909#5contact#8366_metal-1-metal-2#2 net#8909#5contact#8366_metal-1-metal-2#3 9.3

```

Figure 35: Extracted Parasitic Resistors Sample of Transmission Gate 16-to-1 Multiplexer Layout

Section 7: LTSPICE Simulations:

After creating the schematic and layout design of the 16-to-1 Multiplexer, waveforms were created using LTSPICE. These waveforms were created by using Spice Code (Figure 27) to initialize our VDD, GND, and our many inputs, D0-D15, and S0-S3, so that it could test certain computations. The computations that we tested set each input (D0-D15) for 50 nanoseconds at different times, then back to low; in other words, 100 nanoseconds period, with rise time and fall time of 5 nanoseconds and 50% duty cycle. Each of the inputs were high at different times so they wouldn't be able to relate to each other. After that, we tested all the computations for the selector (S0-S3), starting from 0 to 15. This way, it'll be able to output each individual input and show a wavelike output. The computations that we tested are the same between the schematic and layout. We were able to verify the waveforms obtained from LTSPICE were correct by matching it with the truth table on Table 1.

Section 7.1: Schematic:

For the schematic, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the inputs and confirming that the output shows a wavelike form.

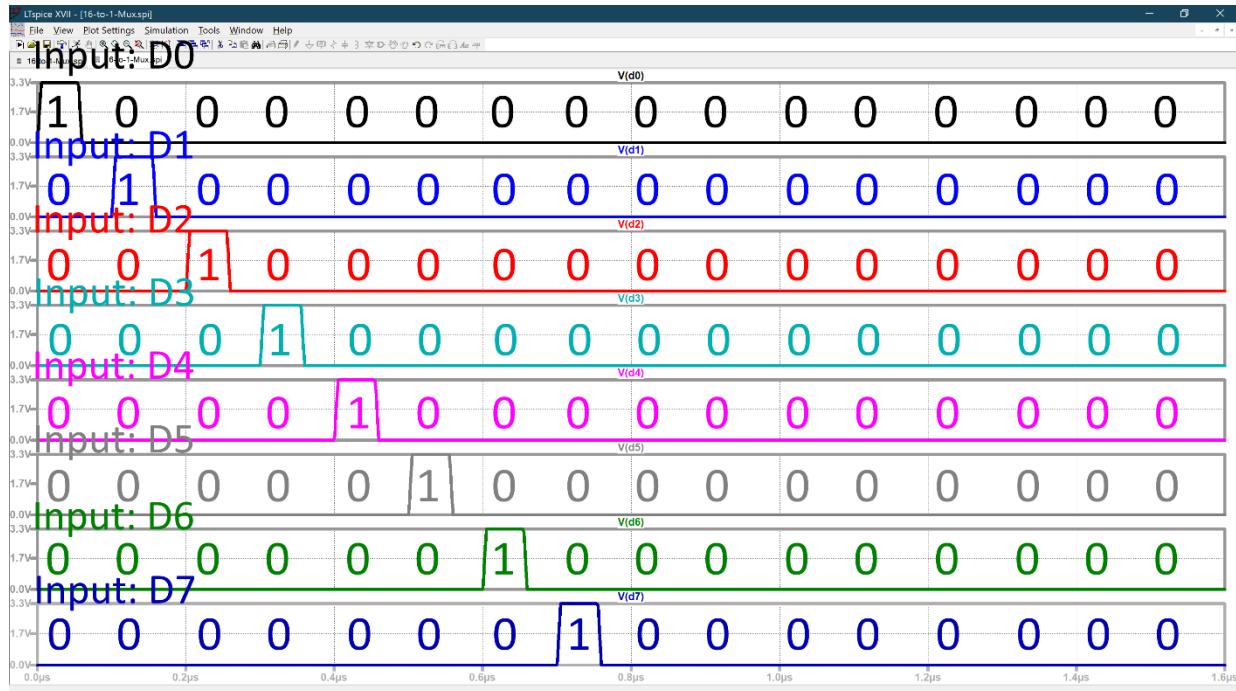


Figure 36.1: LTSPICE Waveforms of Schematic Design of a 16-to-1 Multiplexer (Inputs)

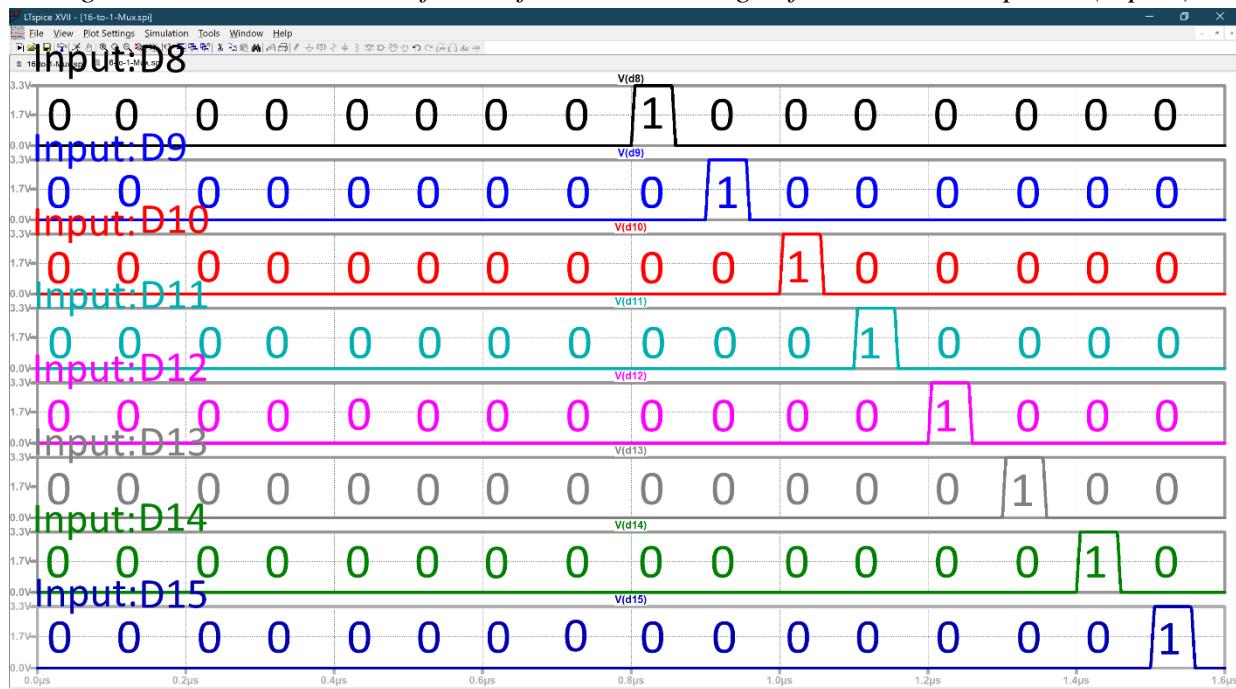


Figure 36.2: LTSPICE Waveforms of Schematic Design of a 16-to-1 Multiplexer (Inputs)

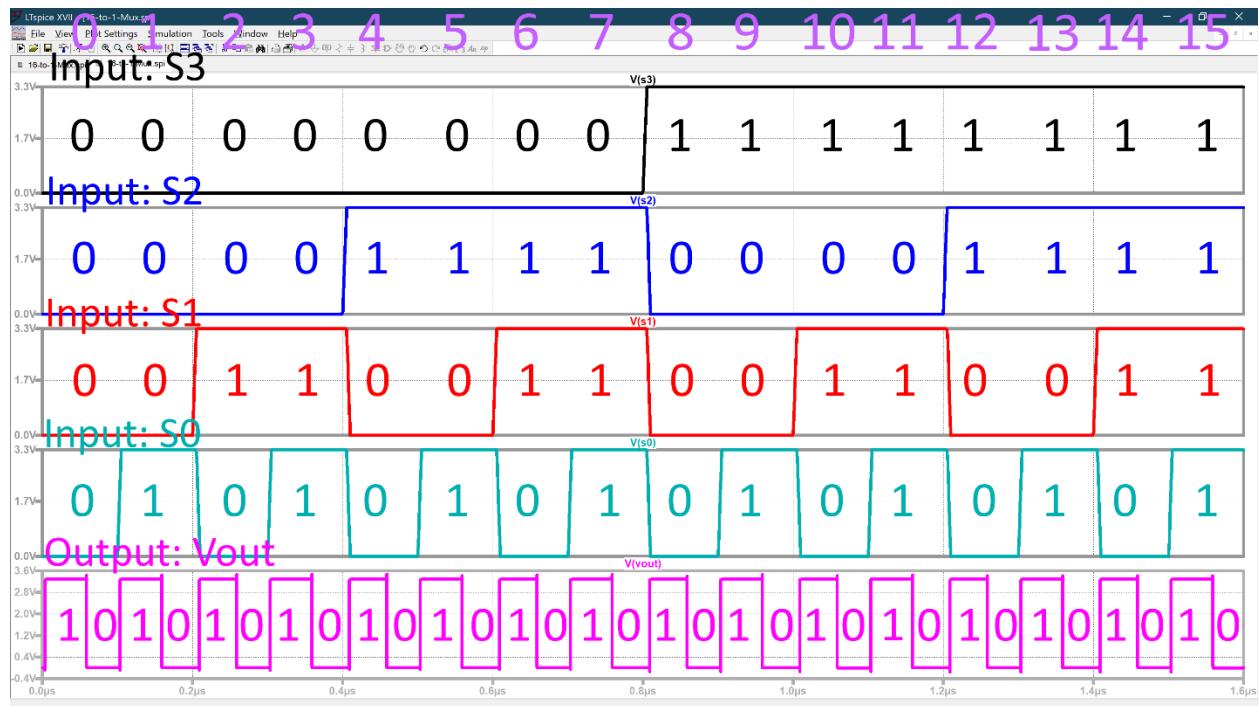


Figure 37: LTSPICE Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Outputs)

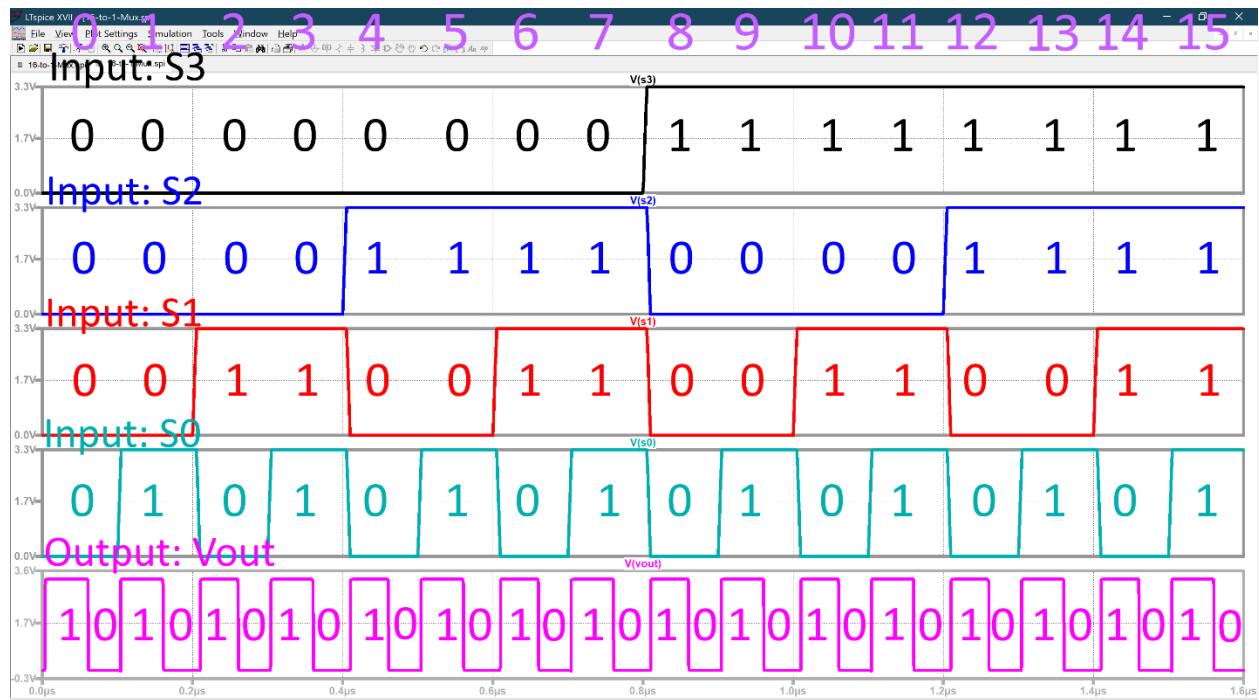


Figure 38: LTSPICE Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Outputs)

Section 7.2: Layout:

For the layout, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the inputs and confirming that the output shows a wavelike form.

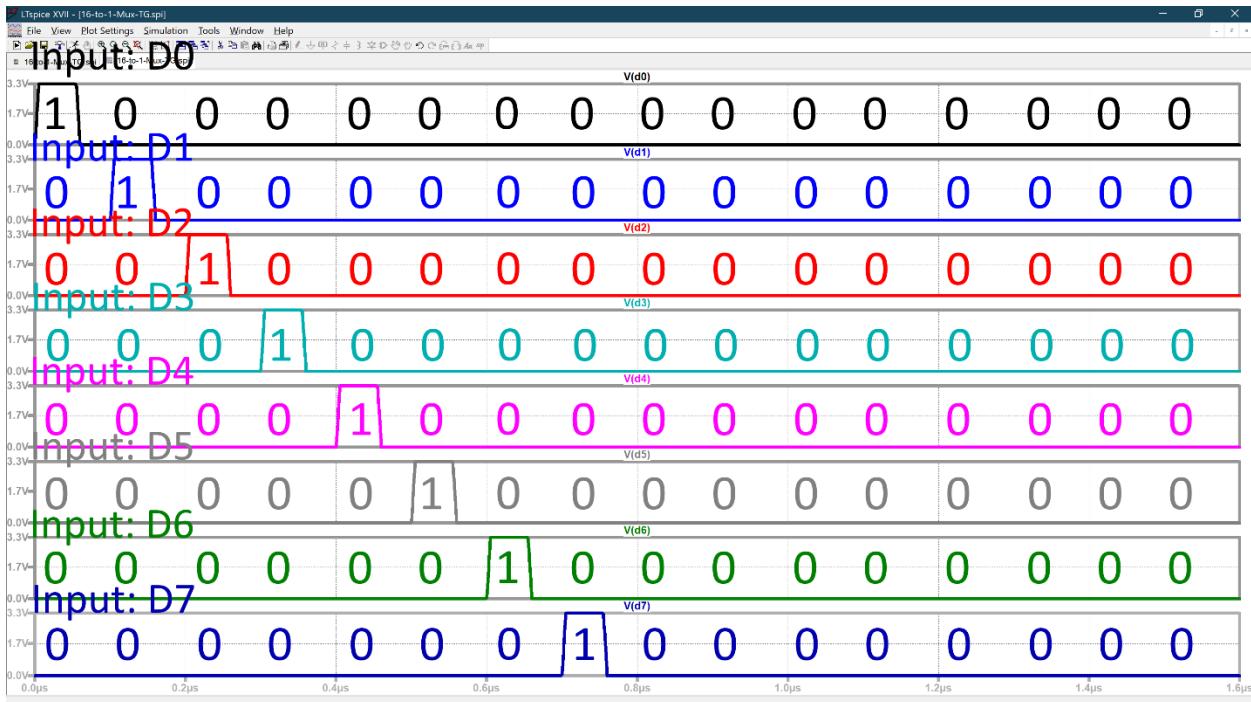


Figure 39.1: LTSPICE Waveforms of Layout Design of a 16-to-1 Multiplexer (Inputs)

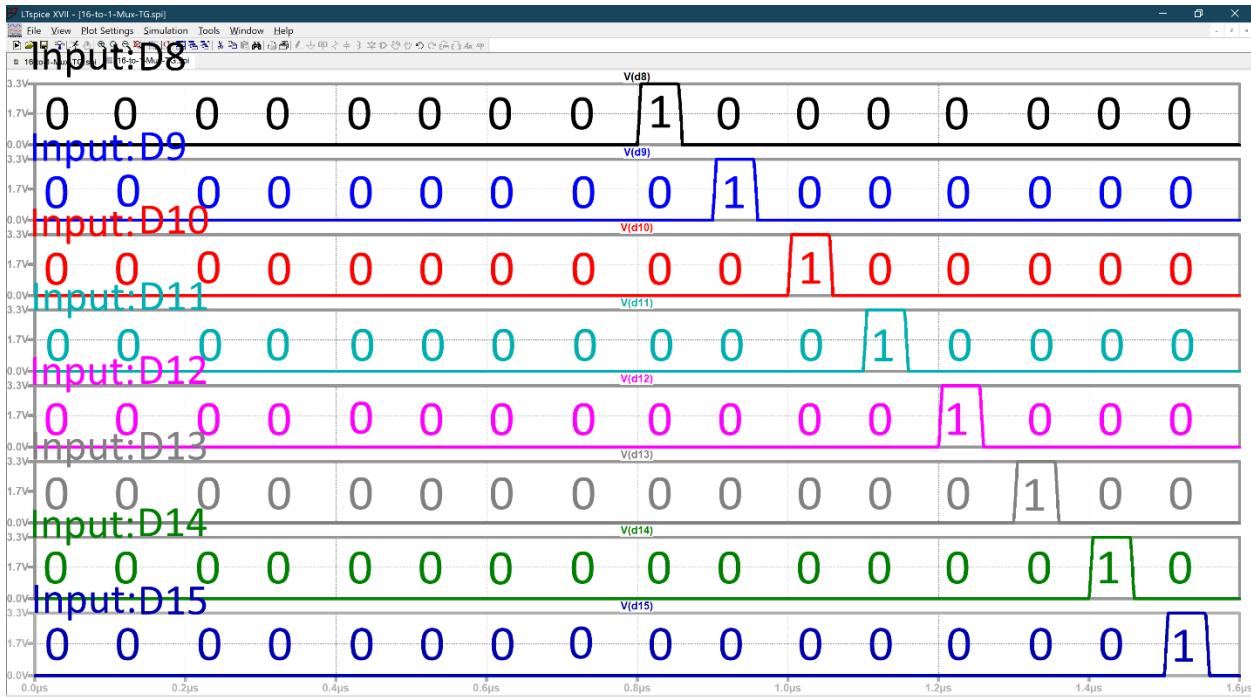


Figure 39.2: LTSPICE Waveforms of Layout Design of a 16-to-1 Multiplexer (Inputs)

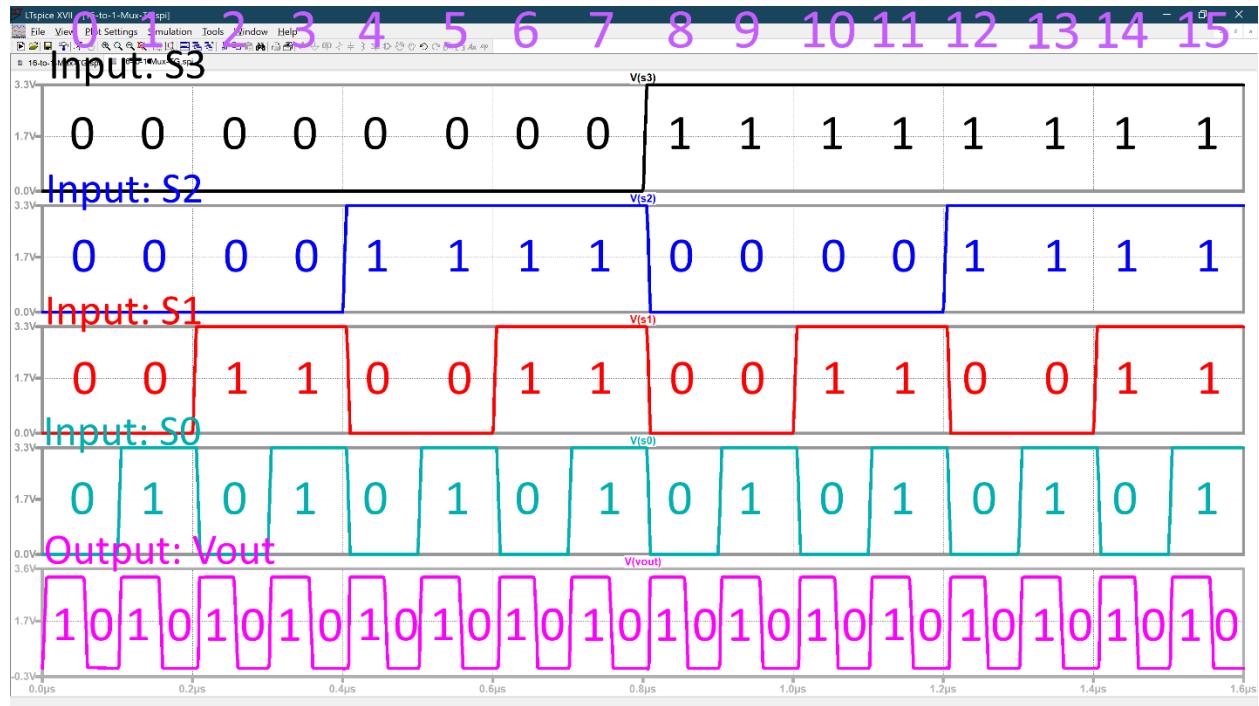


Figure 40: LTSPICE Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Outputs)

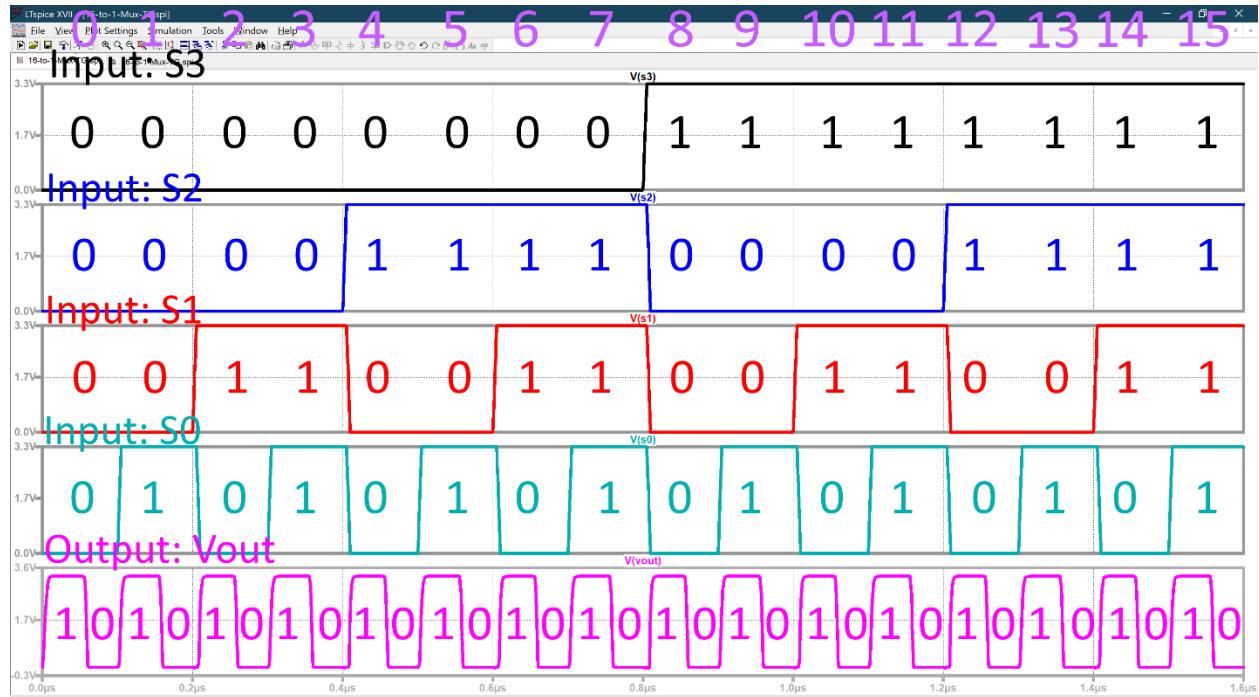


Figure 41: LTSPICE Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Outputs)

Section 7.3: Comparison:

For LTSPICE, by comparing Figure 37 (Conventional Schematic), Figure 38 (Transmission Gate Schematic), Figure 40 (Conventional Layout), and Figure 41 (Transmission Gate Layout) with each other, the way the output reacted given the certain inputs appears to be the same. In addition, with the inputs we gave, it gave us the appropriate outputs that we were looking for, so it confirms that our design is correct. The outputs that we were looking from could be seen by using the truth table on Table 1. The only noticeable difference between the figures would be the propagation delay and the way the waveforms looked, which could be seen on Table 6. For Figure 37, the output almost looks like a perfect square waveform, with similar rise and fall times; it has some parts where it peaks up. For Figure 38, the output waveform appears to have a longer fall time but appear as almost like a perfect square waveform. For Figure 40, the output waveform appears to have a longer rise time and fall time, but still appear as a square waveform (a bit curvier). For Figure 41, the output waveform appears to have a really long rise time and fall time, but still appears as a square waveform (a lot more curvier); this is probably because of the long rise time and fall time, which causes it to not stay high for very long before it has to go back to low. Depending on the which design, each has its own different propagation delay.

In conclusion, LTSPICE shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures were the rise time, fall time, and propagation delay. The differences can be viewed on Table 6, which has a summary of the measurements.

Section 8: Measurement Summary:

The rise time, fall time, and propagation delay of gates of entire I/O are all shown on the table below, Table 6. It's found that for LTSPICE, the Schematic is faster compared to the Layout; the delay times are less, and it's rise and fall time are shorter. It's also found that for the IRSIM, the Schematic is faster compared to the Layout; the delay times are less. Furthermore, Table 7 provides more measurements for each of the designs, such as the transistor sizes, power dissipation, and total chip area. It's found that the transmission gate takes a lot less power and area compared to the conventional CMOS. This is because it uses less transistors compared to the conventional resulting in less power to power the transistors.

Table 6: Summary of Measurements

	Rise Time	Fall Time	Propagation Delay
Conventional LTSPICE Schematic	103.54 ns - 103.42 ns = 0.12 ns	158.92 ns - 158.72 ns = 0.20 ns	$T_{HL} = 1 \text{ ns}$, $T_{LH} = 0.90 \text{ ns}$
Conventional LTSPICE Layout	104.70 ns - 104.20 ns = 0.50 ns	161.37 ns - 160.65 ns = 0.72 ns	$T_{HL} = 1.4 \text{ ns}$ $T_{LH} = 1.5 \text{ ns}$
Conventional IRSIM Schematic	N/A	N/A	Between 0.70ns - 1.55 ns
Conventional IRSIM Layout	N/A	N/A	Between 0.85 ns- 1.60 ns
Transmission Gate LTSPICE Schematic	105.20 ns - 101.20 ns = 4.00 ns	160.00 ns - 150.00 ns = 1.00 ns	$T_{HL} = 0.18 \text{ ns}$ $T_{LH} = 0.20 \text{ ns}$
Transmission Gate LTSPICE Layout	110.00 ns - 101.00 ns = 9.00 ns	160.90 ns - 155.20 ns = 5.70 ns	$T_{HL} = 0.82 \text{ ns}$ $T_{LH} = 0.85 \text{ ns}$
Transmission Gate IRSIM Schematic	N/A	N/A	Between 0.50 ns - 1.20 ns
Transmission Gate IRSIM Layout	N/A	N/A	Between 0.70 ns- 1.45 ns

Table 7: More Measurements

	Conventional Schematic	Conventional Layout	Transmission Gate Schematic	Transmission Gate Layout
Transistor Sizes (W/L)	PMOS (10/2), NMOS (5/2)	PMOS (10/2), NMOS (10/2)	PMOS (10/2), NMOS (5/2)	PMOS (10/2), NMOS (10/2)
Transistor Counts	Inverter = 2 AND = 6 3-AND = $6 + 6 = 12$ OR = 6 4-OR = $6 + 6 + 6 = 18$ $4\text{-to-1} = (4 * 12) + 18 + (2 * 2) = 70$ $16\text{-to-1} = (70 * 5) = 350$ Total = 350	3-AND = 8 4-OR = 10 Inverter = 2 $4\text{-to-1} = (8 * 4) + 10 + (2 * 2) = 46$ $16\text{-to-1} = (46 * 5) = 230$ Total = 230	4-to-1 = 16 $16\text{-to-1} = (16 * 5) = 80$ Total = 80	4-to-1 = 16 $16\text{-to-1} = (16 * 5) = 80$ Total = 80
Total Chip Area	X	17126.1891 μm^2	X	12288.4727 μm^2
Power Dissipation	$3.3 \text{ V} * 0.0032 \text{ A} = 0.01056 \text{ Watts}$	$3.3 \text{ V} * 0.0044 \text{ A} = 0.01452 \text{ Watts}$	$3.3 \text{ V} * 0.0023 \text{ A} = 0.00759 \text{ Watts}$	$3.3 \text{ V} * 0.0029 \text{ A} = 0.00957 \text{ Watts}$

Calculations:Conventional: Size = $1077.5 \lambda \times 519 \lambda = 188562.5 \text{ nm} \times 90825 \text{ nm} = 17126.1891 \mu\text{m}^2$ Transmission Gate: Size = $387.5 \lambda \times 1035.5 \lambda = 67812.5 \text{ nm} \times 181212.5 \text{ nm} =$

$$12288.4727 \mu\text{m}^2$$

Section 9: Conclusion:

In this project, we designed a CMOS of a 16-to-1 Multiplexer by connecting five 4-to-1 Multiplexers together. A conventional 4-to-1 Multiplexer is designed by connecting 4 three input AND gates, 1 four input OR gate, and two inverters together. A transmission gate 4-to-1 Multiplexer is designed by connecting six transmission gates, and two inverters together. By using the Electric software, we created four different designs, a conventional schematic design, a conventional layout design, a transmission gate (TG) schematic design, and a transmission gate (TG) layout design. We also generated waveforms using two different software, IRSIM and LTSPICE. The two different software helped support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the four different design, we compared them and observe their similarities and differences. We observed that for LTSPICE and IRSIM, the input and output reacted the same way given certain inputs for both the Electric Schematic and for the Electric Layout; in addition, it matched the computed values and the goal we were trying to achieve. The only difference between the Electric Schematic and the Electric Layout were the rise time, fall time, and propagation delay. For LTSPICE and IRSIM, these forms of differences can be observed by checking out Table 6, Summary of Measurements. Another thing that we compared were the differences between conventional CMOS and transmission gates. Based off Table 7, it's found that transmission gates take less area and power compared to the conventional CMOS. This is because transmission gates are used to help simplify circuitry and because there's less transistors, there's less power needed to run all those transistors. Therefore, based on our observation and the data that was gathered, we can conclude that there isn't a significant difference in terms of the waveforms; however, there is a difference in the rise time, fall time and propagation delay when zooming in on the waveform. In addition, using transmission gates are more efficient compared to using regular convention CMOS because it saves on the amount of transistors, space, and power.

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