EE 457: Digital Integrated Circuits

Project #1 Report Cover Sheet
Due: 9/23/2019

PROJECT TITLE: CMOS 2-input OR Gate

Student Name: Kevin Chen
(print your name)

Your report should follow the following items in sequence. *Do not change the sequence.* Put a table of content after the cover sheet.	GRADE
Section 1: Executive Summary	/5
Section 2: Background and Approach (Include a truth table)	/5
Section 3: Electric Schematic	/15
Section 4: LTSPICE for Electric schematic	/10
Section 5: IRSIM for Electric schematic	/10
Section 6: Electric Layout	/25
Section 7: LTSPICE for Electric layout (compare with schematic)	/15
Section 8: IRSIM for Electric layout	/10
Section 9: Conclusions and References	/5
TOTAL	**/100**

Note: Do not rearrange this table.

Put your report in a report binder. Do not use ring binders or slide-in paper holders. Appropriate points will be deducted for not following the instructions and incorrectly presenting your work.

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Executive Summary:

In this project, we will be designing a CMOS of a two input OR gate using Electric. By using the Electric software, we'll be creating two different designs, a schematic design and a layout design. In order to test if our designs are correct, we'll be generating waveforms to test for correctness by giving a specific input and expecting a certain output. We'll be generating the waveforms using two different software, IRSIM and LTSPICE. The two different software would help support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the two different design, we'll compare them and observe their similarities and differences.

To design a two input OR gate, we plan to use two different designs and combining them together. One design we plan to use is a two input NOR gate and another design we plan to use is an inverter. By combining the two input NOR gate and an inverter, we'll be able to obtain a two input OR gate. We would also test each individual design using waveforms before putting them together to make sure they satisfy our requirements. By testing each individual design would also help with the debugging process when combining the two designs together because we'll know where the problem lies in case the waveform doesn't turn out like the way expected.

Background and Approach:

A two input OR gate is a form of digital logic gate that is used to produce a desired output given certain inputs. It could also be seen in terms of a Boolean expression, such as F = A + B. The two input OR gate would compare the two inputs and would output '1' when any of the two inputs are '1'; otherwise, it's '0'. It's mainly used in circuit designs where signals are being manipulated through logic gates.

The truth table of a two input OR gate is shown in Table 1.

Table 1: Truth Table of a Two Input OR Gate

Input: A	Input: B	Output: A OR B
0	0	0
0	1	1
1	0	1
1	1	1

The approach we plan to take to design the two input OR gate would be to use two different designs and combining them together. The two designs that we plan to use would be a two input NOR gate and an inverter. The reason for this approach is because we can't directly build a CMOS two input OR gate, and we'll have to use a two input NOR gate and an inverter. By applying an inverter on the two input NOR gate, we'll get the inverse of a two input NOR gate, resulting in a two input OR gate.

The figures below show the schematic and layout of the two input NOR gate and an inverter that we plan to use for this project.

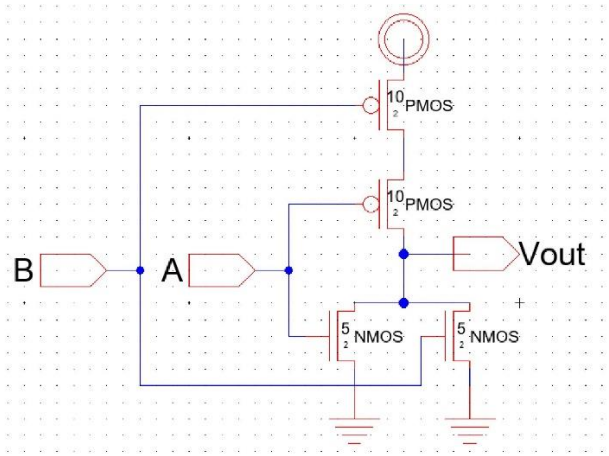

Figure 1: Schematic Design of a Two Input NOR Gate

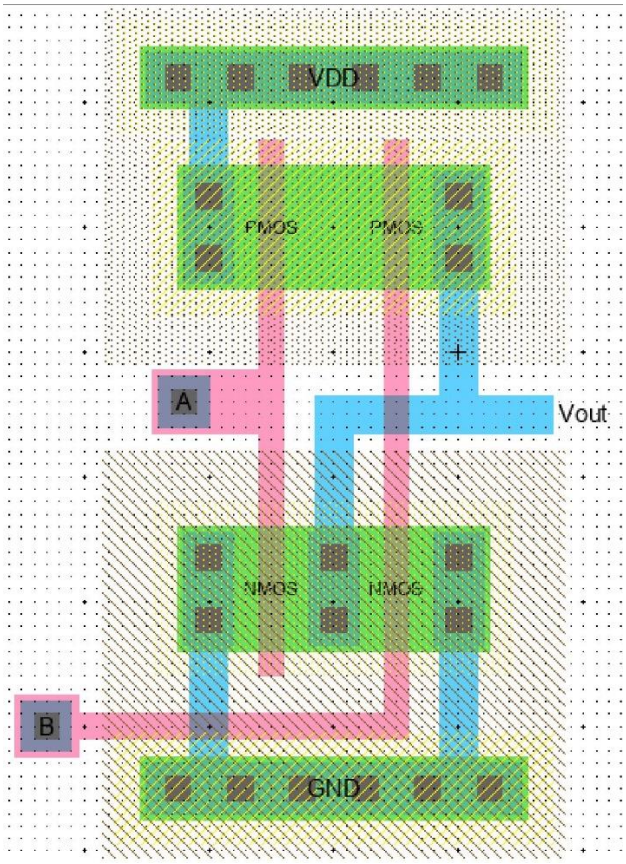

Figure 2: Layout Design of a Two Input NOR Gate

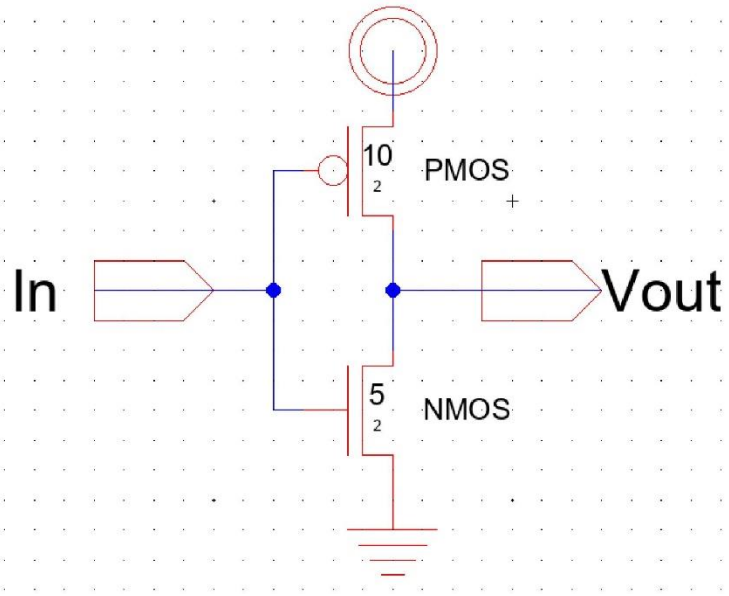

Figure 3: Schematic Design of an Inverter

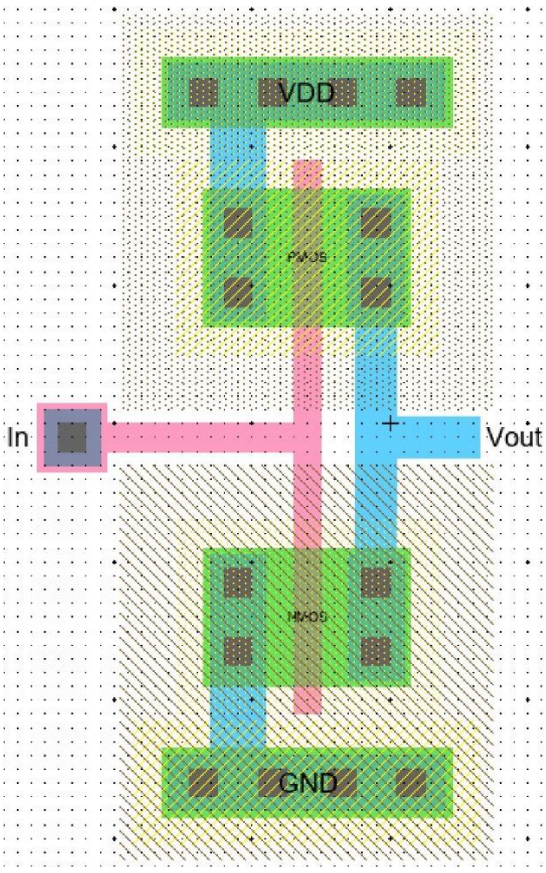

Figure 4: Layout Design of an Inverter

Electric Schematic:

We created a schematic of the two input OR gate by combining a two input NOR gate (Figure 1) with an inverter (Figure 3). It was combined by connecting the output of the two input NOR gate to the input of the inverter. Figure 5 shows the schematic design that was built using Electric of the two input OR gate. Figure 6 shows the Design Rule Check (DRC) that was performed on the schematic; it indicates that there were no errors or warning with the schematic.

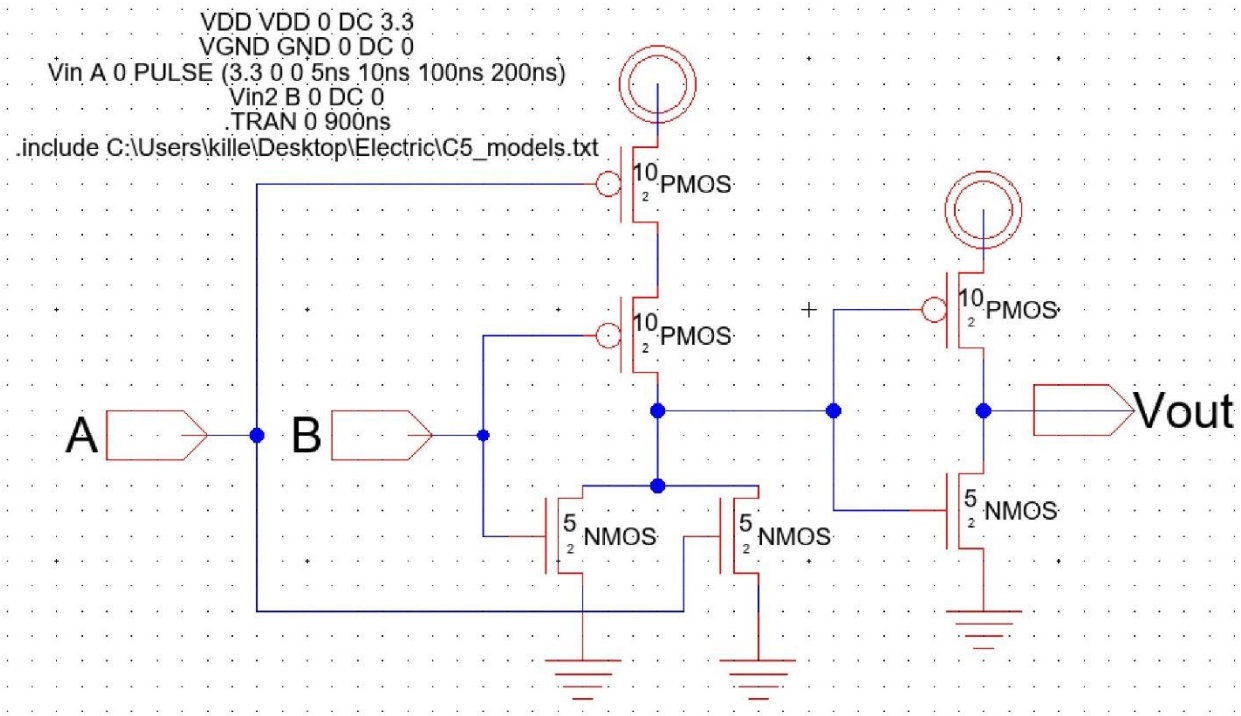

Figure 5: Schematic Design of a Two Input OR Gate

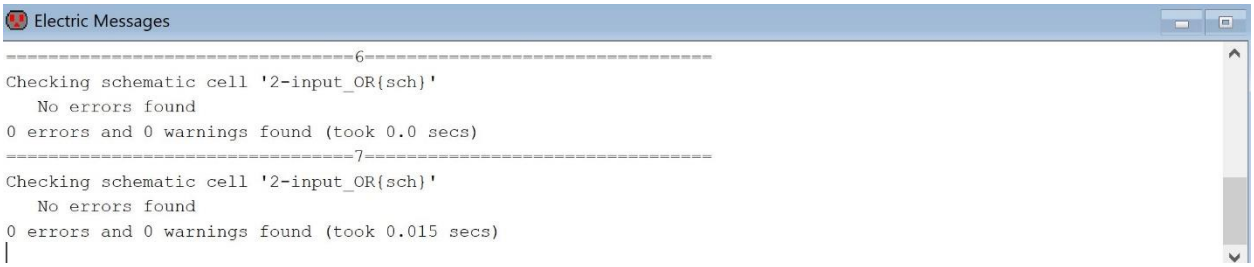

Figure 6: Design Rule Check (DRC) of a Two Input OR Gate Schematic Design

LTSPICE for Electric Schematic:

After creating the schematic design of the two input OR gate, waveforms were created using LTSPICE. The waveforms were created by using Spice Code to initialize our VDD, GND, and our two inputs, A and B. It was also used to produce the type of analysis we want; in this case, we used a transient analysis, which goes as far as 900ns.

We ran a total of two different Spice Codes for the schematic design of the two input OR gate. The difference between the two different Spice Codes was how we initialized our input, B. The first Spice Code, B was set to a constant of 0, which indicates that B wasn't outputting any voltage. The second Spice Code, B was set to have a pulse, which was coded so it could check all possible inputs between A and B to confirm that the two input OR gate satisfied our requirements.

The similarities between the two different Spice Codes are how we initialized our VDD, GND, and our input, A. We set VDD to have a constant volt of 3.3 volts. We set our GND to have a constant volt of 0 volts. We set our input, A to have a pulse so it's able to show how the output changes depending on the input. The pulse of A was initialized by using the pulse function, which has 7 parameters. Pulse is defined as Pulse (V1(Initial Value) V2(Pulsed Value) TD (Delay Time) TR (Rise Time) TF (Fall Time) PW (Pulse Width) PER (Period)). We set our pulse to have an initial value of 3.3 volts, pulsed value of 0 volts, delay time of 0 seconds, rise time of 5 nanoseconds, fall time of 10 nanoseconds, pulse width of 100 nanoseconds, and period of 200 nanoseconds, which is equivalent to 5 MHz.

Table 2 shows the data for the waveforms. Figure 7 shows the LTSPICE waveform for the two input OR gate, setting B to zero. Figure 8 shows the LTSPICE waveform for the two input OR gate, testing all possible inputs; there's a drop in the output due to the fall time from A becoming

0 volts and the rise time of B become 3.3 volts. The propagation delay for figure 7 was approximately 0.7 ns. The propagation delay for figure 8 is approximately 0.6 ns.

Table 2: Spice Code Configurations and Data Analysis for Electric Schematic

	Figure 7	**Figure 8**
VDD	3.3 Volts	3.3 Volts
GND	0 Volts	0 Volts
A	Pulse: Initial Value = 3.3 volts Pulsed Value = 0 volts Delay Time = 0 seconds Rise Time = 5 nanoseconds Fall Time = 10 nanoseconds Pulse Width = 100 nanoseconds Period = 200 nanoseconds = 5 MHz.	Pulse: Initial Value = 3.3 volts Pulsed Value = 0 volts Delay Time = 0 seconds Rise Time = 5 nanoseconds Fall Time = 10 nanoseconds Pulse Width = 100 nanoseconds Period = 200 nanoseconds = 5 MHz.
B	0 Volts	Pulse: Initial Value = 3.3 volts Pulsed Value = 0 volts Delay Time = 0 seconds Rise Time = 5 nanoseconds Fall Time = 10 nanoseconds Pulse Width = 400 nanoseconds Period = 800 nanoseconds = 1.25 MHz.
Vout	Rise Time: 0.80 ns Fall Time: 0.45 ns Propagation Delay: 0.7 ns	Rise Time: 0.55 ns Fall Time: 0.55 ns Propagation Delay: 0.6 ns

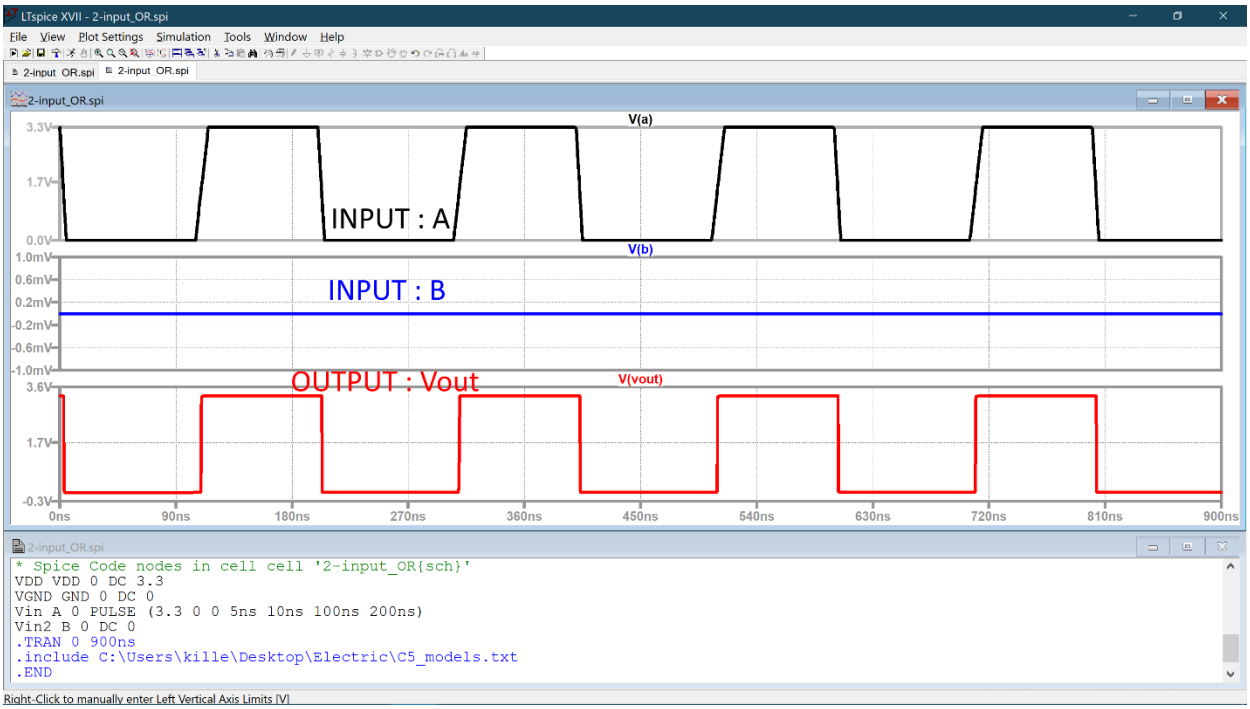

Figure 7: LTSPICE Waveforms of Schematic Design of a Two Input OR Gate (Setting B to Zero)

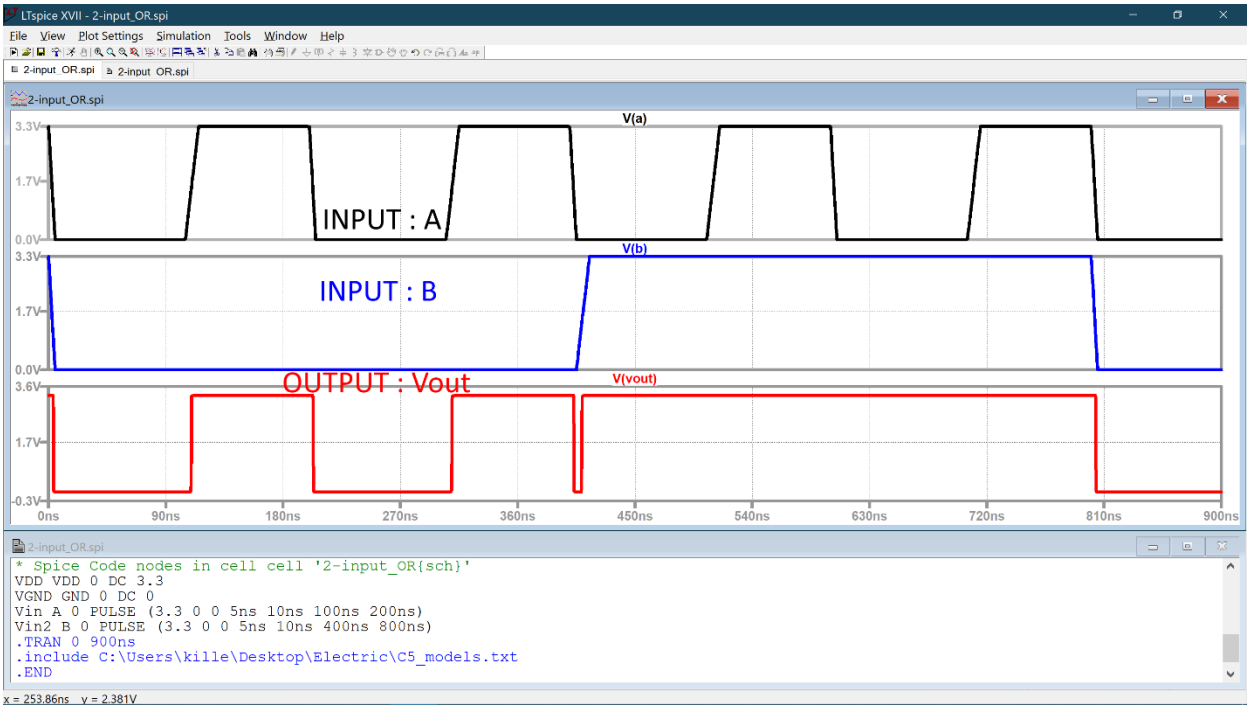

Figure 8: LTSPICE Waveforms of Schematic Design of a Two Input OR Gate (Testing All Possible Inputs)

IRSIM for Electric Schematic:

After creating the schematic design of the two input OR gate, waveforms were created using IRSIM. Theses waveforms were created by giving the inputs, A and B certain values at certain times. The input values we gave A and B was configured so it could test all possible combinations, allowing us to analysis how the output would react towards this approach. When setting in values for the inputs, the output would automatically update based on the inputs. We were able to verify that the waveforms obtained from IRSIM matches those of the truth table (Table 1). The propagation delay that appears on IRSIM is approximately 0.138 ns.

Table 3 shows the data for the waveforms. Figure 9 shows the IRSIM waveforms for the two input OR gate.

Table 3: IRSIM Configurations and Data Analysis for Electric Schematic

	0s	2ns	4ns	6ns	8ns
Input: A	0	1	0	1	0
Input: B	0	0	1	1	0
Output: Vout	0	1	1	1	0

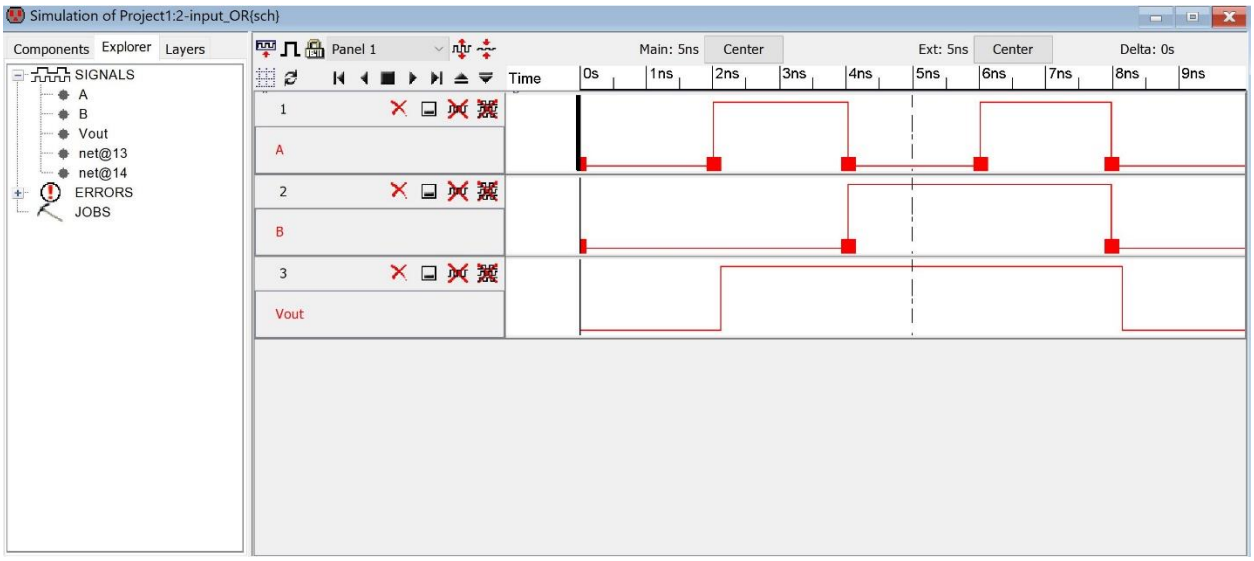

Figure 9: IRSIM Waveforms of Schematic Design of a Two Input OR Gate (Testing All Possible Inputs)

Electric Layout:

We created a layout of the two input OR gate by combining a two input NOR gate (Figure 2) with an inverter (Figure 4). It was combined by connecting the output of the two input NOR gate to the input of the inverter.

Figure 10 shows the layout design that was built using Electric of the two input OR gate. Figure 11 shows the Design Rule Check (DRC) and Well Check that was performed on the layout; it indicates that there were no errors or warning with the layout.

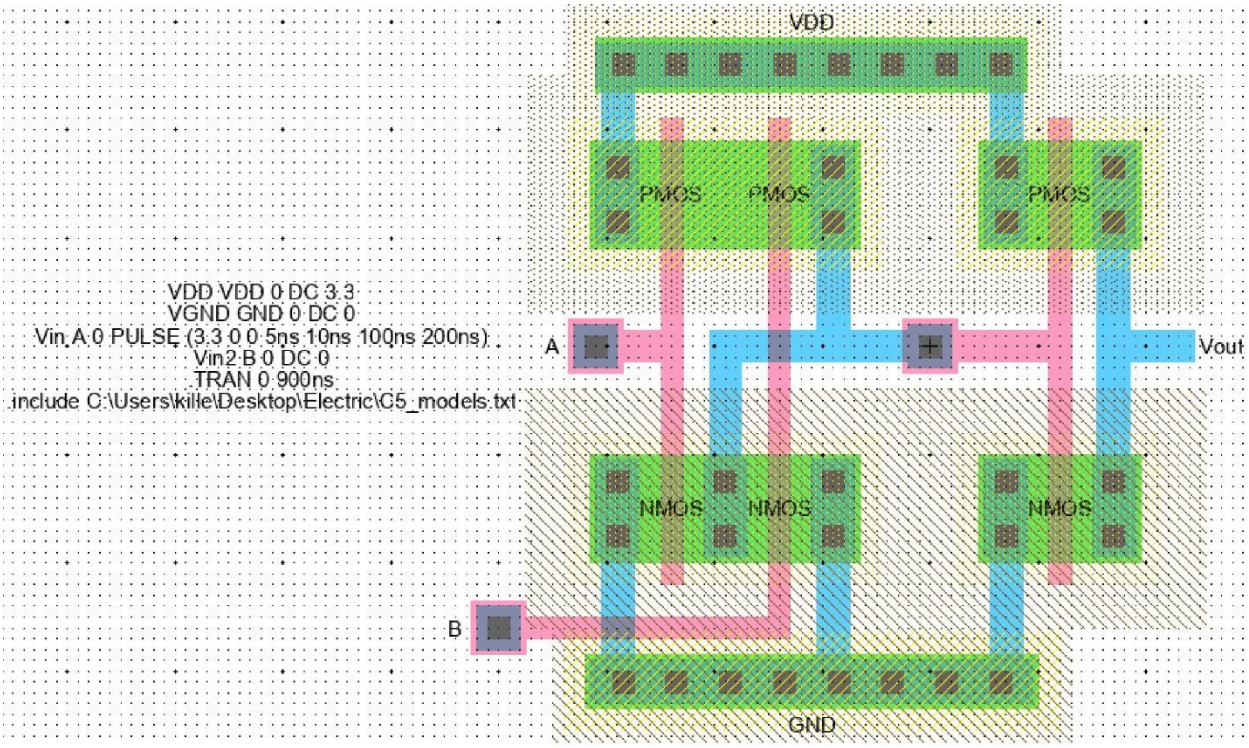

Figure 10: Layout Design of a Two Input OR Gate

Figure 11: Design Rule Check (DRC) and Well Check of a Two Input OR Gate Layout Design

LTSPICE for Electric Layout:

After creating the layout design of the two input OR gate, waveforms were created using LTSPICE. The Spice Code that was used for figure 12 and figure 13 is the same Spice Code that was used for the schematic design of the two input OR gate, refer to table 2 if needed.

Table 4 shows the data for the waveforms. Figure 12 shows the LTSPICE waveform for the two input OR gate, setting B to zero. Figure 13 shows the LTSPICE waveform for the two input OR gate, testing all possible inputs; there's a drop in the output due to the fall time from A becoming 0 volts and the rise time of B become 3.3 volts. The propagation delay for Figure 12 was approximately 0.9 ns. The propagation delay for Figure 13 is approximately 0.9 ns.

Table 4: Spice Code Configurations and Data Analysis for Electric Layout

	Figure 12	**Figure 13**
VDD	3.3 Volts	3.3 Volts
GND	0 Volts	0 Volts
A	Pulse: Initial Value = 3.3 volts Pulsed Value = 0 volts Delay Time = 0 seconds Rise Time = 5 nanoseconds Fall Time = 10 nanoseconds Pulse Width = 100 nanoseconds Period = 200 nanoseconds = 5 MHz.	Pulse: Initial Value = 3.3 volts Pulsed Value = 0 volts Delay Time = 0 seconds Rise Time = 5 nanoseconds Fall Time = 10 nanoseconds Pulse Width = 100 nanoseconds Period = 200 nanoseconds = 5 MHz.
B	0 Volts	Pulse: Initial Value = 3.3 volts Pulsed Value = 0 volts Delay Time = 0 seconds Rise Time = 5 nanoseconds Fall Time = 10 nanoseconds Pulse Width = 400 nanoseconds Period = 800 nanoseconds = 1.25 MHz.
Vout	Rise Time: 0.70 ns Fall Time: 0.49 ns Propagation Delay: 0.9 ns	Rise Time: 0.60 ns Fall Time: 0.54 ns Propagation Delay: 0.9 ns

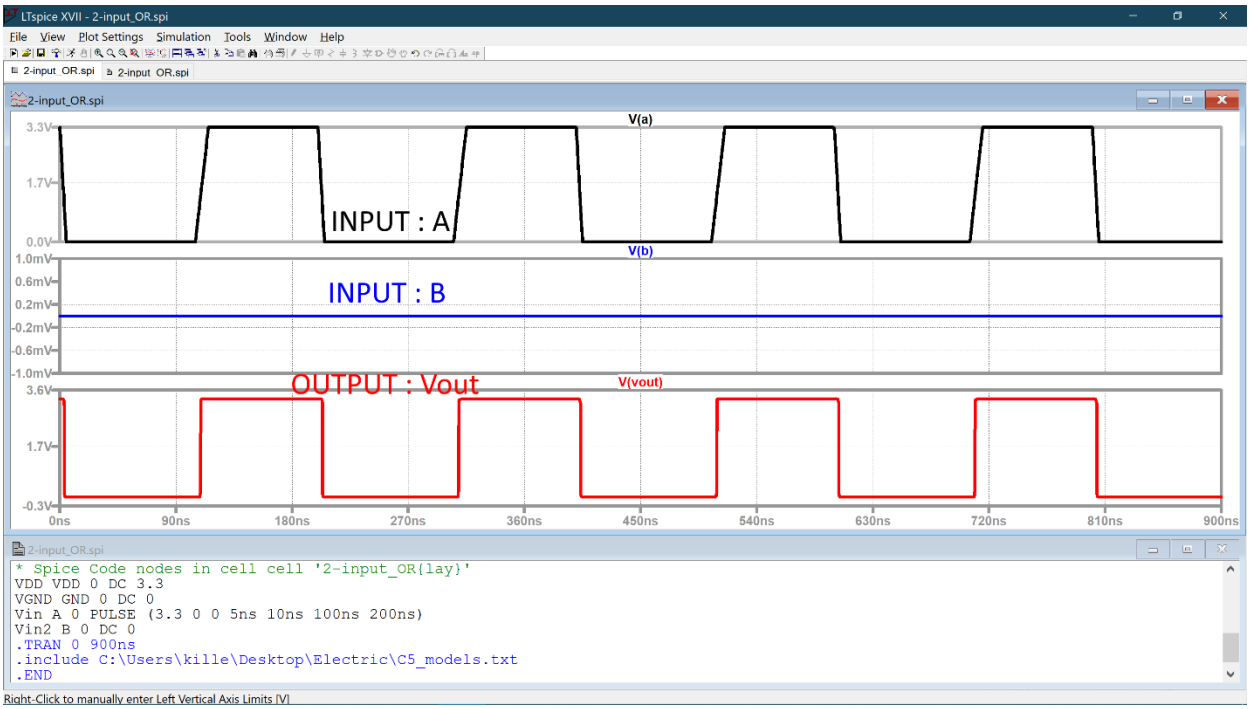

Figure 12: LTSPICE Waveforms of Layout Design of a Two Input OR Gate (Setting B to Zero)

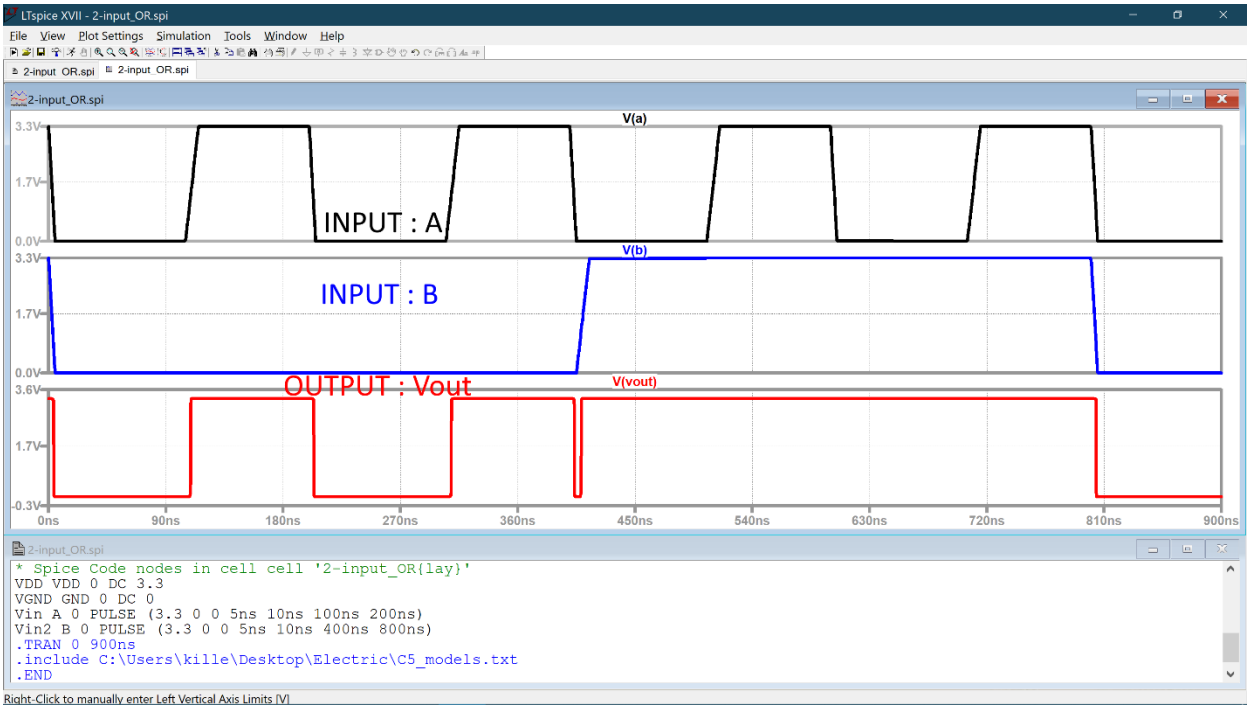

Figure 13: LTSPICE Waveforms of Layout Design of a Two Input OR Gate (Testing All Possible Inputs)

Comparison Between LTSPICE for Electric Schematic and for Electric Layout

By comparing Figure 7 (Electric Schematic) with Figure 12 (Electric Layout), the way the input and output reacted given the Spice Code appears to be the same. Whenever the input, A, is set to high (3.3 volts), the output, Vout, is also set to high (3.3 volts). Since the input, B, is constant and set to 0, it wouldn't affect the output in anyway. The only noticeable difference between the two figures would be the rise time, fall time, and propagation delay.

By comparing Figure 8 (Electric Schematic) with Figure 13 (Electric Layout), the way the input and output reacted given the Spice Code appears to be the same. Whenever the inputs, A or B, is set to high (3.3 volts), the output, Vout, is also set to high (3.3 volts). The only noticeable difference between the two figures would be the rise time, fall time, and propagation delay.

In conclusion, LTSPICE shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures were the rise time, fall time and propagation delay. The difference can be viewed by comparing Table 2 and Table 4.

IRSIM for Electric Layout:

After creating the layout design of the two input OR gate, waveforms were created using IRSIM. Theses waveforms were created by giving the inputs, A and B certain values at certain times. The input values we gave A and B was configured so it could test all possible combinations, allowing us to analysis how the output would react towards this approach. When setting in values for the inputs, the output would automatically update based on the inputs. We were able to verify that the waveforms obtained from IRSIM matches those of the truth table (Table 1). The propagation delay that appears on IRSIM is approximately 0.17 ns.

Table 5 shows the data for the waveforms. Figure 14 shows the IRSIM waveforms for the two input OR gate.

Table 5: IRSIM Configurations and Data Analysis for Electric Layout

	0s	2ns	4ns	6ns	8ns
Input: A	0	1	0	1	0
Input: B	0	0	1	1	0
Output: Vout	0	1	1	1	0

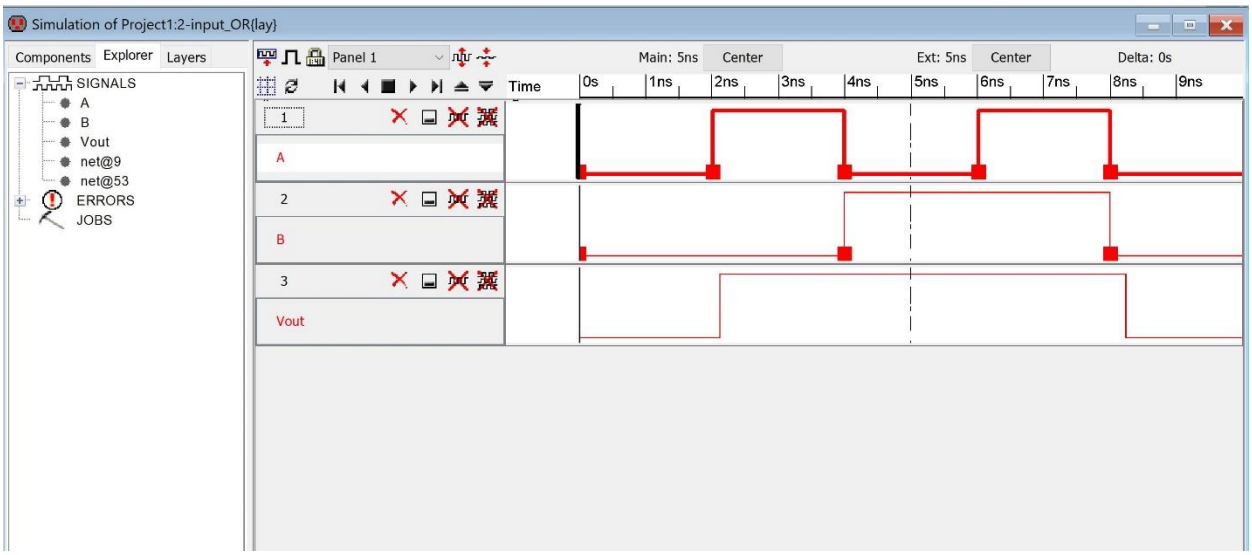

Figure 14: IRSIM Waveforms of Layout Design of a Two Input OR Gate (Testing All Possible Inputs)

Comparison Between IRSIM for Electric Schematic and for Electric Layout

By comparing Figure 9 (Electric Schematic) with Figure 14 (Electric Layout), the way the input and output reacted given the certain inputs appears to be the same. Whenever the inputs, A or B, is set to high, the output, Vout, is also set to high. This could also be seen on Table 3 (Electric Schematic) and Table 5 (Electric Layout). The only noticeable difference between the two figures would be the propagation delay. Figure 9 has a propagation delay of approximately 0.138 ns, while Figure 14 has a propagation delay of approximately 0.17 ns.

In conclusion, IRSIM shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures was the propagation delay. It's shown that the Electric Schematic has a shorter propagation delay compared to the Electric Layout.

Conclusion:

In this project, we designed a CMOS of a two input OR gate by connecting a two input NOR gate and an inverter. By using the Electric software, we created two different designs, a schematic design and a layout design. We also generated waveforms using two different software, IRSIM and LTSPICE. The two different software helped support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the two different design, we compared them and observe their similarities and differences. We observed that for LTSPICE and IRSIM, the input and output reacted the same way given certain inputs for both the Electric Schematic and for the Electric Layout; in addition, it matched the truth table and the goal we were trying to achieve. The only difference between the Electric Schematic and the Electric Layout were the rise time, fall time, and propagation delay. For LTSPICE, these forms of differences can be observed by comparing Table 2 and Table 4. For IRSIM, Electric Schematic had a propagation delay of approximately 0.138 ns in Figure 9 compared to the Electric Layout, which had a propagation delay of approximately 0.17 ns in Figure 14. Therefore, based on our observation and the data that was gathered, we can conclude that there isn't a significant difference in terms of the waveforms; however, there is a difference in the rise time, fall time and propagation delay when zooming in on the waveform.

References:

[1] *The CMOS Inverter Explained* [Online] Available:

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