**EE 457**

**Project #1**

***Due 9/23/19***

# Design a CMOS 2-input OR gate using Electric to realize Boolean function F=A+B.

# Provide the following:

1. Circuit schematic in Electric (snapshots)
2. Layout in Electric.(snapshots)
3. DRC and Well Check snapshots
4. Generated SPICE code snapshot. Use the A input with pulsed input that has period (T) of 5MHz digital pulse and it has 5ns rise and 10ns fall times. The initial delay is zero.
5. Print the output waveform of SPICE using the pulsed “A” input.

Note:

1. Do not hand draw schematics. Use only Electric.
2. All tables must be labeled and captioned on top of the table (e.g., Table 1: Data from the Schematic.)
3. All Figures must be labeled and captioned below the figure (e.g., Figure 1: Illustration of the Inverter Schematic.)
4. All grammar should be written professionally.

**Do the following:**

1. Watch appropriate Electric Tutorials. Make sure you have watched Tutorials #1, #2, #3 and #4 before starting this project.
2. Perform design rule checks to see if you violated any design rules (DRC).
3. Put text on inputs, output, VDD and VSS.
4. Make sure you provide a truth table.

**What to turn-in: (violations will result in minus 2 points for each violation)**

1. A typed report that has the following:
   1. Cover page (print the attached cover page). Type your name. Do not hand write your name.
   2. Executive Summary: Summarize your project in about 1/2 –page format.
   3. Background: Provide some background and motivations, what your design does, etc.
   4. Approach: Put theory of the operation and others. What will you do to accomplish the work? How will you approach this project? Etc.
   5. Layout Details: Put layout of the CMOS gate from Electric. Use snapahots and put cropped screen in MSWord. Use the print command and put grid on the paper.
   6. Simulate your designed circuit using LTSPICE. Provide output rise and fall times. Measure output delay from the input and compare the two.
   7. Run IRSIM and verify your design with the truth table for both.
   8. Conclusions: Put what you observed and what you did. Provide some measurement data to conclude your work.
   9. **VERY IMPORTANT**: Label all your waveforms clearly using MS Word on LTSpice and IRSIM. Appropriate points will be deducted for not identifying and unclear representation of waveforms.

EE 457: Digital Integrated Circuits

Project #1 Report Cover Sheet

Due: 9/23/2019

## **PROJECT TITLE:\_\_CMOS 2-input OR Gate\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

Student Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

(print your name)

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| Your report should follow the following items in sequence.  *Do not change the sequence.*  Put a table of content after the cover sheet. | GRADE |
| Section 1: Executive Summary | /5 |
| Section 2: Background and Approach (Include a truth table) | /5 |
| Section 3: Electric Schematic | /15 |
| Section 4: LTSPICE for Electric schematic | /10 |
| Section 5: IRSIM for Electric schematic | /10 |
| Section 6: Electric Layout | /25 |
| Section 7: LTSPICE for Electric layout (compare with schematic) | /15 |
| Section 8: IRSIM for Electric layout | /10 |
| Section 9: Conclusions and References | /5 |
| TOTAL | **/100** |

Note: Do not rearrange this table.

Put your report in a report binder. Do not use ring binders or slide-in paper holders. Appropriate points will be deducted for not following the instructions and incorrectly presenting your work.