***ECE457 Digital IC Design***

***Project #2***

***Choose only one Project from (A), (B) or (C).***

**Due on 10/21/2019 in class**

**WARNING: This project is estimated to take over 30 hours. Please plan accordingly. I hope you enjoy it.**

Note: ALL reporting work must be done in MS Word. Please pay special attention to presenting your work in Electric layouts. Please make your layout print large so I can see it. Please put figure numbers, table numbers and refer them in your text rather than just have them in your report. All projects have supply voltage of 3.3V. It is necessary to show all DRC and well checks for error free design.

**Choose from one of the following Projects:**

*Note: The links shown below are only my suggestions. I do not take any responsibilities from your understandings from them nor their contents.*

1. Design of high performance 2’s complement 16-bit adder circuit using ripple carry adder. (see <https://www.youtube.com/watch?v=koZbKyUikYw> )
2. Design of high performance 2’s complement 8-bit adder circuit using carry Look Ahead Adders. (See [www.ece.lsu.edu/ee3755/2013f/cla.pdf](http://www.ece.lsu.edu/ee3755/2013f/cla.pdf) and <https://www.youtube.com/watch?v=-LVxHFUtZHQ>)
3. Design 8-bit by 8-bit multiplier.

**For Project (A):**

In ***ripple*** ***carry adders (RCA)***, 16 bits are added one bit at a time. This provides a very slow addition process. Study the ripple carry adder carefully first to appreciate the objectives.

1. Draw a logic schematic of the 8-bit RCA in Electric and simulate it in LTSpice.
2. Draw stick diagrams and Euler’s paths where appropriate to design.
3. Perform the Electric Layout with IRSIM.
4. Verify your design by adding the following numbers: (1) -32+107=75, (2) -28+16= -12 and (3) 52378+589 = 52,967 (4) –71+(-10000) = -10,071 to verify. You must provide the 4 additions for verifications.
5. Provide details of LTSPICE measurements on rise time, fall time and propagation delays.

**For Project (B):**

In ***carry look ahead adders***, the carry propagation time is much less than RCA. Therefore, the addition process is very fast. As you get more familiar with CLA concept you will understand why we need it for faster adder hardware. Study the ripple carry adder first to appreciate the objectives.

1. Draw a logic schematic of the 8-bit CLA in Electric and simulate it in LTSpice.
2. Draw stick diagrams and Euler’s paths where appropriate to design.
3. Perform the Electric Layout with IRSIM.
4. Verify your design by adding the following numbers: (1) -32+107=75, (2) -28+16= -12 and (3) 33+70= 103 (4) –71+(-10) = -81 to verify. You must provide the 4 additions for verifications.
5. Provide details of LTSPICE measurements on rise time, fall time and propagation delays.

**For Project (C):**

Design 8-bit multiplier. Show minimum of 5 multiplications to show proper operations of your design. You may use transmission gates, static or dynamic CMOS design.

**What to turn-in: You will be graded for points in the table of the cover sheet.**

1. Follow the Grading cover page for sequence of your sections. Do not reorder them.
2. A typed report that has the following:
   1. Cover page (print the attached cover page)
   2. Executive Summary: Summarize your project in 1/2 –page format.
   3. Introduction: Provide some background and motivations
   4. Approach and calculations: Put schematics and details of the design. Put detailed calculations of all parameters. Put theory of the operation and others. Use schematic or drawing tools to draw schematic.
   5. LTSPICE Simulations: Put the output of the circuit in peace by peace as you need to analyze. Put input and output waveforms on the same panel. Make the waveforms clearly and label them.
   6. IRSIM of the layout. Verify all numbers that I asked.
   7. Perform waveform measurements for rise/fall times and periods
   8. Conclusion: Put what you observed and what you did.
   9. **References**: put any papers that are relevant to this project by using the IEEE format. The IEEE format is only for the reference section.
3. Calculate the following parameters:
   1. Calculate transistor sizes (W/L) and delays.
   2. Power dissipation of the device. You can do this by going to the LTSPICE and find out how much the chip is drawing current while operating.
   3. Compute the total chip area. Do not simply give me lambda by lambda. I need you to give me in micrometer by micrometer, i.e., micrometer squired.
4. Put your report in a flat report binder.



EE457: Digital IC Design

Fall Semester 2019

Project #2 Report Cover Sheet

Due 10/21/2019

## **\*PROJECT TITLE:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

\*Student Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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| Sections | GRADE Points |
| 1. Executive Summary | /5 |
| 1. Introduction | /5 |
| 1. Electric Circuit Schematic | /10 |
| 1. LTSpice simulations of Schematic (label waveforms) | /10 |
| 1. IRSIM simulations of Schematic (label waveforms) | /10 |
| 1. Electric Layout | /25 |
| 1. LTSpice simulation of Layout | /10 |
| 1. IRSIM Simulations of layout | /10 |
| 1. Summary of Measurements in 2. Propagation delays of gates and entire I/O, 3. Total Chip area in um2 | /3  /2 |
| 1. Comparisons of Schematic & Layout | /5 |
| 1. Conclusion | /5 |
| TOTAL | **/100** |

\*Do not hand-write.