EE 444

Embedded Systems Design

Lab 0: *MSP430: Digital I/O*

*1/31/2017*

**Chic J O’Dell**

Does your solution work the way it’s supposed to work? □YES □NO1

1If your answer is NO, please explain in your report.

Instructor/TA comments and grading

# Objective and Background

The main goal of this laboratory is to get familiar with the Texas Instruments MSP-EXP430F5438a experimenter’s board, CrossStudio programming environment from Rowley, and the process of downloading, executing, and debugging programs on MSP430-based boards. In addition, the Digital I/O and timer capabilities of MSP430 will be explored.

# Equipment

* CrossStudio for MSP430
* TI MSP-EXP430F5438A board
* Agilent mixed-signal oscilloscope

# Procedure

## Part 1

In order to output a 4 MHz clock signal generated using MCLK the code seen in Figure 1. The first step in constructing the code to accomplish this is setting the appropriate MCLK registers “UCSCTLx” 0 through 9. After consulting the “MSP430x5xx\_x6xx user guide” it became obvious that only UCSCTL2 and UCSCTL4 need be modified for this output.

UCSCTL2, as seen in Figure 5 is set to 121. This might seem like sloppy code as it overwrites the entire register and the tries to overwrite reserved bits but it is valid because I chose to do so on purpose for the sake of simplicity. Setting UCSCTL2=121 has no adverse effects as it does not change any of the default register values outside of the FLLN field. Setting the FLLN field in the UCSCTL2 register controls the multiplier bits of the DCO. Setting the FLLN=121 gives results in a DCOCLK = FLLN\*MCLK=122\*32\*1024= 3994696 Hz.

UCSCTL4, definition seen in Figure 6 is programed with more care. Using the bit mask “UCSCTL4 |= SELS\_\_DCOCLK + SELM\_\_XT1CLK” sets the input to MCLK to be DCOCLOK and MCLK source select to use XT1CLK instead of the default VLOinput.

## Part 2

We can again easily use the timer to generate a square wave signal with a period of approximately 100 us and 50% positive duty cycle with the output on a general I/O pin. Given time=1/frequency we know that a clock frequency of 1 MHz will provide the correct 100 us pulse time and 50% duty cycle. Again, checking through the control registers we find that we need to set UCSCTL4.

Bit masking “UCSCTL4 |= SELM\_\_DCOCLK;” sets the DCOCLK to MCLK which will now have the crystal frequency of 32768 Hz.

# Results

## Part 1

After the UCSCTL2 and UCSCTL4 registers have been set the signal needs to be routed to test pins in order to capture the wave form on the scope. The TI breakout board provides just such clock test pins found from the breakout board schematic, snippet seen in Figure 7. Setting up the pins to show the MCLK output as “P11DIR |= BIT1;” and “P11SEL |= BIT1;” produced the scope plot as seen in Figure 6.

## Part 2

Using a for loop as a crude delay function the pulse was experimentally tuned by adding loop iterations or taking them away. In order to achieve the desired, pule time of 100 us 40 iterations of the for loop was sufficiently close as seen in the scope capture Figure 4 output on P5.0.

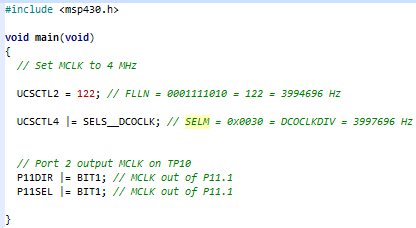


Figure : Software for Part1.

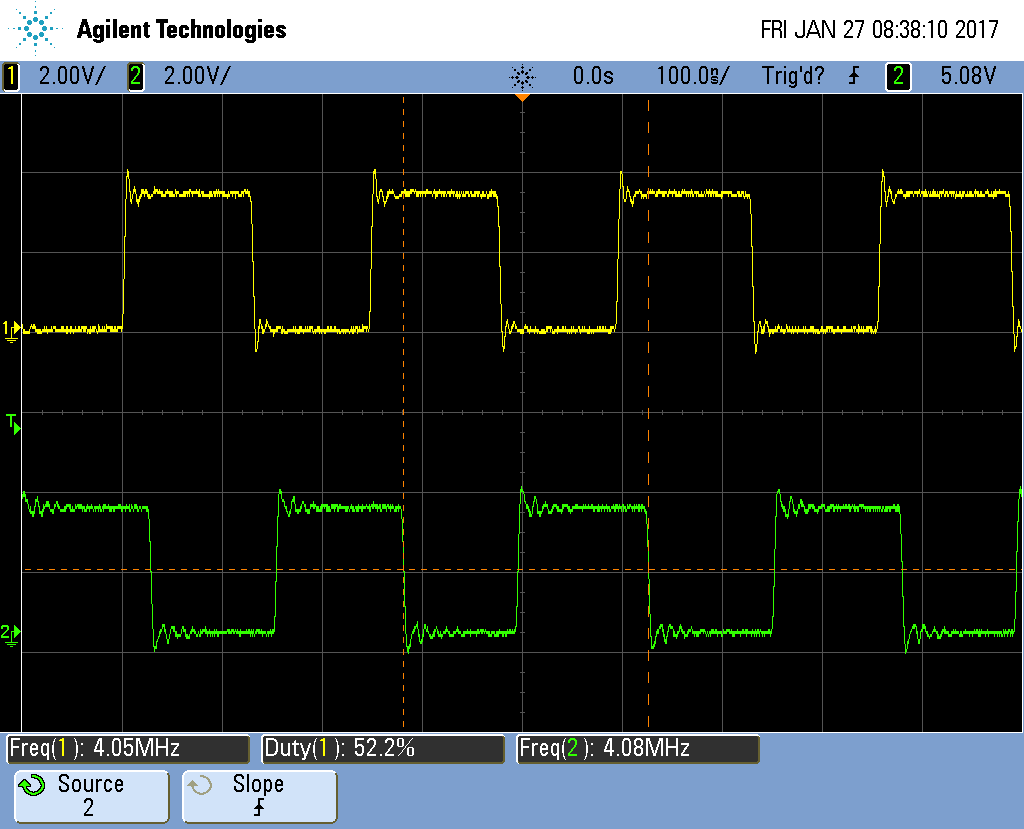


Figure : 4 GHZ MCLK output in yellow.

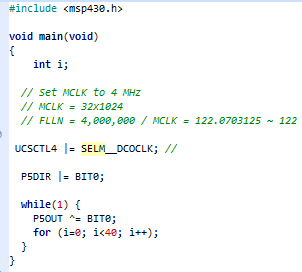


Figure : Software Part 2

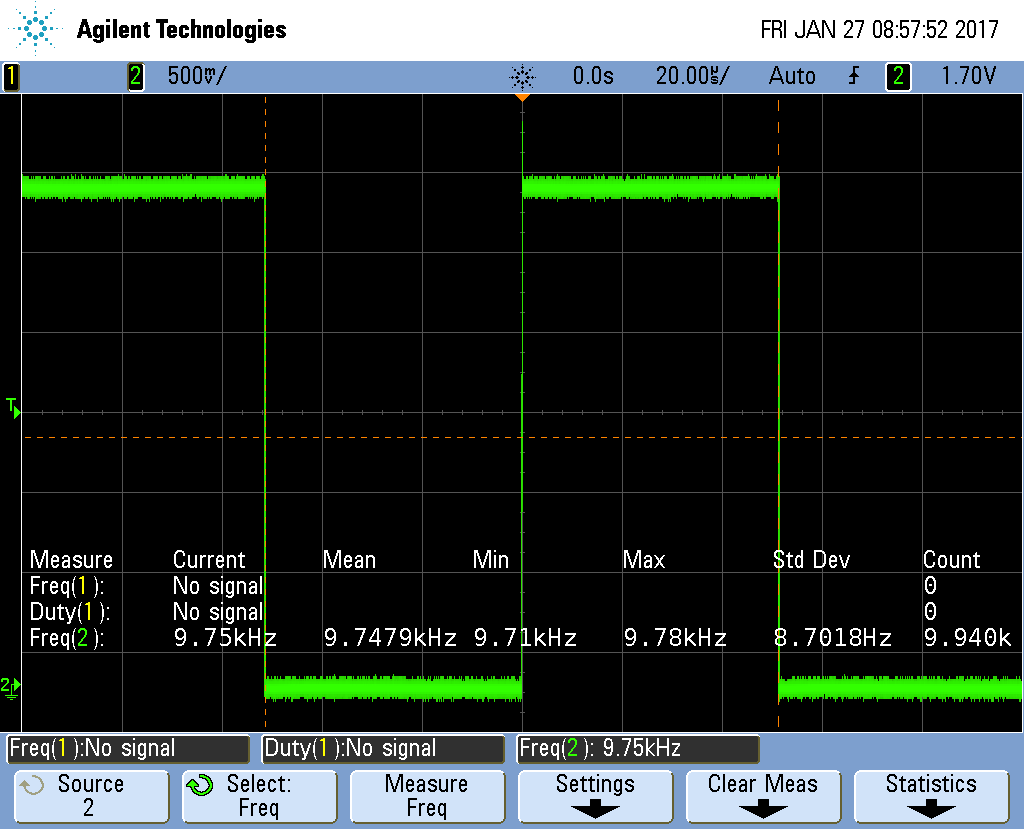


Figure : 1 MHz MCLK output in Green 100 us 50% duty cycle. .

Both parts of the labs went pretty well. The most challenging part of both labs was sifting through the associated data sheets to find relevant information. I think I could have improved the second part of the lab by using a divider and a timer interrupt instead of the for loop to generate the 100 us clock pulse. A non-poling coding method would be a lot more efficient.

# Conclusion

The wide utility of the timer is evident after reading through the control registers. With the many different timer channels provide the ability to accomplish many different uses given one main clock frequency. In fact the MSP430 provides such clock customization you could “bit bang” simply using timerA.

# 7. Attachments

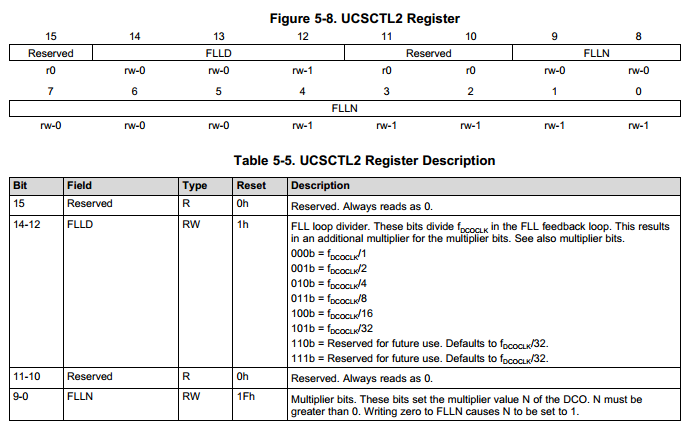
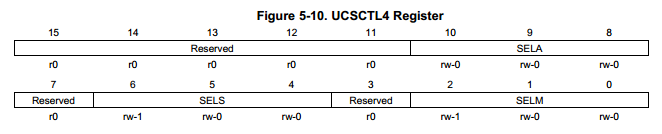


Figure : UCSCTL2 register description.



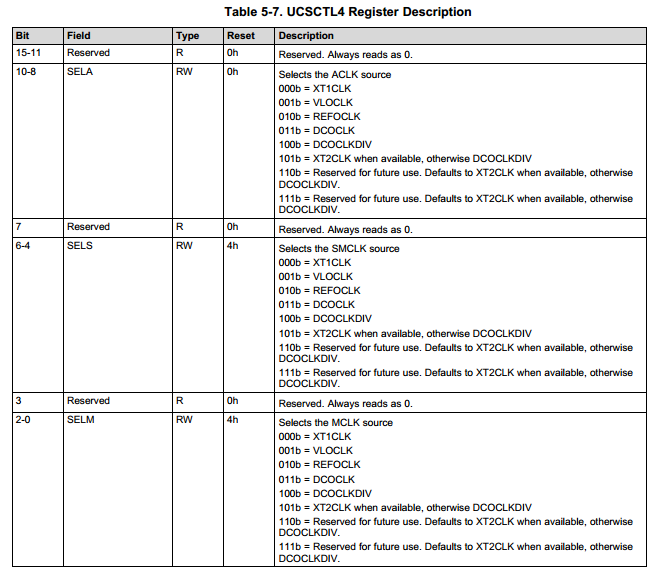


Figure : UCSCT4 register description.

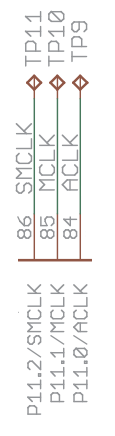


Figure :MCLK test pin on MSP430 breakout board.

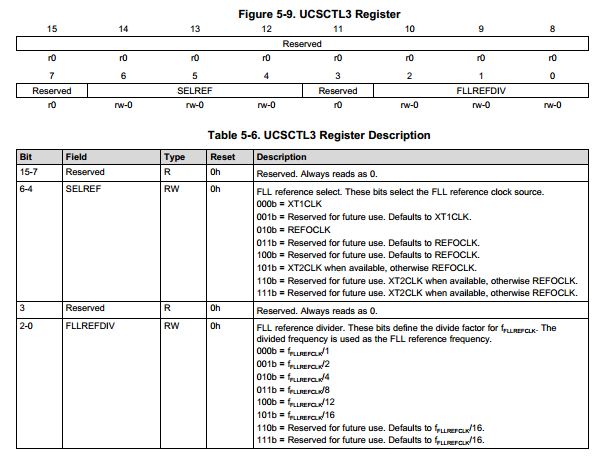


Figure : UCSCTL3 Register.