EE 444

Timer A output modes

Lab 2: *MSP430: Digital I/O*

*2/14/2017*

**Chic J O’Dell**

Does your solution work the way it’s supposed to work? □YES □NO1

1If your answer is NO, please explain in your report.

Instructor/TA comments and grading

# Objective and Background

Using Timer A in order to output a PWM pulse with a variable duty cycle (75 and 25 %) for a signal of . In order to achieve high precision both SMCLK and MCLK are set to 25 MHz, SMCLK to be used as the source for Timer A. The clock request logic for SMCLK was disabled (This was to stop SMCLK when entering LPM where it would normally be off ).

# Equipment

* CrossStudio for MSP430
* TI MSP-EXP430F5438 Experimenter Board
* Oscilloscope

# Procedure

Running the code shown in Figure 1 we start by setting both MCLK and SMCLK to 25 MHz. It is necessary change the MSP core voltage to level 3 and select the appropriate DCORSEL value in order for the chip to support 25 MHz clock. Using “UCSCTL2=762” the default input clock frequency is multiplied up to approximately 25 MHz , setting UCSCTL1 the appropriate DCO is selected, and lastly UCSCTL4 is set in order to use our 25 MHz clock as inputs for MCLK and SMCLK. The 25 MHz SMCLK output is shown in Figure 2.

In order to most easily output PWM signals from the Timer A modal we can use any convenient CCRx “OUTx” pins. In this case those pins are connected to CCR1 and CCR2 at 8.6 and 7.3. In order for these outputs to drive a PWM signal it is necessary to define the proper output mode. Using “OUTMOD\_4” will set the output pin to be toggled on/off every time the TAxCCRn value and the programed value in the respective CCRx register match in the comparitor. Setting TA1CCTL0 =125 sets the peak of our timer in up/down mode, as seen in Figure 3. Setting the values of TA1CCR1 and TA1CCR2 as close as possible to 25% and 75% of TA1CCR0 produces the respective 25 and 75% duty cycle 10 s pulse.

# 4. Results

As in Lab 1 the 25 MHz clocks on both MCLK an SMCLK are very noisy but still seem to work just fine. The final output of the duty cycle is shown in Figure 4.

* *What happened?*
* *Did it work as expected?*
* *If not, why?*
* *If it did work, how could you make it better?*

# 5. Discussion and Questions

* *Answer the questions that were asked in the assignment (sometimes it might be more practical to include them in the previous section).*

# 6. Conclusion

* *What was the point of this lab?*
* *What did you learn from this lab?*

# 7. Attachments

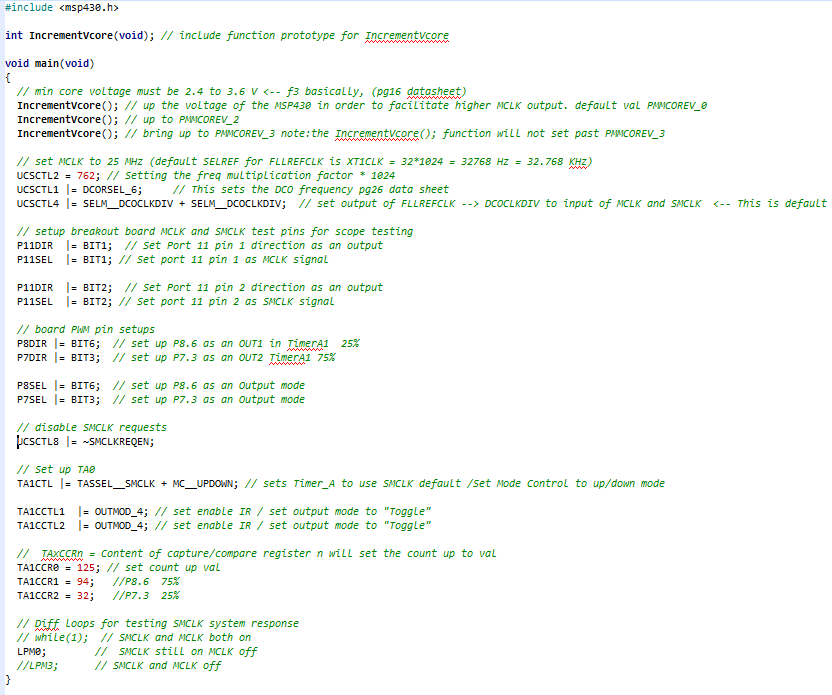


Figure 1: Lab 2 code, incrementVcore was also included in this solution.

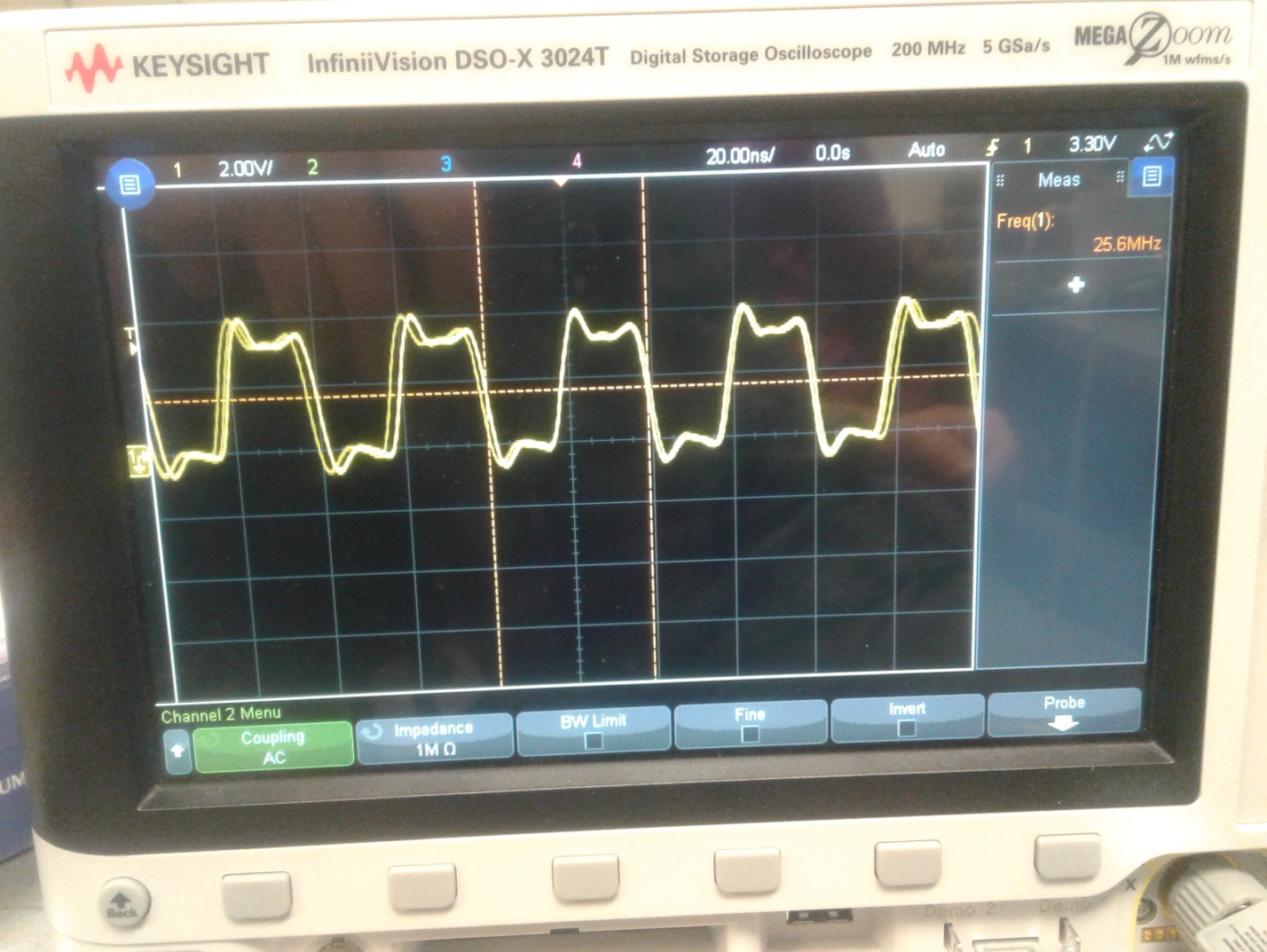


Figure 2: 25 MHz SMCLK output.

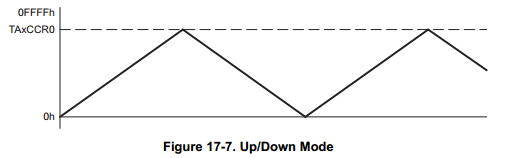


Figure 3: Up/Down Mode timer.

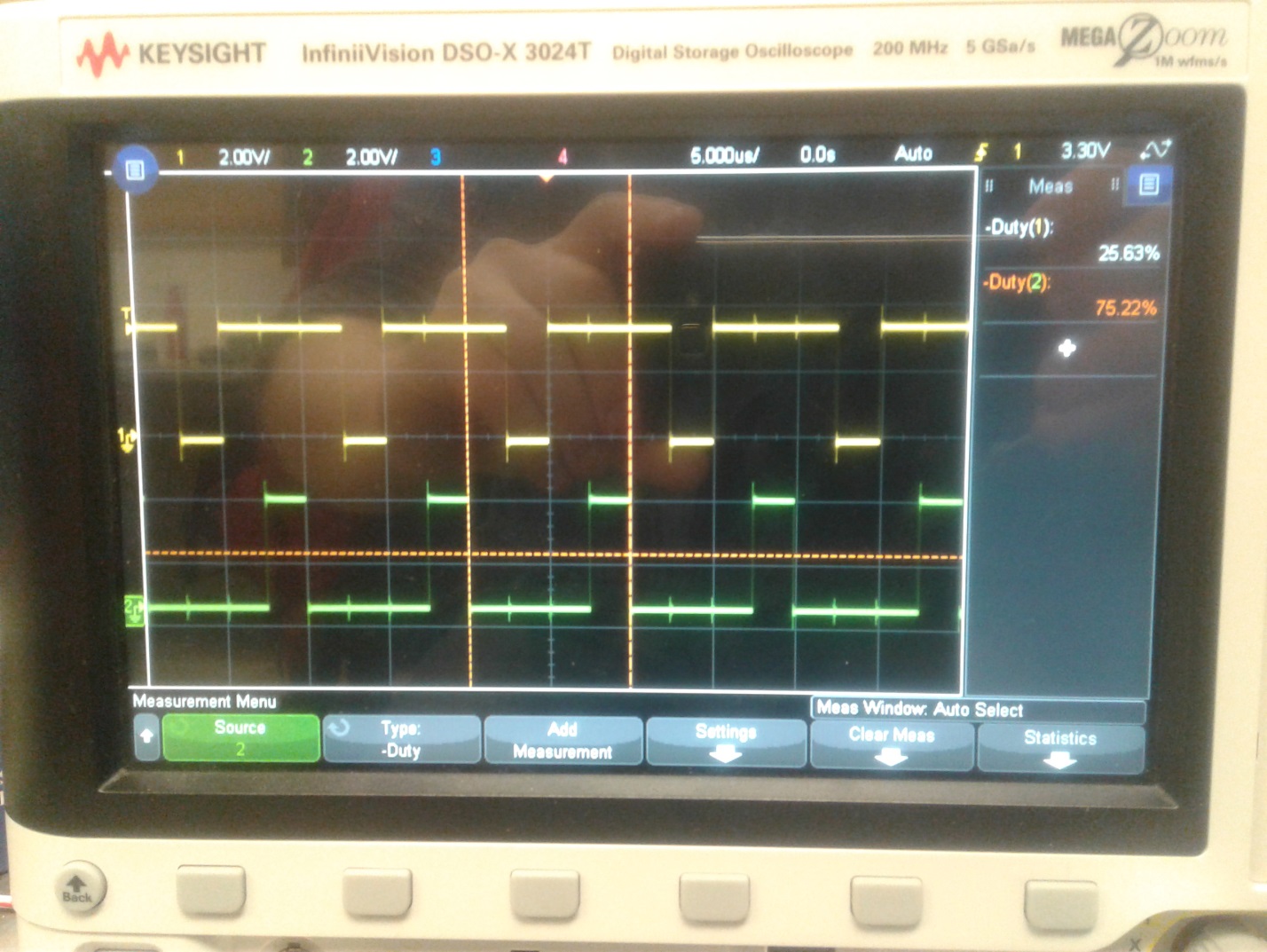


Figure 4: Timer A 75% and 25% duty cycle output.