EE 444

Timer A output modes

Lab 2: *MSP430: Digital I/O*

*2/14/2017*

**Chic J O’Dell**

Does your solution work the way it’s supposed to work? □YES □NO1

1If your answer is NO, please explain in your report.

Instructor/TA comments and grading

# Objective and Background

Using Timer A in order to output a PWM pulse with a variable duty cycle (75 and 25 %) for a signal of . In order to achieve high precision both SMCLK and MCLK are set to 25 MHz, SMCLK to be used as the source for Timer A. The clock request logic for SMCLK was disabled (This was to stop SMCLK when entering LPM where it would normally be off).

# Equipment

* CrossStudio for MSP430
* TI MSP-EXP430F5438 Experimenter Board
* Oscilloscope

# Procedure

Running the code shown in Figure 4 we start by setting both MCLK and SMCLK to 25 MHz. It is necessary change the MSP core voltage to level 3 and select the appropriate DCORSEL value in order for the chip to support 25 MHz clock. Using “UCSCTL2=762” the default input clock frequency is multiplied up to approximately 25 MHz , setting UCSCTL1 the appropriate DCO is selected, and lastly UCSCTL4 is set in order to use our 25 MHz clock as inputs for MCLK and SMCLK. The 25 MHz SMCLK output is shown in Figure 2.

Setting UCSCTL8 allows for SMCLK requests to be disabled. This setting is tested by putting the MSP in different low power modes. Give ~SMCLKREQEN SMCLK should no longer function in LPM2 and lower.

In order to most easily output PWM signals from the Timer A modal we can use any convenient TA1CCRx “OUTx” pins. In this case those pins are connected to TA1CCR1 and TA1CCR2 at 8.6 and 7.3. In order for these outputs to drive a PWM signal it is necessary to define the proper output mode. Using “OUTMOD\_4” will set the output pin to be toggled on/off every time the TAxCCRn value and the programed value in the respective TA1CCRx register match in the comparator. Given we are using SMCLK of 25 MHz and we want a period of 10 we will set TA1CCTL0 =125 so that the peak of our timer in up/down mode, as seen in Figure 1 produces a 10ns pulse. Setting the values of TA1CCR1 and TA1CCR2 as close as possible to 25% and 75% of TA1CCR0 produces the respective 25 and 75% duty cycle of a10 s pulse.

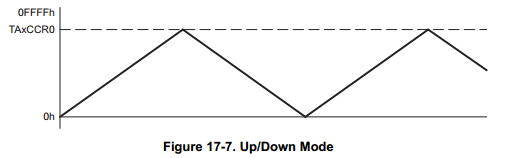


Figure 1: Up/Down Mode timer.

# 4. Results

As in Lab 1 the 25 MHz clocks on both MCLK an SMCLK are very noisy but still seem to work just fine as seen in Figure 2.

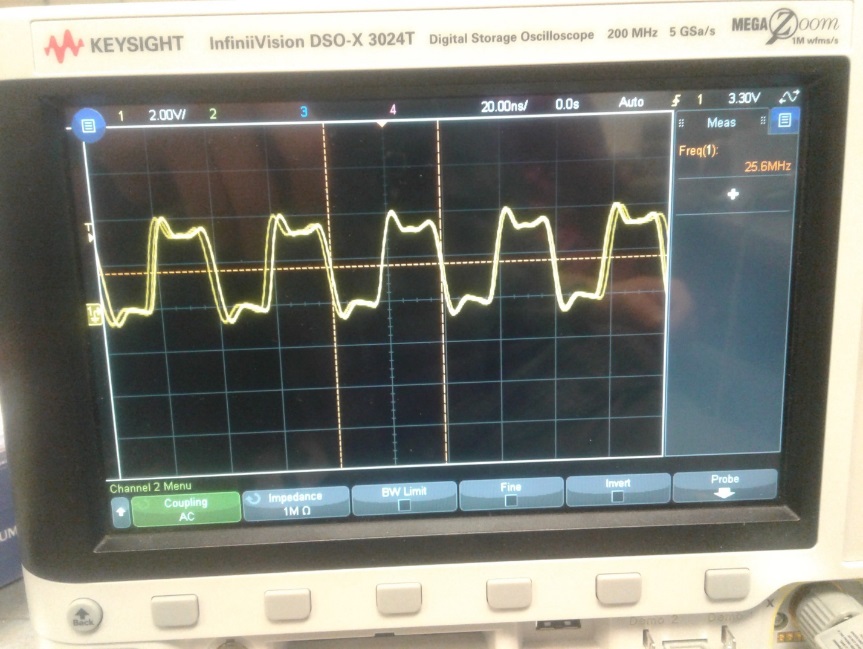


Figure 2: 25 MHz SMCLK output.

The final output of the duty cycle is shown in Figure 3 with 25.63% and 75.22% given TACCRn of 32 and 94.

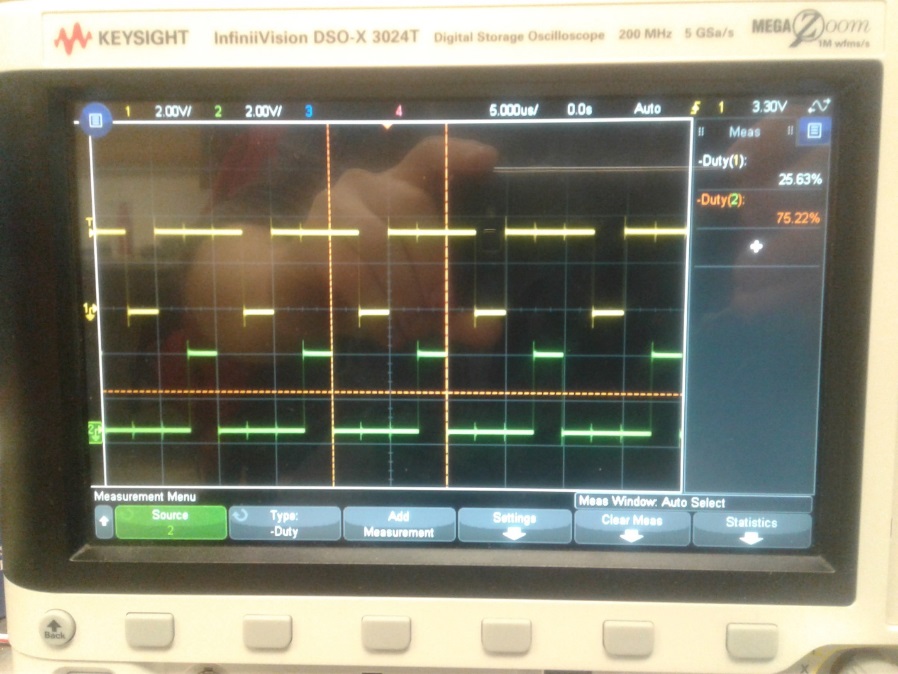


Figure 3: Timer A 75% and 25% duty cycle output.

Using different low power modes and an endless loop checking the outputs of MCLK and SMCLK are as seen in Table 1. These results are not surprising as they are consistent with what the MSP430f5xx user guide tell us to expect (pg168). As long as the SMCLK SMCLKREQEN bit is set to 0 the SMCLK will not run in any mode given SMCLKOFF has a default value of 0. If we do not set SMCLKREQEN SMCLK will remain in operation down to LPM4.

Table : MCLK and SMCLK outputs given different CPU states with SMCLKREQEN disabled.

|  |  |  |  |
| --- | --- | --- | --- |
|  | AM | LPM0 | LPM3 |
| MCLK | on | off | off |
| SMCLK | on | on | off |

# 5. Conclusion

This lab highlighted a very important use of the timer module to generate variable duty cycle pulses without the MSP processor even being awake. The cavoite to this mode of operation being the clock used by the timer module will not run in some low power mode. This means it is important to know what clock your feeding your modules and understanding clock requests

# 6. Attachments

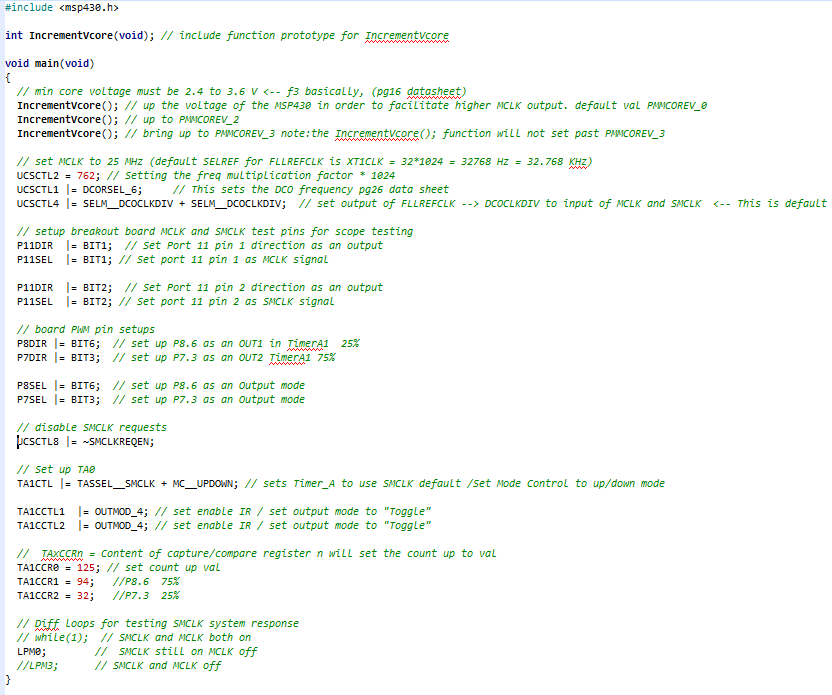


Figure : Lab 2 code, incrementVcore was also included in this solution.