Lab 5: Character LCD Control

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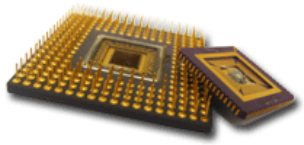
Fall, 2025

Lab 5: Character LCD Control

- In this lab, you will implement a slot machine by switches and display the results on the standard 1602 character LCD.
- The lab file submission deadline is on 10/13 by 6:00pm.

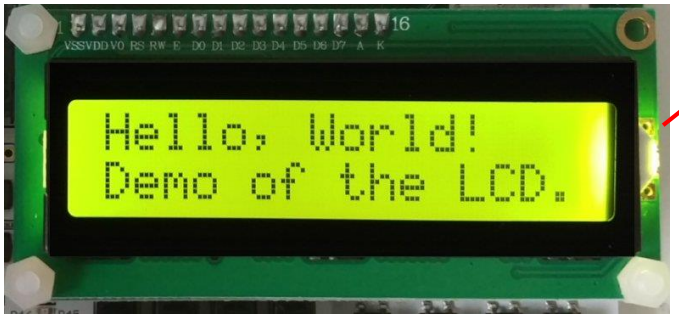
1602 Character LCD Display

- The Arty board has only simple I/O devices such as the LEDs, switches, buttons, and UART.
- We have designed an expansion board, Arty_IO, that adds three more peripherals to Arty:
  - a 1602 character LCD device (supports only 4-bit mode)
  - a SD card socket (supports only the SPIF mode)
  - a 12-bit color VGA interface



Memory Map of the LCD

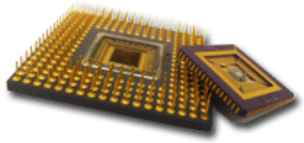
- The LCD device can be treated as a 32-byte memory.
  - Each memory cell corresponds to a character on the display.
  - Writing an ASCII code to a cell will display the character on the corresponding location on the LCD:



Note: the LCD device is slow, you should not update the screen faster than 2 Hz.

- Display data memory (DD RAM) addresses:

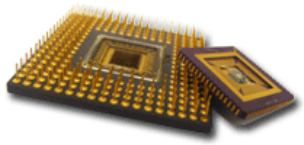
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16



Character LCD Interface (1/2)

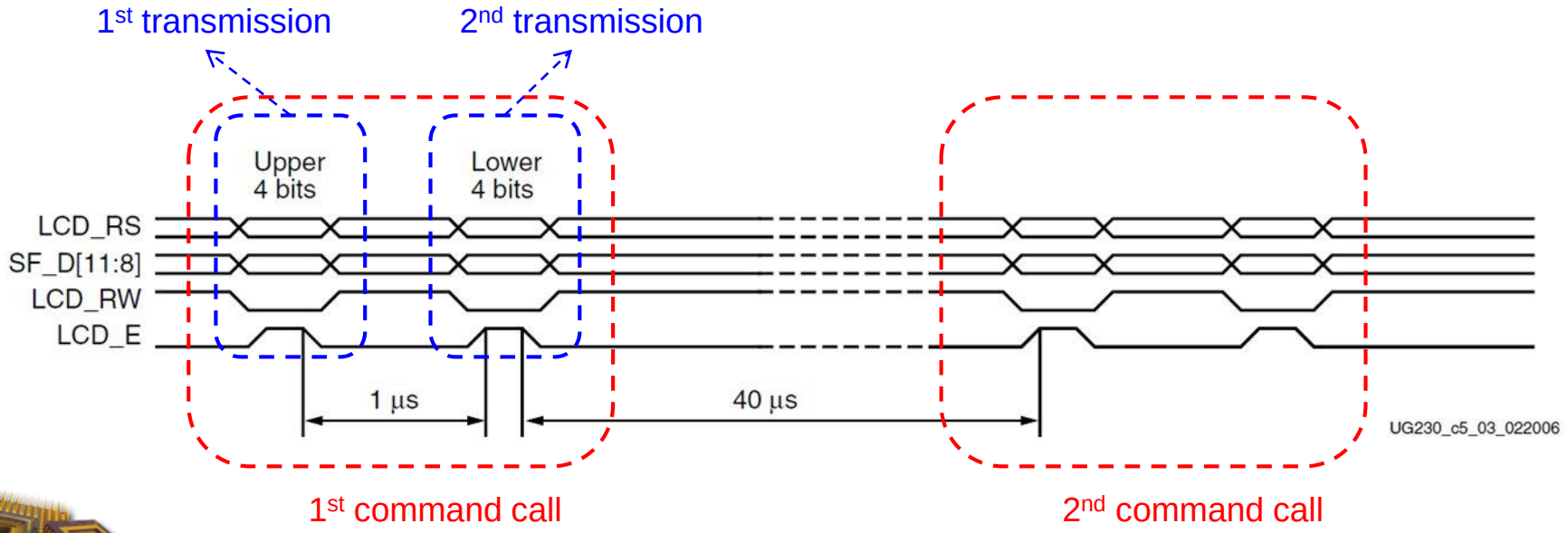
- The LCD interface has 8 data wires (DB0 ~ DB7) and 3 control wires (LCD_E, LCD_RS, LCD_RW):
  - LCD_E enables/disables the inputs to the LCD module.
  - The rest of the wires are defined depending on the functions:

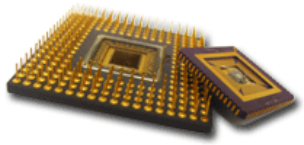
Function	LCD_RS	LCD_RW	Upper Nibble				Lower Nibble			
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Clear Display	0	0	0	0	0	0	0	0	0	1
Return Cursor Home	0	0	0	0	0	0	0	0	1	-
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display On/Off	0	0	0	0	0	0	1	D	C	B
Cursor and Display Shift	0	0	0	0	0	1	S/C	R/L	-	-
Function Set	0	0	0	0	1	0	1	0	-	-
Set CG RAM Address	0	0	0	1	A5	A4	A3	A2	A1	A0
Set DD RAM Address	0	0	1	A6	A5	A4	A3	A2	A1	A0
Read Busy Flag and Address	0	1	BF	A6	A5	A4	A3	A2	A1	A0
Write Data to CG RAM or DD RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Read Data from CG RAM or DD RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0



Character LCD Interface (2/2)

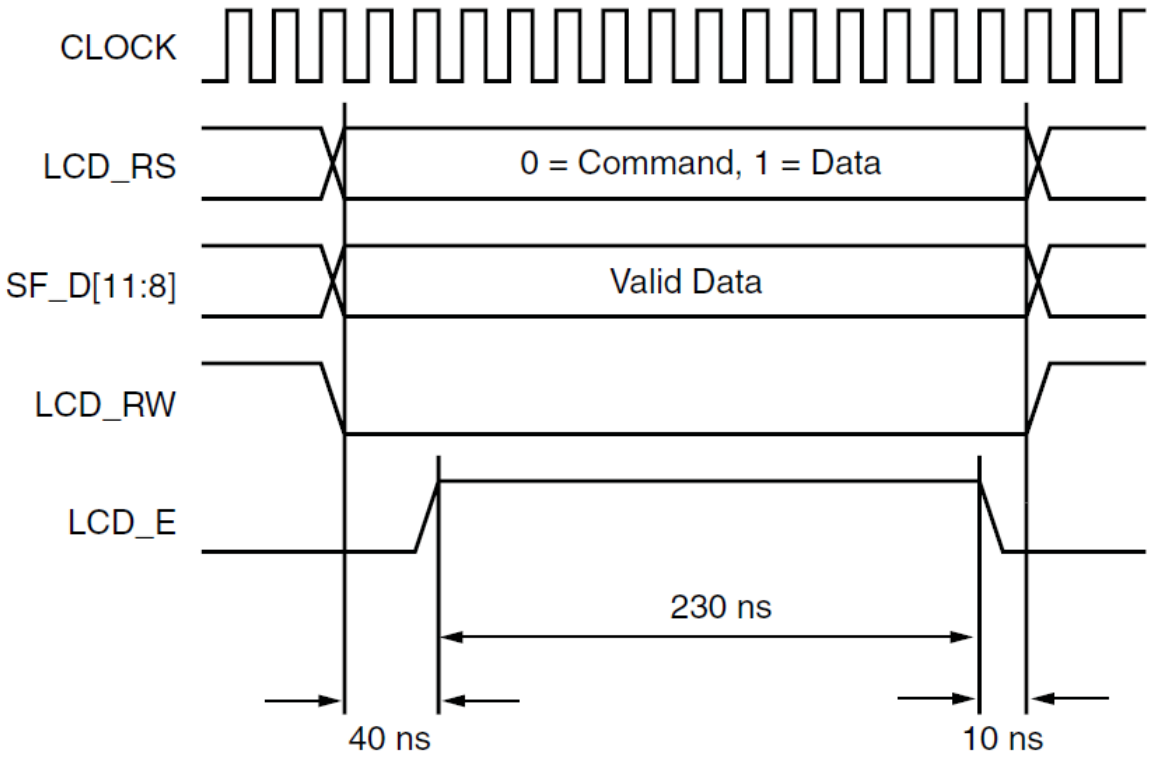
- However, the Arty_IO board uses the 4-bit operating mode of the LCD device, that is, only DB4~DB7 are connected to the FPGA.
  - Execution of a function will need two transmissions, using only LCD_E, LCD_RS, LCD_RW, and DB4~DB7:

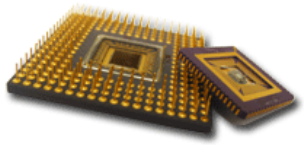




Timing Diagrams for Transmission

- The timing diagram for one transmission in four-bit mode is as follows:
  - Note that execution of a function requires two transmissions.





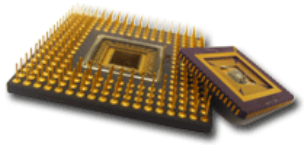
Sample Circuit of Lab 5

- Two Verilog program files will be provided to you:
  - LCD_Module.v – An LCD controller module (You do not need to modify this file)
  - Lab5.v – a sample top-level module that prints a “Hello, World!” message using the LCD controller module

```
module LCD_module(
    input clk,
    input reset,
    input [127:0] row_A,
    input [127:0] row_B,
    output reg LCD_E,
    output reg LCD_RS,    //register select
    output reg LCD_RW,    //read / write
    output reg [3:0]LCD_D //data
    );
```

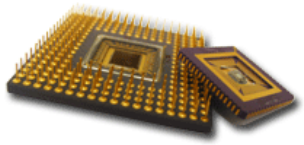
top-row of text

bottom-row of text



Slot Machine

- In this lab, you will implement a slot machine using switches and LCD display.
- Since a casino needs to earn money, we should implement the certain rule.
- [Important] It is not wise to gambling!



What to Do in Lab 5

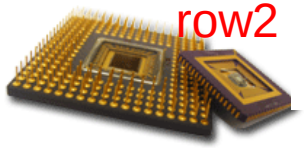
- In Lab 5, you will need to implement following things:
  - Design a circuit to generate some numbers sequences and store the results into the register array.
  - Once they are stored, the LCD will start displaying numbers:
    - In the initial state, your LCD should only display the first and second number in each column.
    - If switch 0 (SW0) is first push down, the LCD scrolls up one number for each column cyclically roughly every 1 or 2 sec.
    - If switch 1 (SW1) is push down, the last column of number should stop counting.
    - If switch 2 (SW2) is push down, the middle column of number should stop counting.
    - If switch 3 (SW3) is push down, the first column of number should stop counting.

row1

row2

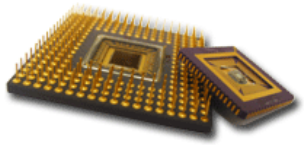
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

col1 col2 col3



What to Do in Lab 5

- If four switches are pull down (low signal level), your LCD should immediately show some result:
  - If all the numbers of three columns are the same, your LCD should output “Jackpots!” in first row.
  - If two of the numbers of three columns are the same, your LCD should output “Free Game!” in first row.
  - If none of numbers of three columns are the same, your LCD should output “Loser!” in first row.
  - You should also show “Game over” in second row in each case.
- Your circuit should come back to initial status and well-prepared for next player when the reset button is pressed.



What to Do in Lab 5

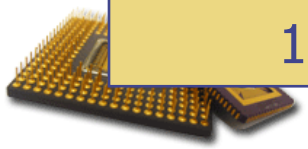
- Each column of LCD should display the following number sequence:
  - First column: {1,2,3,4,5,6,7,8,9,1,2,3…} (scrolls up each second)
  - Second column: {9,8,7,6,5,4,3,2,1,9,8,7…}

  (scrolls up each two second)
  - Third column: you can design your own number sequence! But each sequence should contains all 9 numbers

  (scrolls up each second)
- The first row in LCD should show the future number, while the second row in LCD should show current number.
- Example: assume third column is same as first column:

Initial state

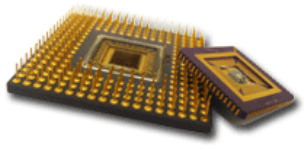
2 | 8 | 2 1 | 9 | 1	3 | 8 | 3 2 | 9 | 2	4 | 7 | 4 3 | 8 | 3



(Advanced) What to Do in Lab 5

- You can earn extra 20% on this lab by correctly implementing the advanced circuit.
- For the advanced part, we'll add a circuit to prevent misuse or cheating.

- If SW1~3 are pulled down before SW0, stop the game.
- During gameplay, if any switch is pulled down and then up again, stop the game.
- Show "ERROR" on the first row and "game stopped" on the second row when these conditions occur.



Reminder

- You can assume when the circuit is first activate or reset, all switches are pulled up (high signal level).
- Your LCD should remain clear when there is no character need to be printed.
- TA will provide an demo example video on E3.
- TA would ask some questions during demo.
  - Please zip and upload the whole project including .bit file on E3 before deadline.