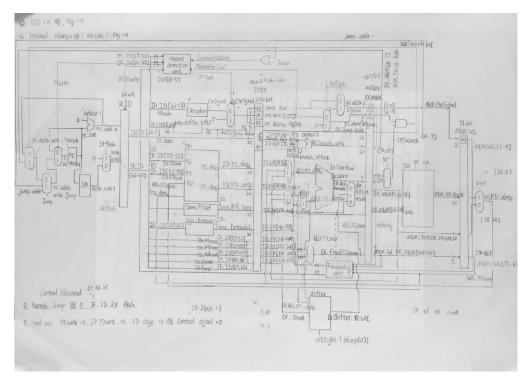
# **Computer Organization**

## Architecture diagrams:



### Hardware module analysis:

Data hazard:EX stage 若是 LW 指令且 EX \$RT == ID \$RS || ID \$RT, Program counter 及 IF/ID Register 不更新

Forwarding: data dependence 時將 MEM stage 或 WB stage 結果 Forward 回去 EX stage

Control hazard:發生 Branch 或 Jump 時將 IF/ID、ID/EX、EX/MEM Register Flash 掉。

#### Finished part:

Data hazard

Forwarding

Control hazard

#### Problems you met and solutions:

無

#### Summary:

無