Computer Architecture

[HW5] 102062111 林致民

Q1

Assembly

```
Loop:
    L.D       F2, 0(Rx)
    ADD.D     F2, F0, F4
    MULT.D    F8, F2, F4
    S.D       F8, 0(Rx)
    DIV.D     F6, F0, F2
    ADD.I     Rx, Rx, #8
    SUB       R20, R4, Rx
    BNZ       R20, Loop
```

Functional Units

FU Type	Cycles in EX	Number of FUs	Number of reservation states
Integer	1	1	5
FP adder	10	1	3
FP multiplier	15	1	2

(a)

根據 `L11, p36` ，定義 `Read access` 也需要 `1 cycle` 定義 `DIV.D` 需要 `15 cycles`

Iteration	Instructions	Issue	Execute	Read access	Write CDB	Commits	Comment
1	`LD F2, 0(Rx)`	1	2	3	4	5	First Issue
1	`ADD.D F2, F0, F4`	1	2		12	13	Wait for `L.D`
1	`MULT.D F8, F2, F4`	2	13		28	29	Wait for `ADD.D`
1	`S.D F8, 0(Rx)`	2	3			29	Wait for `MULT.D`
1	`DIV.D F6, F0, F2`	3	13		28	29	Wait for `ADD.D`
1	`ADD.I Rx, Rx, #8`	3	4		5	6	
1	`SUB R20, R4, Rx`	4	6		7	8	Wait for `ADD.I`
1	`BNZ R20, Loop`	4	8			9	Wait for `SUB`
2	`L.D F2, 0(Rx)`	5	6	7	8	13	Wait for `ADD.D`
2	`ADD.D F2, F0, F4`	5	13		23	24	Wait for `L.D`
2	`MULT.D F8, F2, F4`	6	24		39	40	Wait for `ADD.D`
2	`S.D F8, 0(Rx)`	6	7			40	Wait for `MULT.D`
2	`DIV.D F6, F0, F2`	7	24		39	40	Wait for `ADD.D`
2	`ADD.I Rx, Rx, #8`	7	8		9	10	
2	`SUB R20, R4, Rx`	8	10		11	12	Wait for `ADD.I`
2	`BNZ R20, Loop`	8	12			13	Wait for `SUB`

(b)(1)

dest	value	instruction	Done
F2		L.D F2, 0(Rx)	Y
F2		ADD.D F2, F0, F4	Y
F8		MULT.D F8, F2, F4	EX
--		S.D F8, 0(Rx)	EX
F6		DIV.D F6, F0, F2	EX
Rx		ADD.I Rx, Rx, #8	Y
R20		SUB R20, R4, Rx	Y
--		BNZ R20, Loop	Y