Homework 05 Combinational Design in Verilog HDL

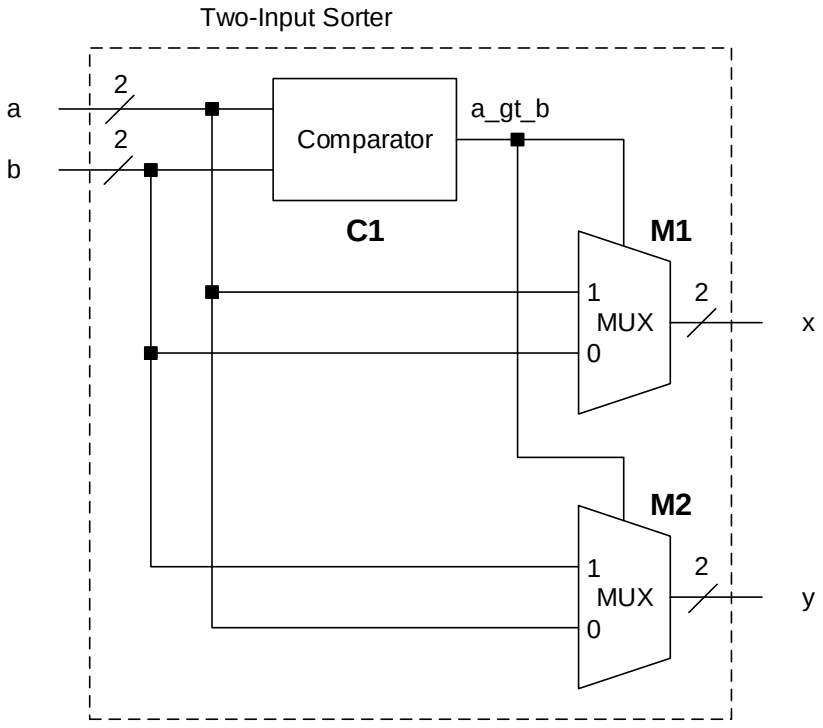
Due on ~~December 9, 10:10am~~ December 16, 11:00pm

1. [Carry Lookahead Adder]
   (a) Write a Verilog model of a 3-bit carry lookahead adder that adds two 3-bit signed 2's-complement numbers A[2:0] and B[2:0] to produce a 3-bit sum S[2:0] and a 1-bit overflow indicator V. When an overflow occurs, V is equal to 1; otherwise V is equal to 0. You must use the following template for your top module.

```
module HW5_1 (S, V, A, B);
  output [2:0] S;
  output V;
  input  [2:0] A, B;
  // add the details of your adder here
endmodule
```

   (b) Write a test bench that tests all possible input combinations of your adder.

2. [Parallel Sorter]
   (a) Write a Verilog model of a two-input sorter. The inputs, a and b, are 2-bit unsigned numbers. The larger of them goes to x; the smaller goes to y. That is, x = max(a, b) and y = min(a, b). You have to write the Verilog model according to the block diagram shown below:

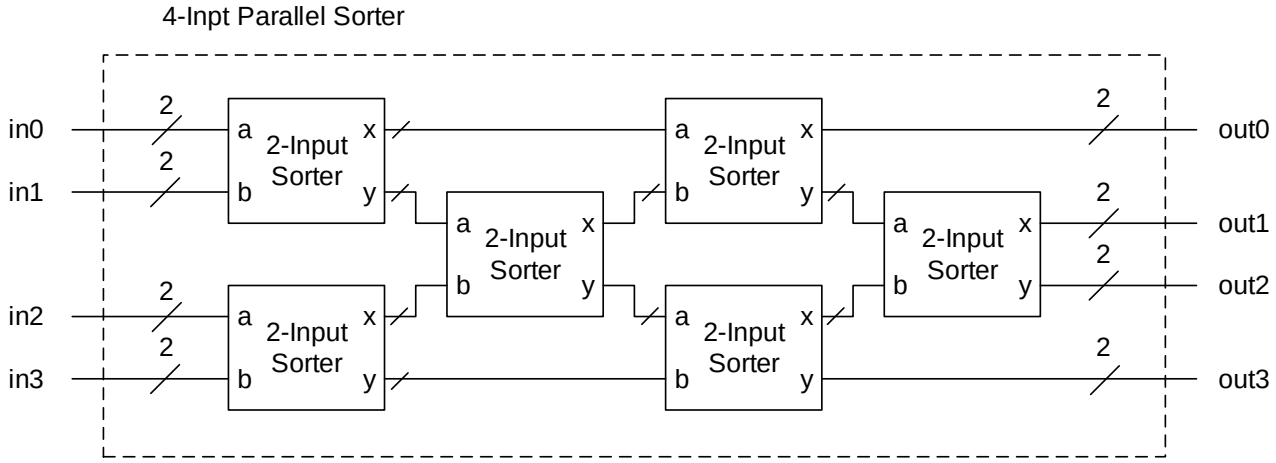


   Use the following template for your top module:

```
module HW5_2a (x, y, a, b);
  output [1:0] x, y;
  input  [1:0] a, b;
  // add the details of your adder here
endmodule
```

Write a test bench that tests all possible input combinations.

(b) Using the two-input sorter to build a four-input parallel sorter. You have to write the Verilog model according to the block diagram shown below:



Use the following template for your top module:

```
module HW5_2b (out0, out1, out2, out3, in0, in1, in2, in3);
  output [1:0] out0, out1, out2, out3;
  input  [1:0] in0, in1, in2, in3;
  // add the details of your adder here
endmodule
```

Write a test bench that tests all possible input combinations.

Requirement

Submit the source codes (Verilog designs and their test benches) with a brief summary report (of a few paragraphs). Our TAs will announce the details later.