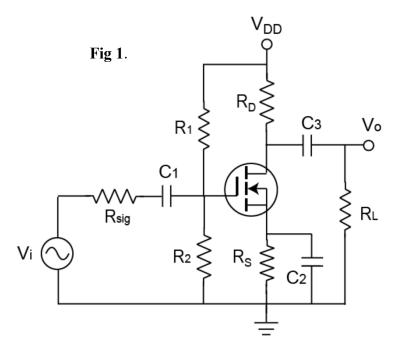
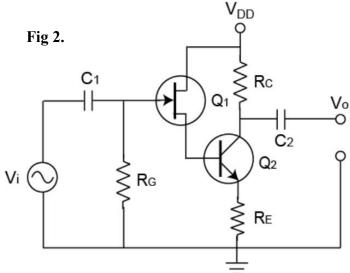
PHYS309 應用電子學一 Final Exam Date: 6/21/2021 Time: 50 min

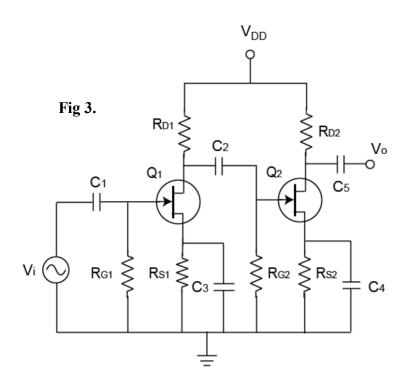
1. Consider the circuit shown in Fig. 1 with E-MOSFET voltage-divider configuration. Here $V_{DD}=30$ V, $V_{in}=0.7$ mV, $r_d=40$ k Ω , $v_{GS(th)}=3.2$ V, $k=5\times10^{-4}$, $R_I=45$ M Ω , $R_I=15$ M Ω



2. The two-transistor amplifier shown in Figure 2 combines a FET Q₁ and a BJT Q₂ to achieve both a high input impedance and a large voltage gain. Assume V_{DD} = 12 V, $g_{os} = 50 \mu S$ and $V_p = -3 V$ for Q₁, and $\beta = 200$ and $r_{\pi} = 100 \Omega$ for Q₂. Here , $R_G = 10 \text{ M}\Omega$, , $R_C = 3 \text{ k}\Omega$, $R_E = 20 \Omega$, $C_I = C_3 = 10 \mu F$. Determine (a) V_{GS} , I_{DSS} (DC) (b) g_m , Z_i (c) Draw the ac equivalent network, i.e. small signal model, (d) $A_V = V_o/V_i$. (30 pt)



3. Consider the JFET cascade amplifier shown in Figure 3. Assume FET Q₁ and Q₂ are identical with $I_{DSS} = 9$ mA, $g_{os} = 50$ µS and $V_p = -2.5$ V. Here $V_{DD} = 20$ V, $R_{GI} = R_{G2} = 10$ M Ω , $R_{DI} = R_{D2} = 3.3$ k Ω , $R_{SI} = R_{S2} = 470$ Ω , $C_I = C_2 = C_5 = 0.05$ µF, and $C_3 = C_4 = 50$ µF. Determine (a) I_{DI} , V_{GS} (DC) (b) g_{mI} , (c) Z_i , and Z_o , (d) $A_V = V_o/V_i$. (30 pt)



4. Consider the circuit shown in Fig 3. Using LT-SPICE determines vo.

Set $v_i = 0.1\sin(\omega t)$, with for frequency from 1mH to 100 MHz.

Send your LT-SPICE file to NTHU-E-Learner system before the deadline 6/21/2021 pm 23:00). (20 pt)

Note:

- (1) JFET: U406 (or pickup one available in the library with similar characteristics)
- (2) Use your student ID as the file name e.g. 101123456.asc
- (2) Use the "TEXT" function (Edit \rightarrow text) to write down your answers and attach them on the worksheet.