

# Eileen HDK 2.0 HMD BD SCHEMATIC

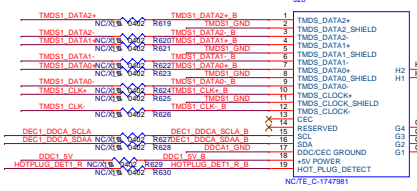
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## MODIFY HISTORY

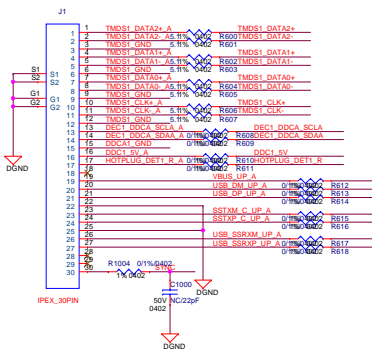
Rev.	STAGE	RELEASE NOTE
G007_A	8L - MOCK UP	1. 12L change to 8L. 2. Add bypass Solomon SD2848 resistor. 3. Reserved EMI recommend solution.
G007_B	8L - DVT	1. Remove Solomon SD2848. 2. Modify reserved EDID download circuit. 3. Add Discharge circuit. 4. Add HOTPLUG_DET powered-down circuit.
G001_A	8L - PVT	1. Fine tune 8870 Core Voltage. 2. Add U54,U61 Enable Pin RC soft start. 3. Reserved MCU HDMI 5V & hotplug detect circuit. 4. Fine tune power sw ic enable soft start.

DDCA\_SDA is a 3.3 V input that is 5 V tolerant  
DDCA\_SCL is a 3.3 V input that is 5 V tolerant

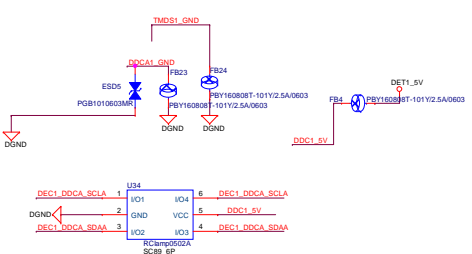
# HDMI Connector



# Universal Connector

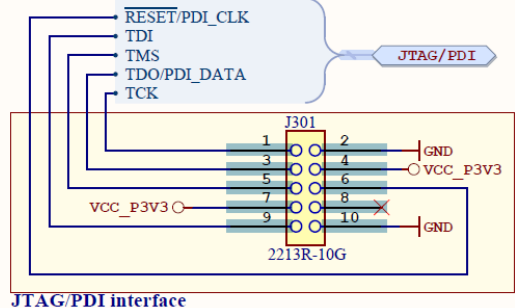


# ESD PROTECTION





## JTAG/PDI

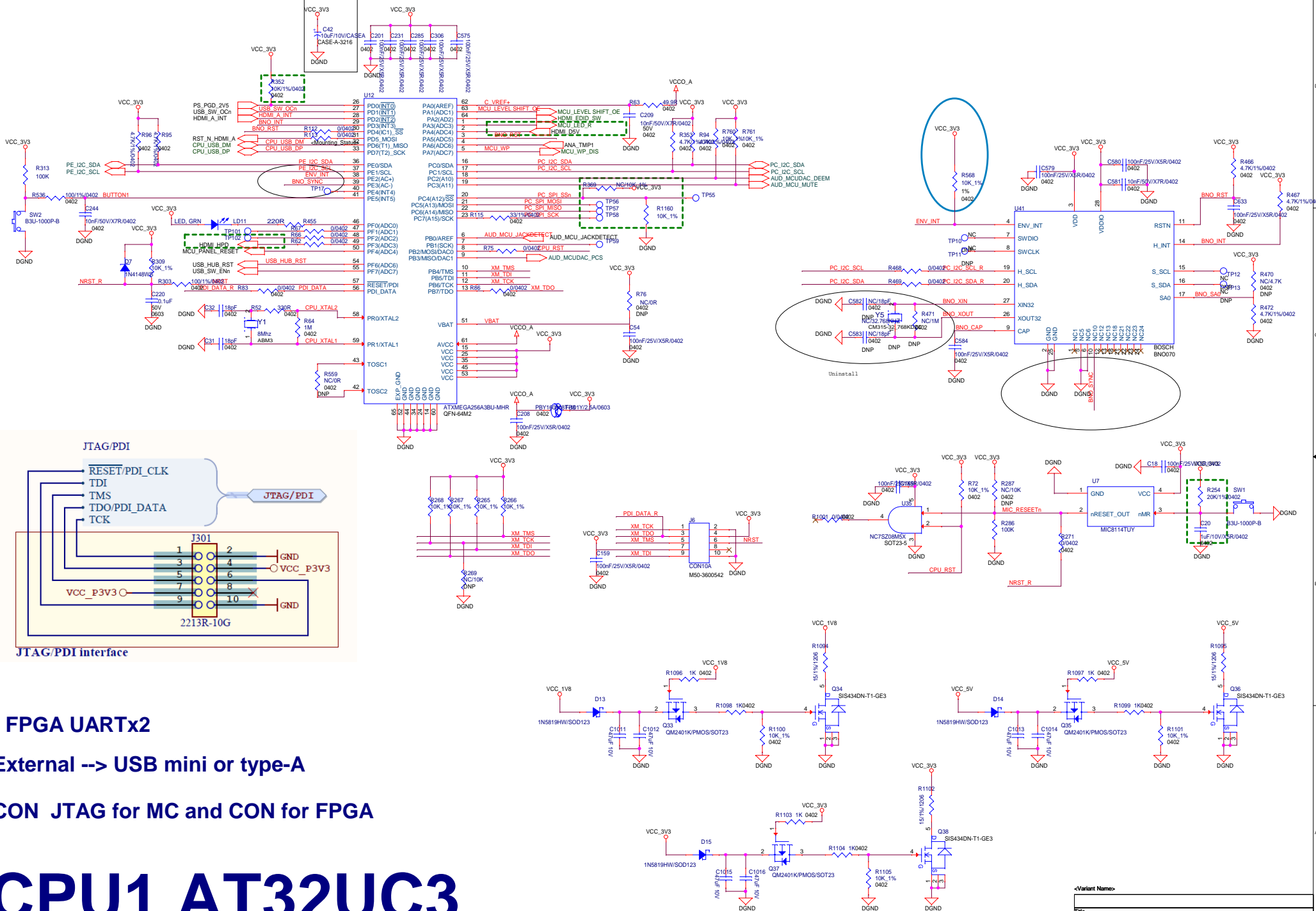


## FPGA UARTx2

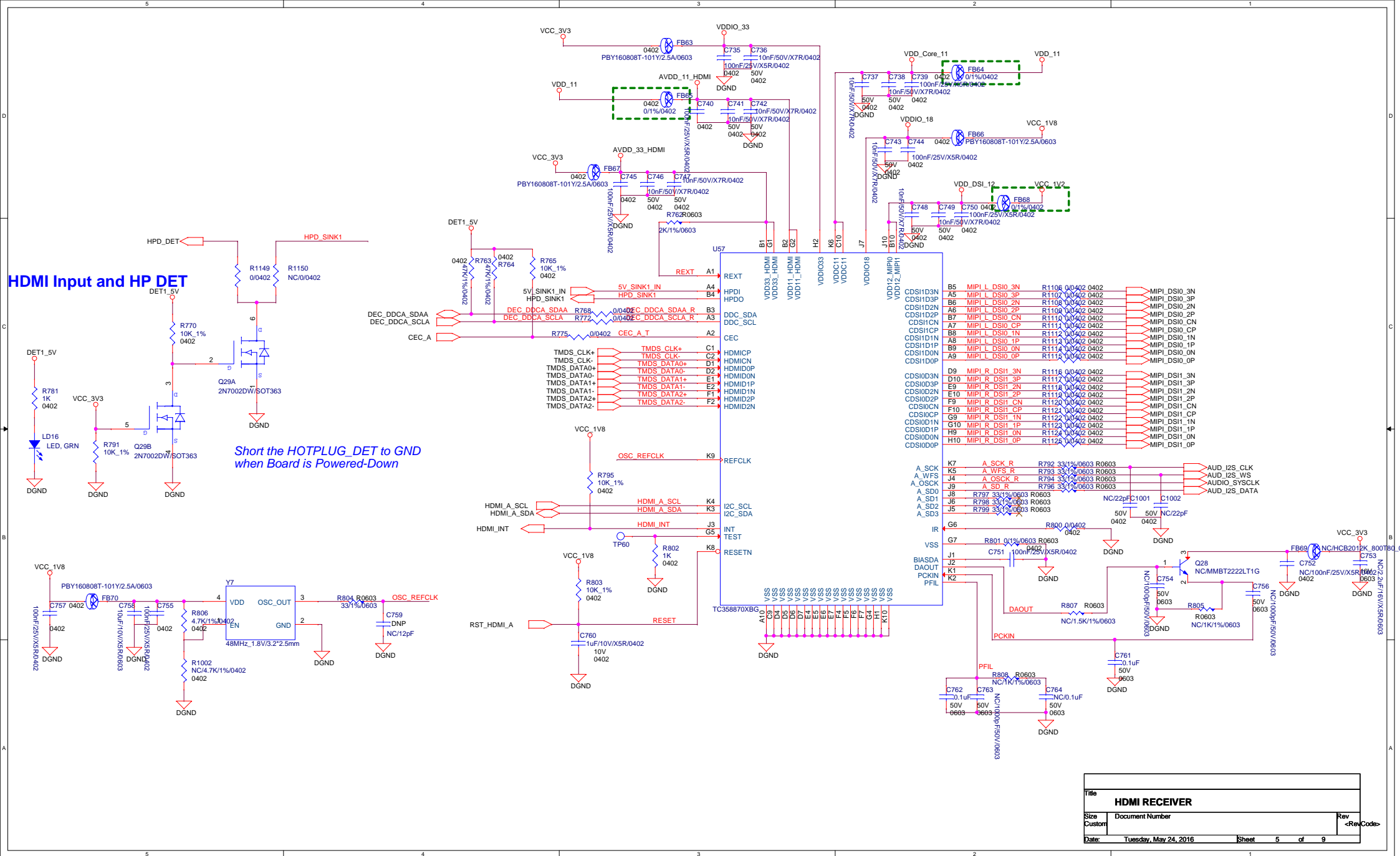
External --> USB mini or type-A

CON JTAG for MC and CON for FPGA

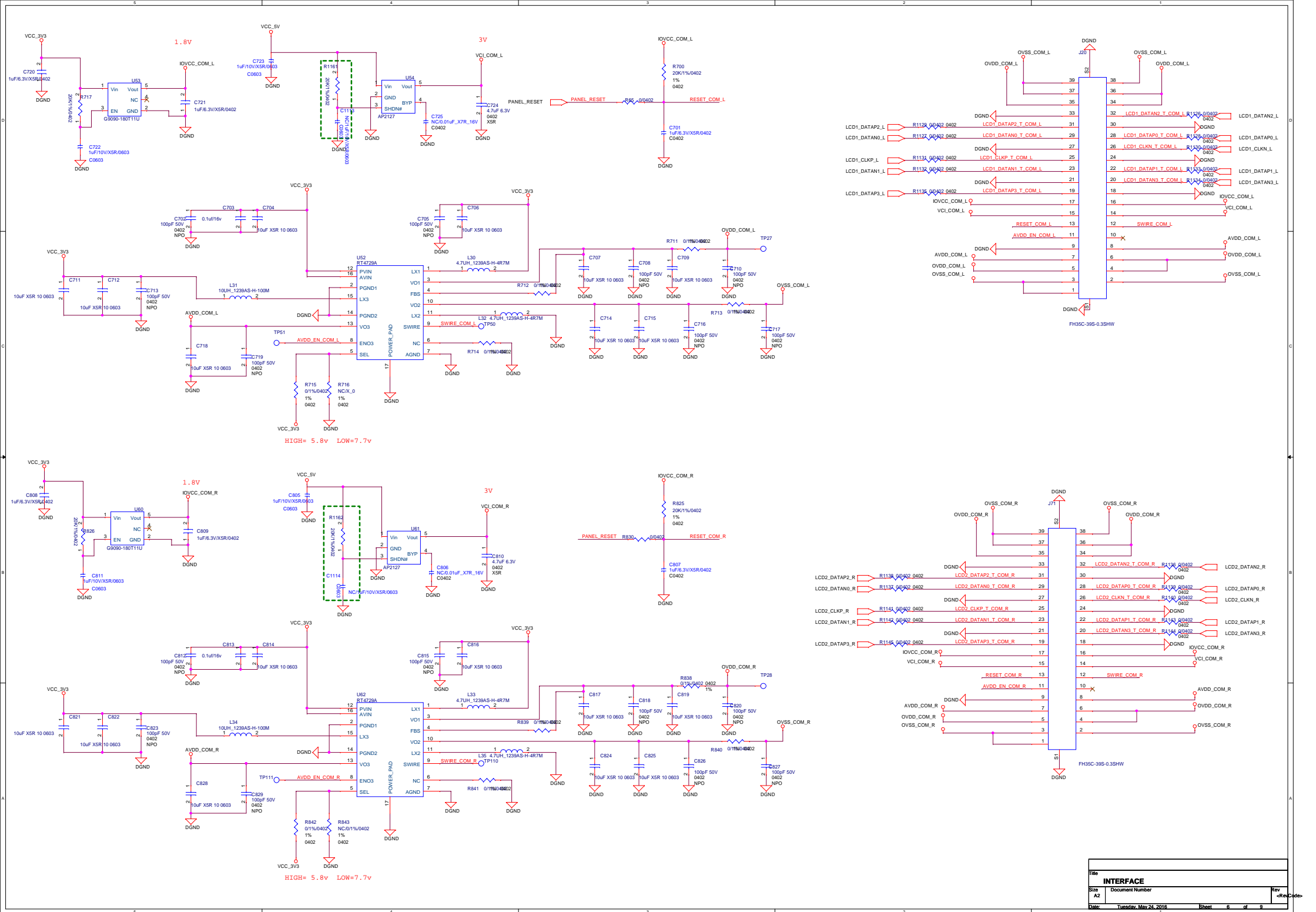
# CPU1 AT32UC3



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CPU1 AT32UC3			
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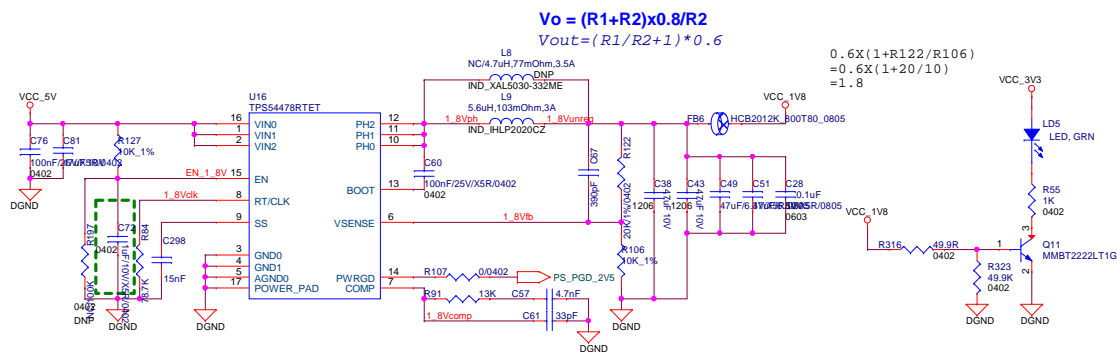
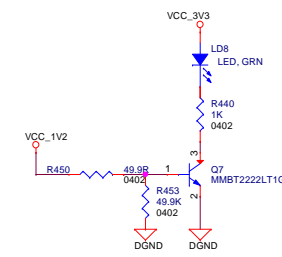
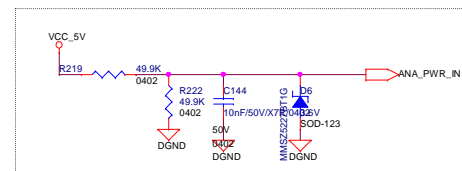
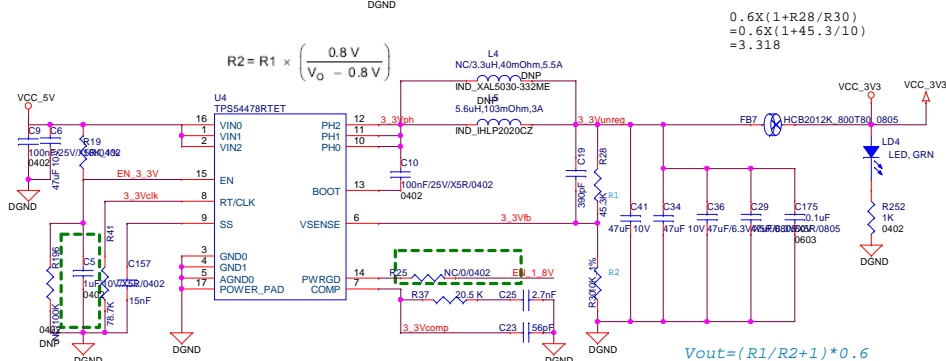
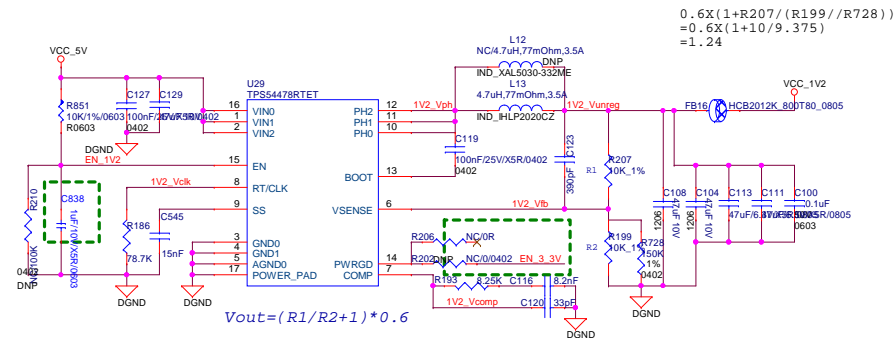
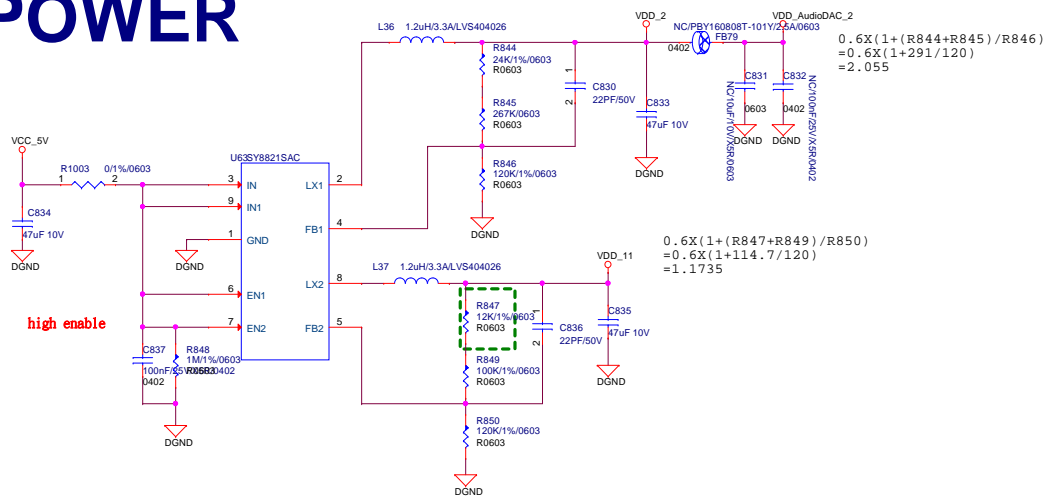


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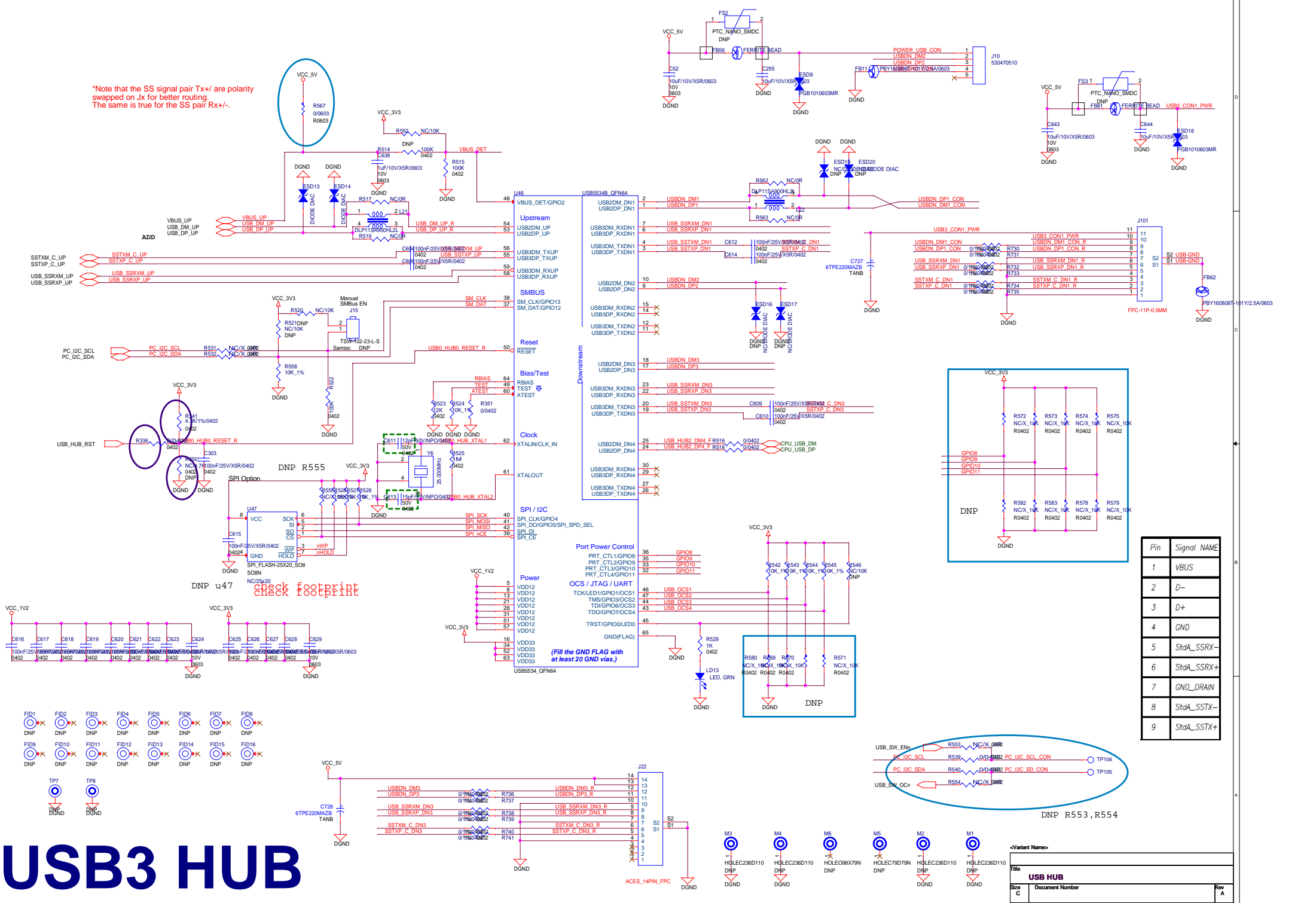
# POWER



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\*Note that the SS signal pair Tx+/- are polarity swapped on Jx for better routing.  
The same is true for the SS pair Rx+/-.



Pin	Signal NAME
1	VBUS
2	D-
3	D+
4	GND
5	StoA_SSRX-
6	StoA_SSRX+
7	GND_DRAIN
8	StoA_SSTX-
9	StoA_SSTX+

# USB3 HUB

<Variant Name>

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