HDMI-Single

VER-T31i_S2_Re_Single

<Variant Name>

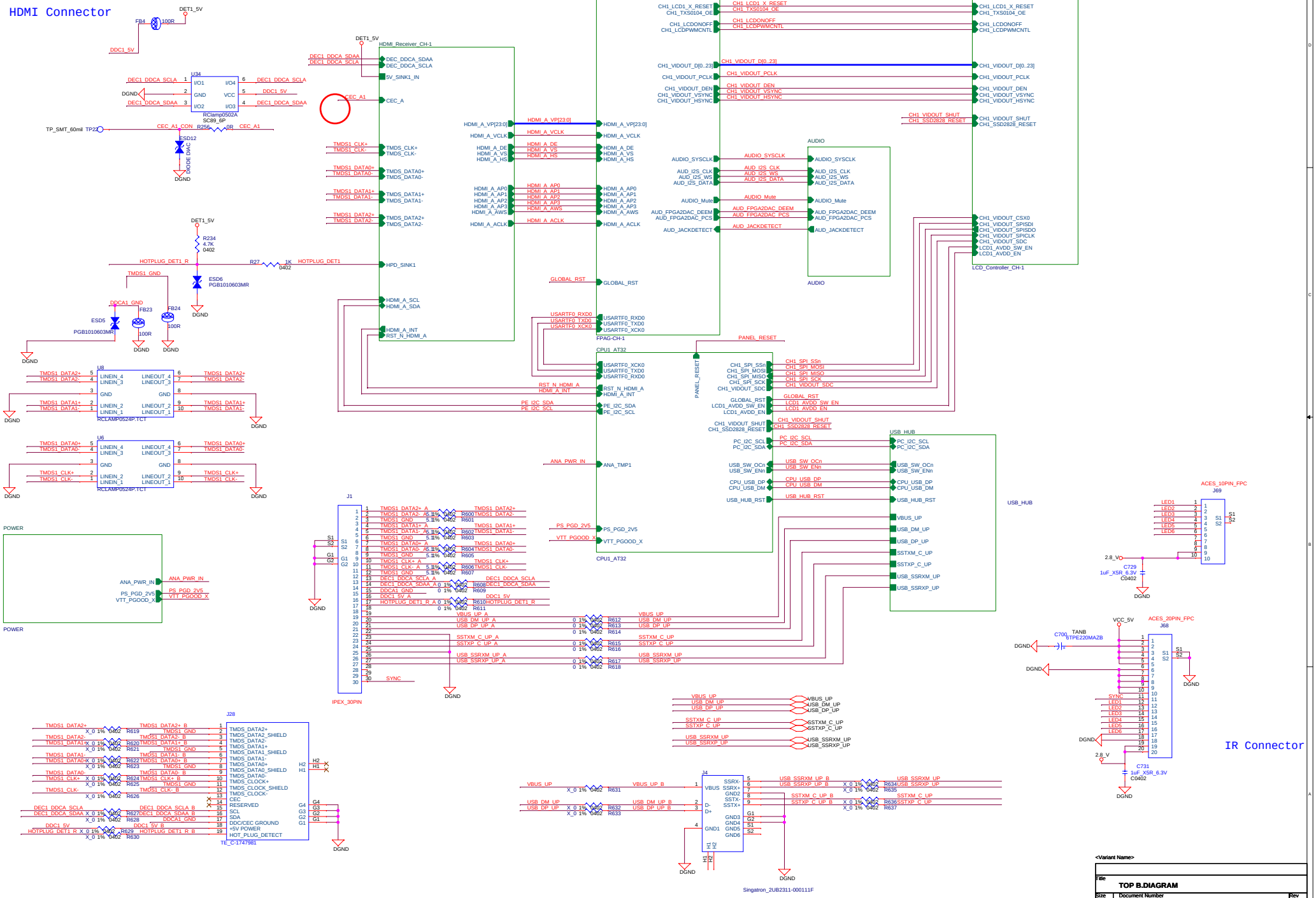
Title: Dual-HDMI		
Size: C	Document Number: <Doc>	Rev: A
Date:	Sheet 1 of 12	

TOP

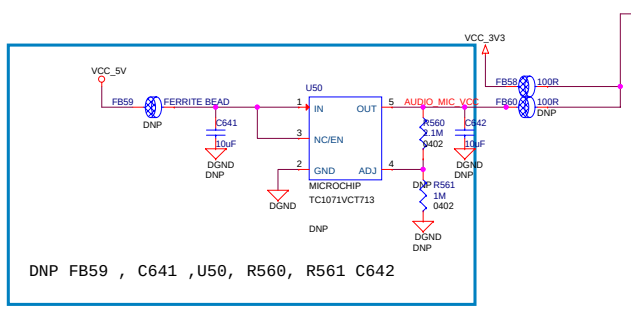
DDCA_SDA is a 3.3 V input that is 5 V tolerant

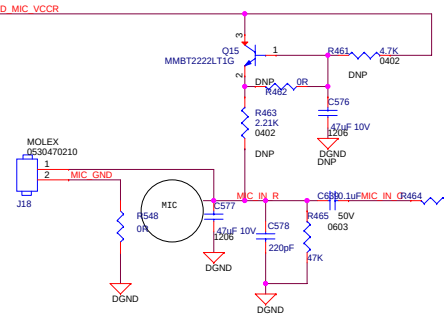
DDCA_SCL is a 3.3 V input that is 5 V tolerant

HDMI Connector

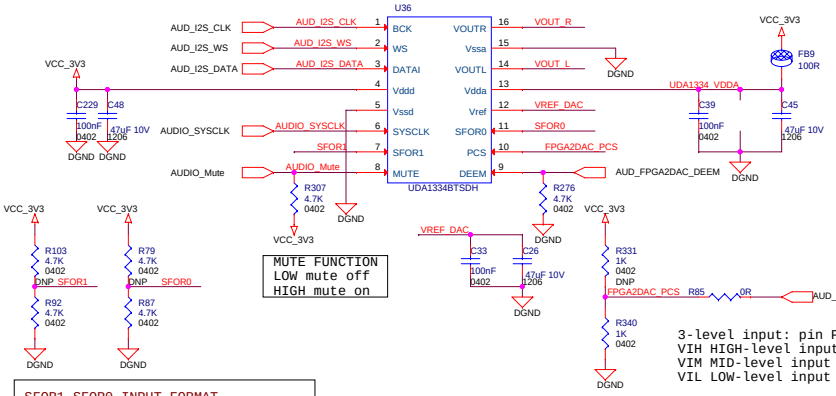


DNP R461 R463 C576





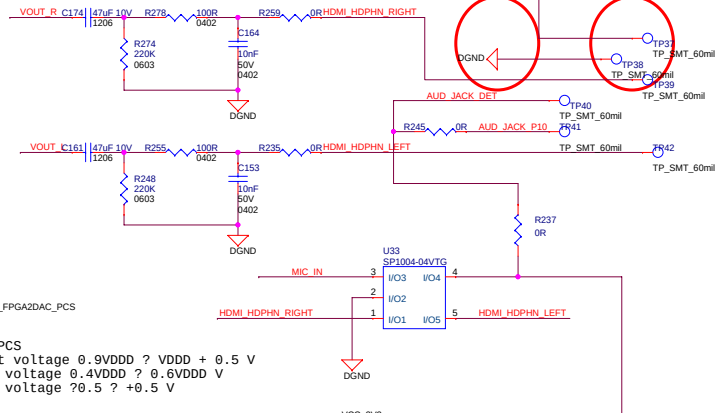
COMPRESSED IMAGE

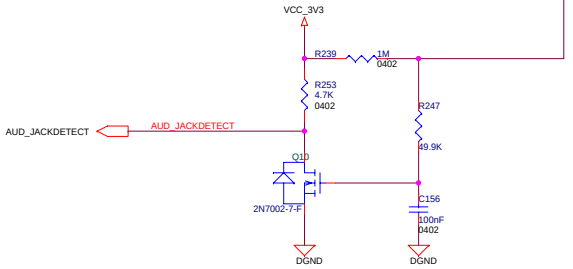


MUTE FUNCTION
LOW mute off
HIGH mute on

SFOR1 SFOR0 INPUT FORMAT
LOW LOW I2S-bus input
LOW HIGH LSB-justified 16 bits input
HIGH LOW LSB-justified 20 bits input
HIGH HIGH LSB-justified 24 bits input

3-level input: pin PCS
VIH HIGH-level input voltage 0.9VDDD ? VDDD + 0.5 V
VIM MID-level input voltage 0.4VDDD ? 0.6VDDD V
VIL LOW-level input voltage ?0.5 ? +0.5 V



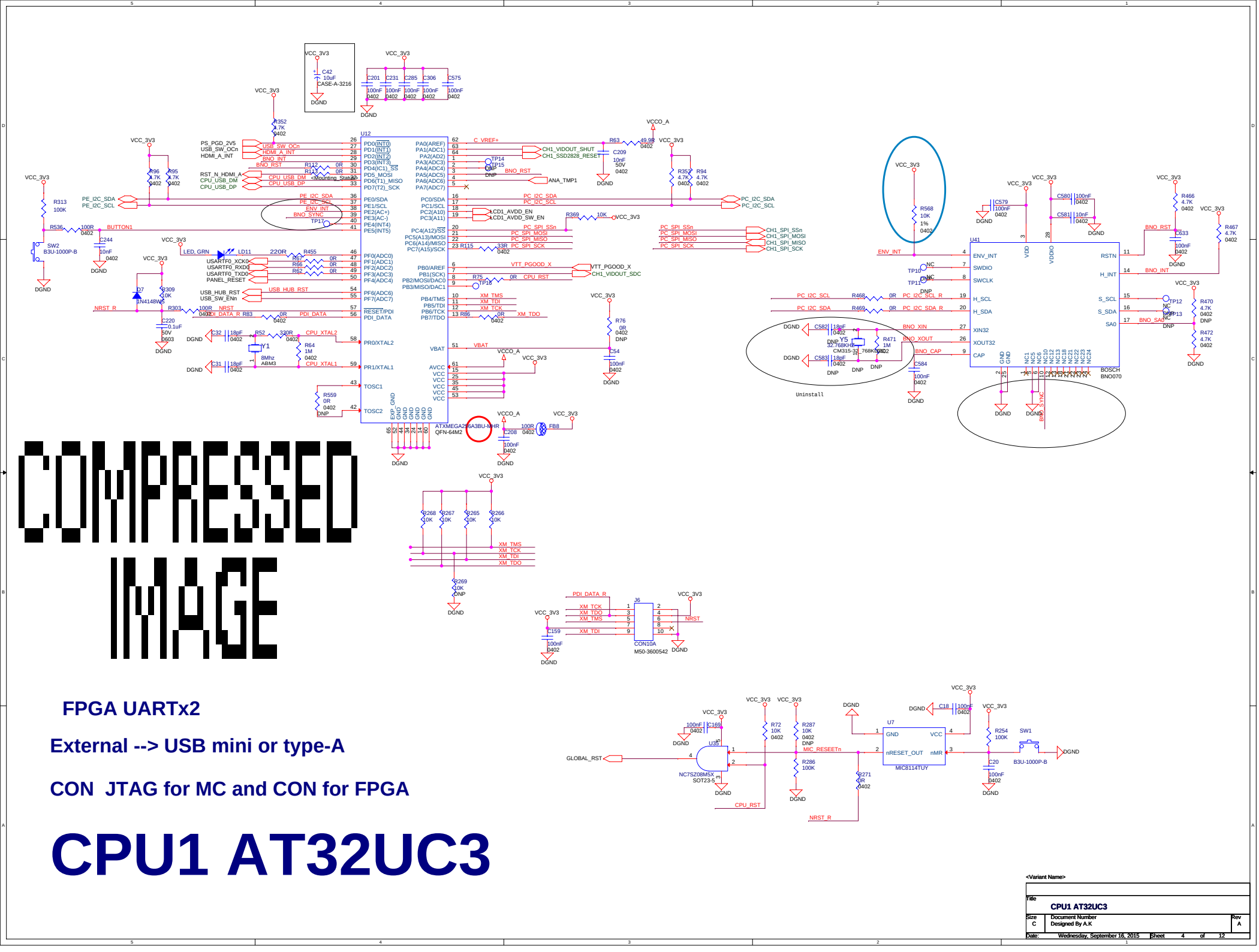


COMPRESSED IMAGE

AUDIO

<Variant Name>

Title	AUDIO	
Size C	Document Number <Doc>	Rev A
Date: Wednesday, September 16, 2015	Sheet 3 of 12	



FPGA UARTx2

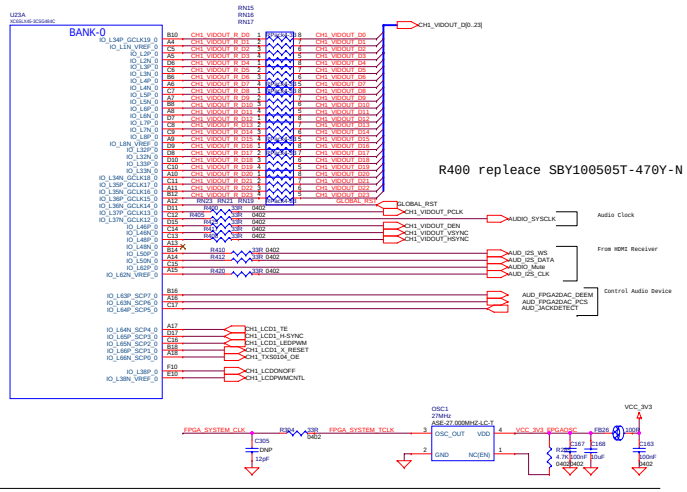
External --> USB mini or type-A

CON JTAG for MC and CON for FPGA

CPU1 AT32UC3

FPGA - Audio/Video Input from SDI Receiver (3.3V)

FPGA - Audio/Video & SDI Rx Ctrl Signals



+-50mil between groups

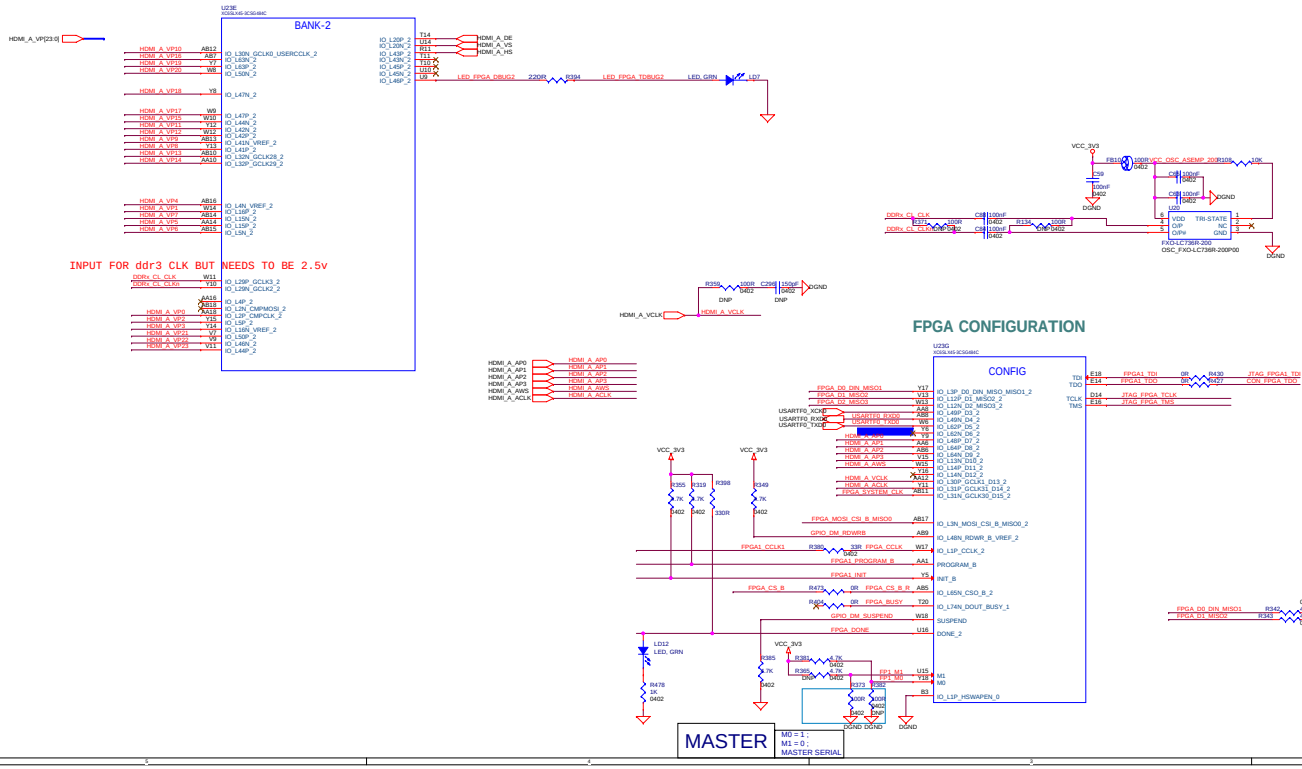
Address /CMD group:
+-20mil between signals

Control group:
+-20mil between signals

Clock group:
+-10mil between CLKn & CLKp

Data group:
+-20mil between DQ
+-10mil between LDQSn & LDQSp
DQS is longer than DQ

* Address/CMD group: BA(2:0), A(15:0), RAS, CAS, WE
* Control group: CS, CKE, ODT
* Clock group: CLK0p and CLK0n
* Data group: DQ[12:0], UDQS, LDQS



6. PIN DESCRIPTION SOIC 208-MIL, PDIP 300-MIL AND WSON 8X6-MM

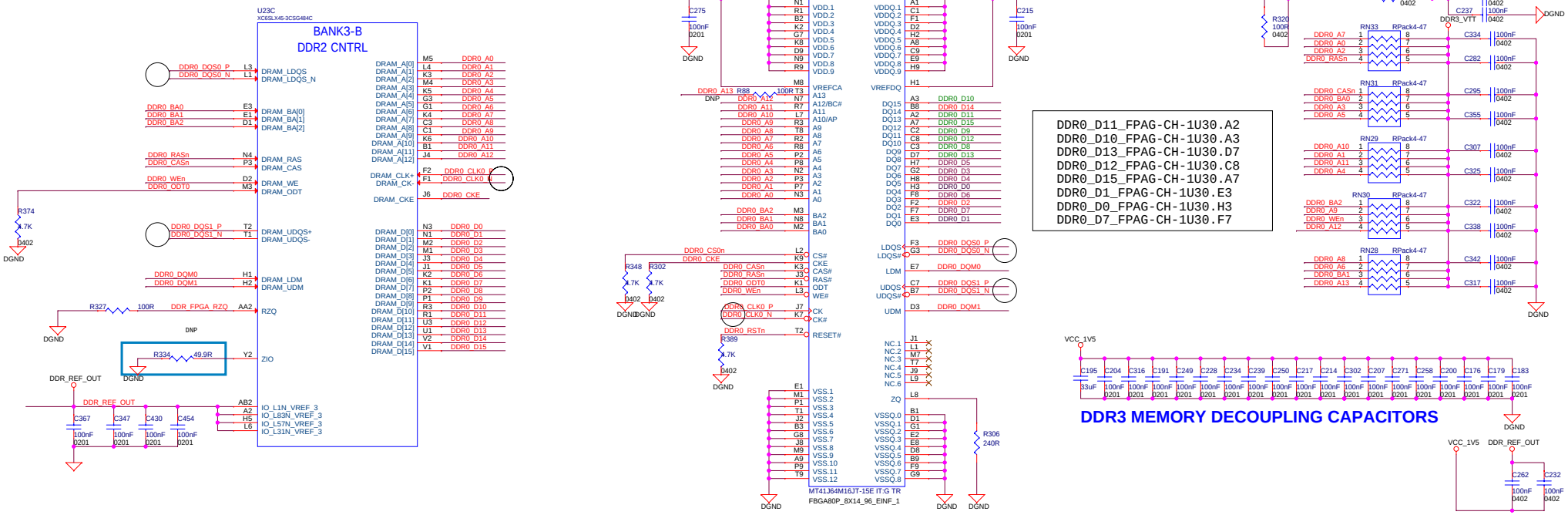
PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)[*1]
3	/WP (IO2)	I/O	Write Protect Input / Data Input Output 2[*2]
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)[*2]
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)[*2]
8	VCC		Power Supply

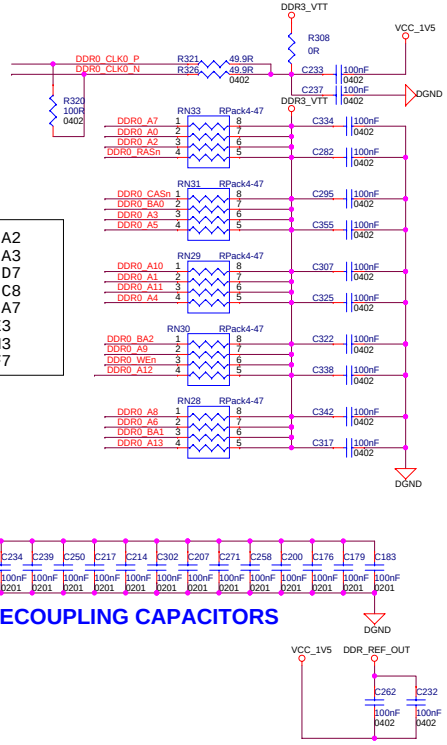
*1 IO0 and IO1 are used for Standard and Dual SPI instructions
*2 IO0 – IO3 are used for Quad SPI instructions

<Variant Name>

Title	DDR3		
Size: D	Document Number: <Doc>		Rev: A
Date: Wednesday, September 16, 2015	Sheet 5 of 12		

FPGA - DDR3 Interface (1.5V)





DDR0_D11_FPAG-CH-1U30.A2
DDR0_D10_FPAG-CH-1U30.A3
DDR0_D13_FPAG-CH-1U30.D7
DDR0_D12_FPAG-CH-1U30.C8
DDR0_D15_FPAG-CH-1U30.A7
DDR0_D1_FPAG-CH-1U30.E3
DDR0_D0_FPAG-CH-1U30.H3
DDR0_D7_FPAG-CH-1U30.F7

DDR3 MEMORY DECOUPLING CAPACITORS

+-50mil between groups

Address /CMD group:
+-20mil between signals

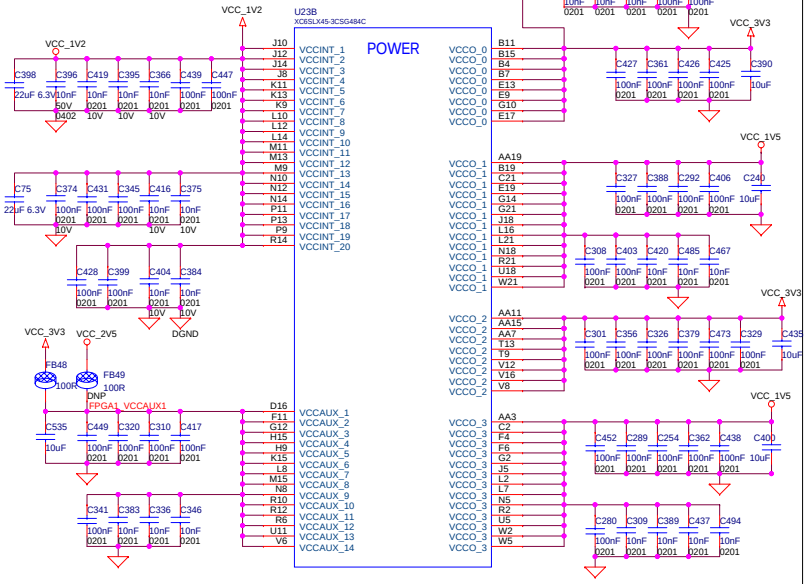
Control group:
+-20mil between signals

Clock group:
+-10mil between CLKn & CLKp

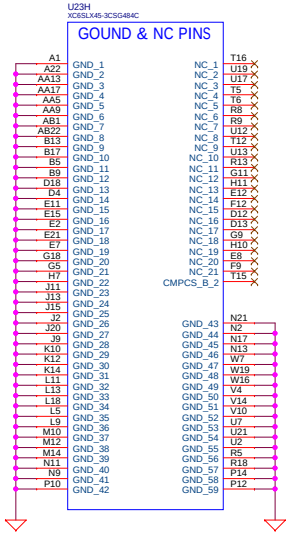
Data group:
+-20mil between DQ
+-10mil between LDQSn & LDQSp
DQS is longer than DQ

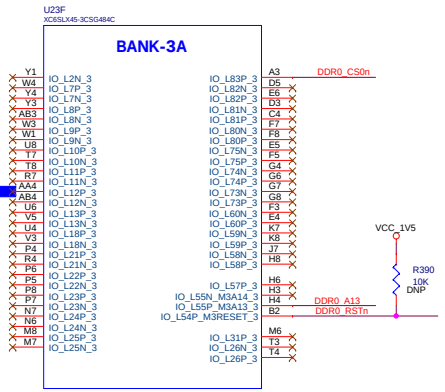
* Address/CMD group: BA(2:0), A(15:0), RAS, CAS, WE
* Control group: CS, CKE, ODT
* Clock group: CLK0p and CLK0n
* Data group: DQ[12:0], UDQS, LDQS

FPGA - Power Pins



FPGA - Ground and NC pins





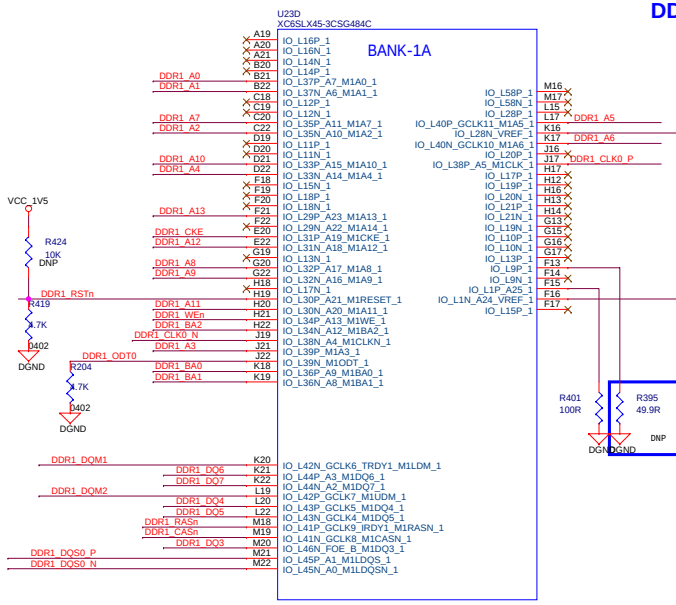
<Variant Name>

Title: FPGA

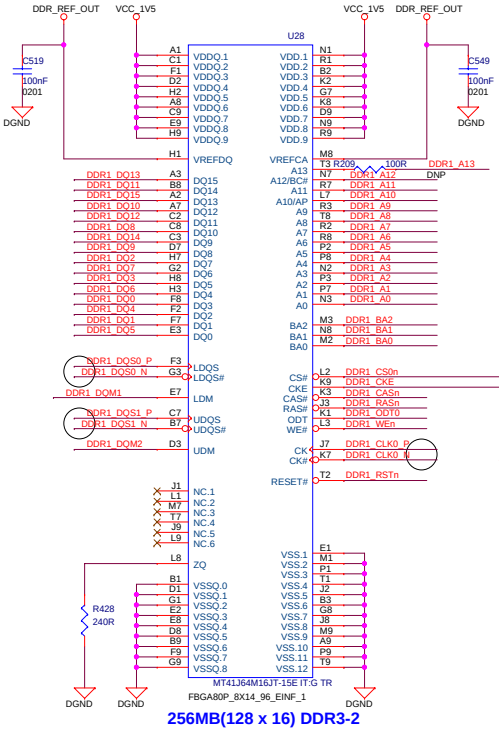
Size	Document Number	Rev
C	<Doc>	A

Date: Wednesday, September 16, 2015 Sheet 6 of 12

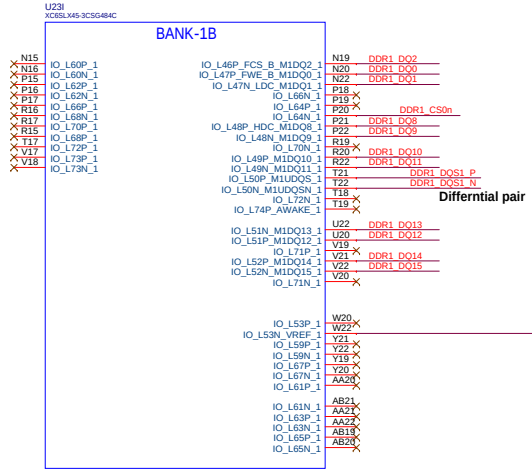
DDR0 MEMORY INTERFACE



DDR1_DQ12_FPAG-CH-1U29.C2
DDR1_DQ14_FPAG-CH-1U29.C3
DDR1_DQ15_FPAG-CH-1U29.A2
DDR1_DQ13_FPAG-CH-1U29.A3
DDR1_DQ9_FPAG-CH-1U29.D7
DDR1_DQ8_FPAG-CH-1U29.C8
DDR1_DQ11_FPAG-CH-1U29.B8
DDR1_DQ10_FPAG-CH-1U29.A7
DDR1_DQ7_FPAG-CH-1U29.G2
DDR1_DQ6_FPAG-CH-1U29.H3
DDR1_DQ4_FPAG-CH-1U29.F2
DDR1_DQ5_FPAG-CH-1U29.E3
DDR1_DQ2_FPAG-CH-1U29.H7
DDR1_DQ3_FPAG-CH-1U29.H8
DDR1_DQ0_FPAG-CH-1U29.F8

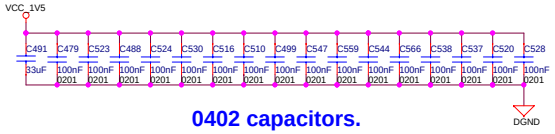


256MB(128 x 16) DDR3-2

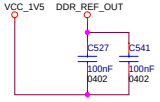


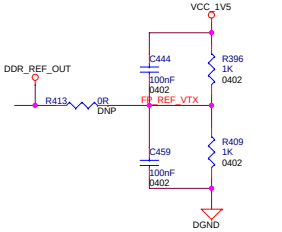
Differntial pair

256MB(128 x 16) DDR3-1

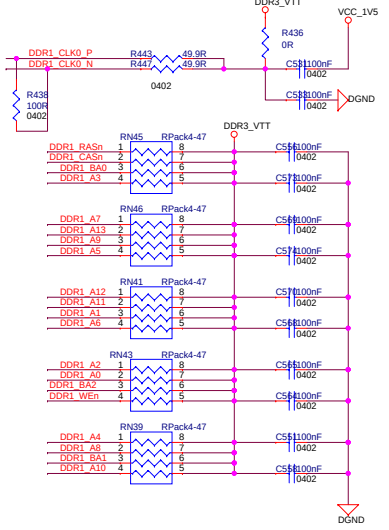


0402 capacitors.





DDR0 ADDRESS,CLK & CNTRL TERMINATION

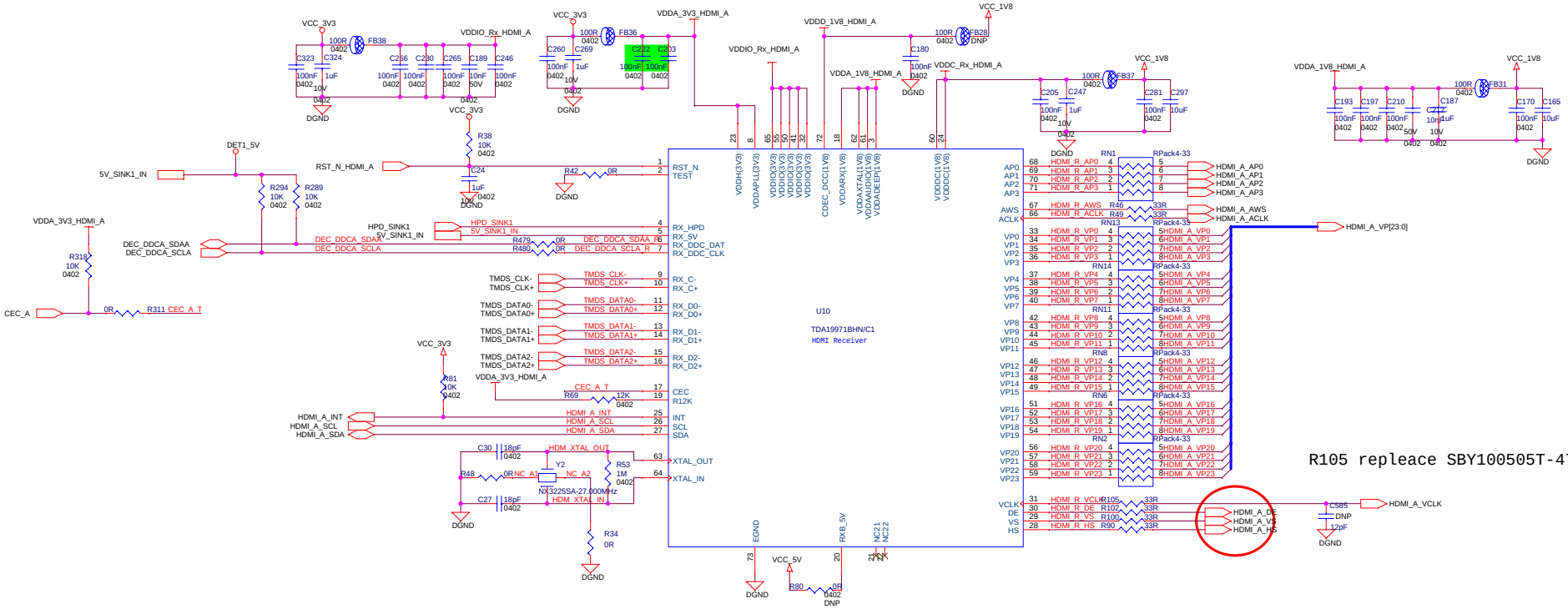


CHECK TERMINATION SIGNALS CLK AND CS

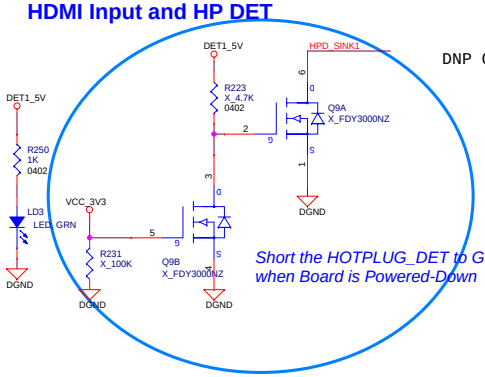
<variant_name>

Title	DDR3	
Size C	Document Number <Doc>	Rev A
Date: Wednesday, September 16, 2015	Sheet 7 of 12	

HDMI RECEIVER PORT A



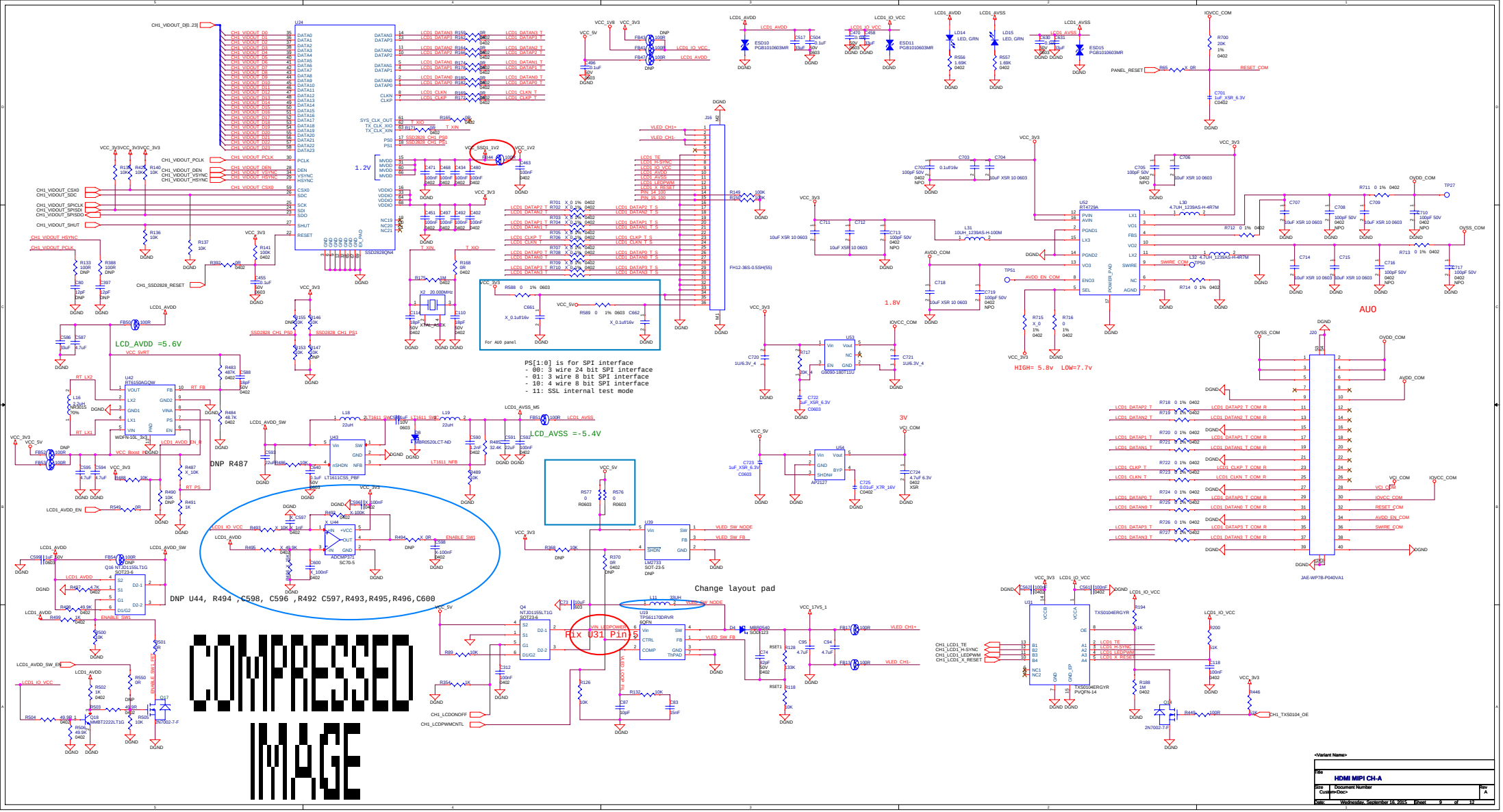
HDMI Input and HP DET



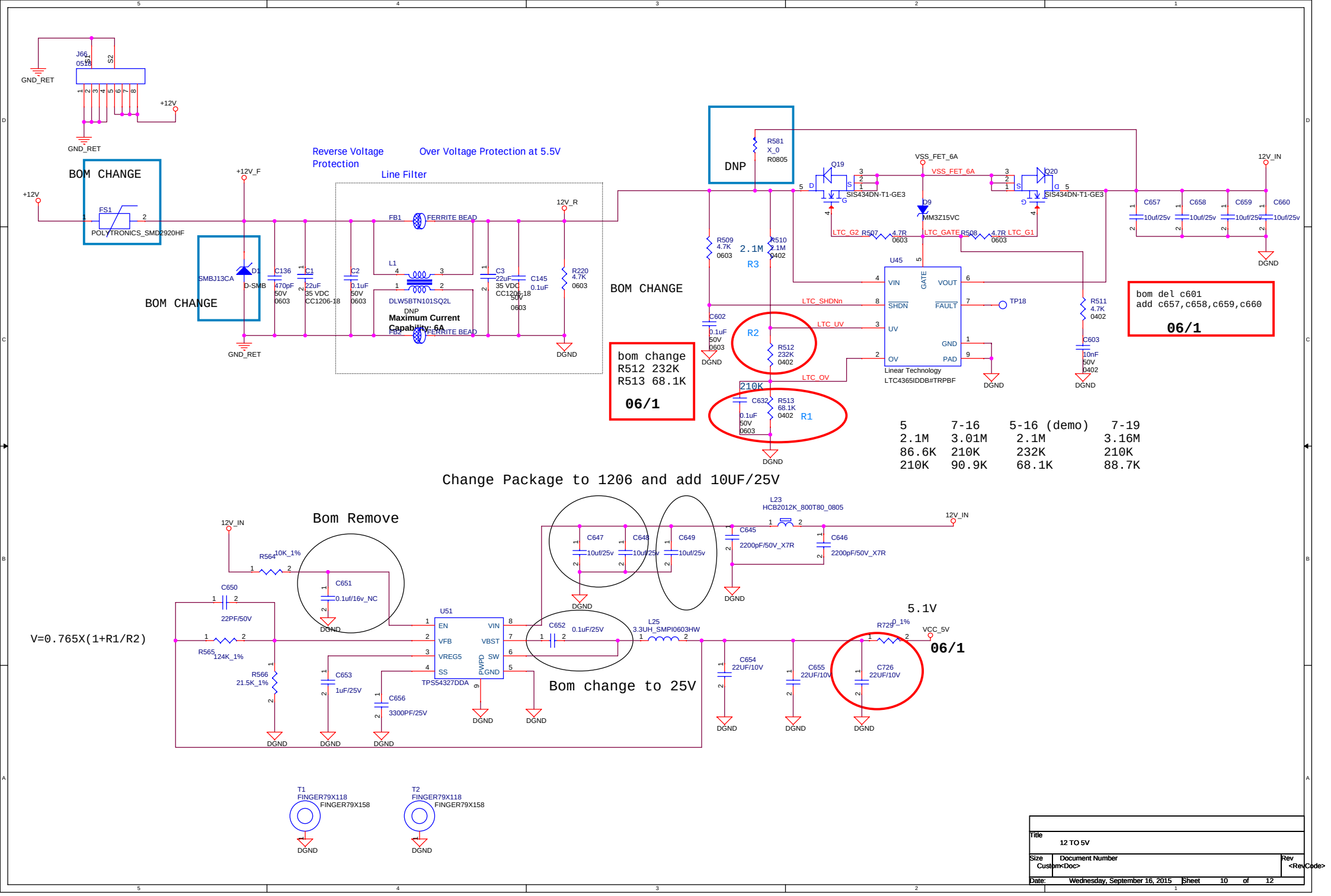
DNP Q9 ,R231 ,R223

HDMI-1

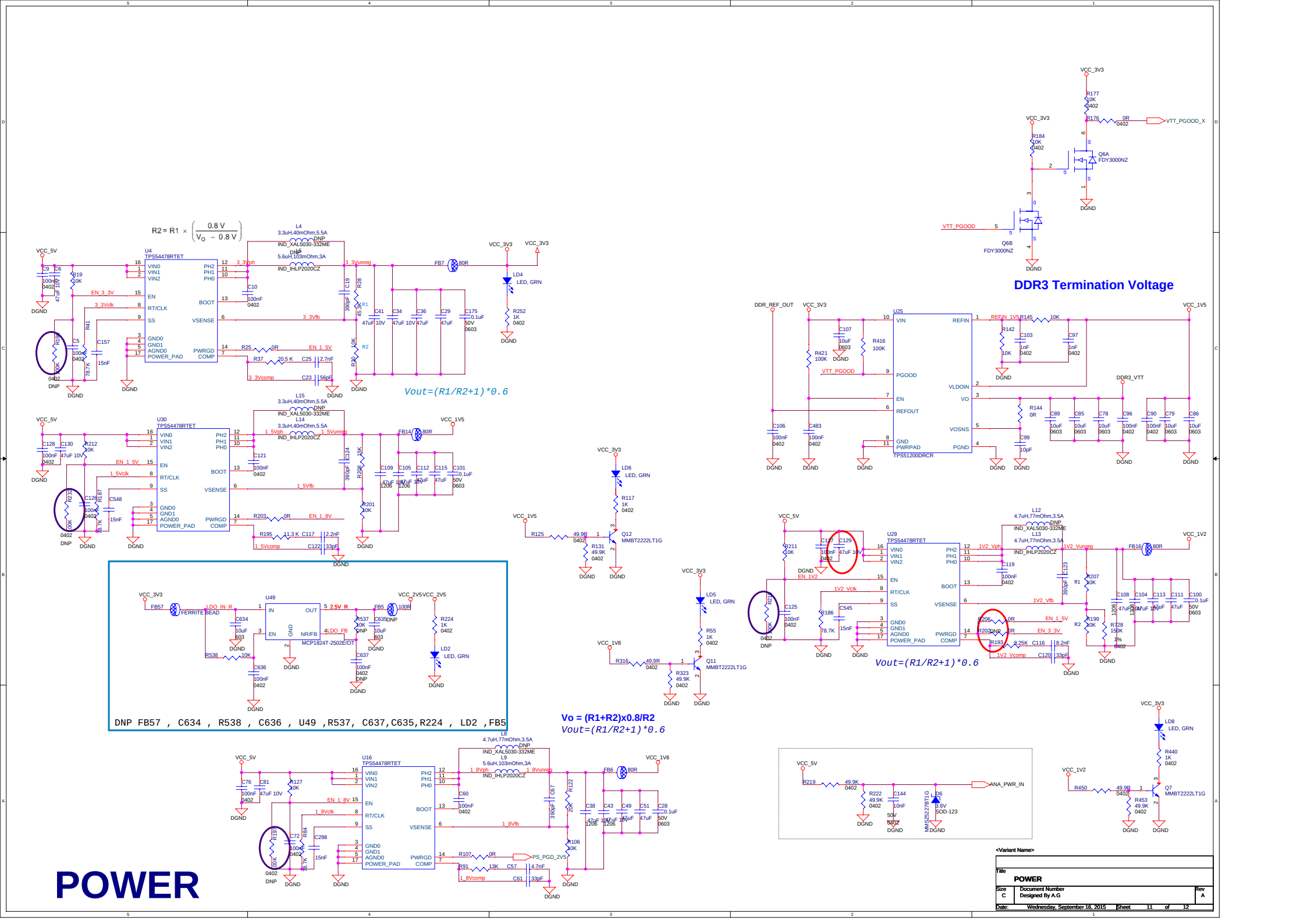
<Variant Name>		
Title: HDMI RECEIVER PORT A		
Size: C	Document Number: <Doc>	Rev: A
Date: Wednesday, September 16, 2015	Sheet 8 of 12	

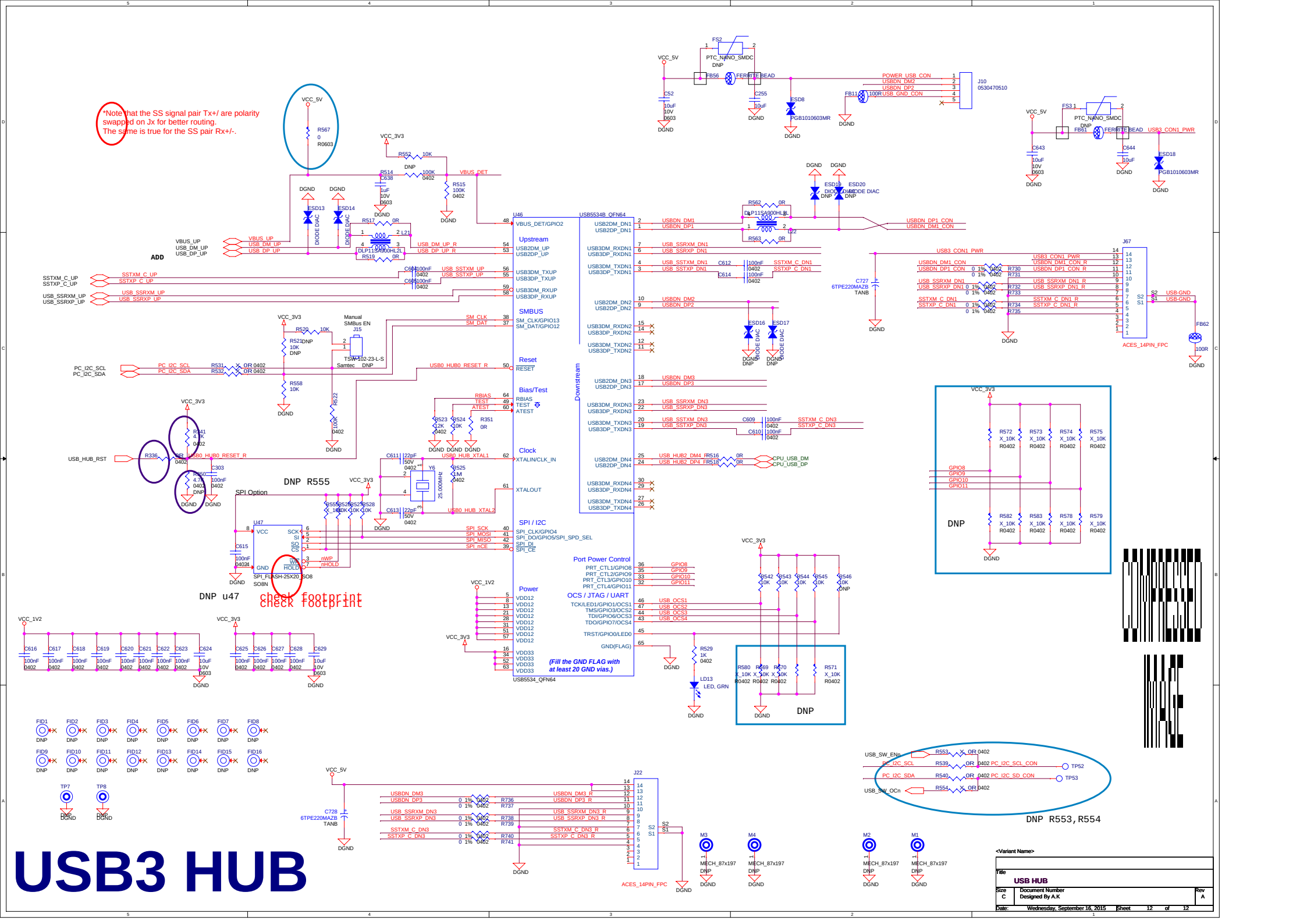


PS[1:0] is for SPI interface
- 00: 3 wire 24 bit SPI interface
- 01: 3 wire 8 bit SPI interface
- 10: 4 wire 8 bit SPI interface
- 11: SSL internal test mode
LCD_AVDD =5.6V
LCD_AVSS =-5.4V
DNP R487
DNP U44, R494 ,C598, C596 ,R492 C597,R493,R495,R496,C600
Change layout pad
Fix U31 Pin 5
HIGH= 5.8V LOW=7.7V
AUO
COMPRESSED IMAGE
<Variant Name>
Title
HDMI MIPI CH-A
Size
Custom<Doc>
Document Number
Rev
A
Date: Wednesday, September 16, 2015
Sheet 9 of 12



J66
0518
GND_RET
+12V
BOM CHANGE
FS1
POLYTRONICS_SMD2920HF
+12V_F
SMBJ13CA
D1
D-SMB
C136
470pF
50V
0603
C1
22uF
35 VDC
CC1206-18
C2
0.1uF
50V
0603
Reverse Voltage Protection
Over Voltage Protection at 5.5V
Line Filter
FB1
FERRITE BEAD
L1
DLW5BTN101SQ2L
DNP
Maximum Current Capability: 6A
FB2
FERRITE BEAD
C3
22uF
35 VDC
CC1206-18
C145
0.1uF
50V
0603
12V_R
R220
4.7K
0603
DGND
DNP
R581
X_0
R0805
Q19
SIS434DN-T1-GE3
VSS_FET_6A
Q20
SIS434DN-T1-GE3
D9
MM3Z15VC
LTC_G2
R507
4.7R
0603
LTC_GATE
R508
4.7R
0603
LTC_G1
12V_IN
C657
10uf/25v
C658
10uf/25v
C659
10uf/25v
C660
10uf/25v
R509
4.7K
0603
2.1M
R3
R510
2.1M
0402
U45
VIN
GATE
VOUT
SHDN
FAULT
UV
GND
OV
PAD
Linear Technology
LTC4365IDDB#TRPBF
TP18
LTC_SHDNn
LTC_UV
LTC_OV
R511
4.7K
0402
C603
10nF
50V
0402
C602
0.1uF
50V
0603
R2
R512
232K
0402
210K
C632
0.1uF
50V
0603
R513
68.1K
0402
R1
bom change
R512 232K
R513 68.1K
06/1
bom del c601
add c657,c658,c659,c660
06/1
5 7-16 5-16 (demo) 7-19
2.1M 3.01M 2.1M 3.16M
86.6K 210K 232K 210K
210K 90.9K 68.1K 88.7K
Change Package to 1206 and add 10UF/25V
Bom Remove
12V_IN
R564
10K_1%
C651
0.1uf/16v_NC
C650
22PF/50V
V=0.765X(1+R1/R2)
R565
124K_1%
R566
21.5K_1%
U51
EN
VFB
VREG5
SS
VIN
VBST
SW
PWPD
GND
TPS54327DDA
C653
1uF/25V
C656
3300PF/25V
C652
0.1uF/25V
Bom change to 25V
C647
10uf/25v
C648
10uf/25v
C649
10uf/25v
L23
HCB2012K_800T80_0805
C645
2200pF/50V_X7R
C646
2200pF/50V_X7R
L25
3.3UH_SMPI0603HW
C654
22UF/10V
C655
22UF/10V
5.1V
R729
0_1%
VCC_5V
C726
22UF/10V
06/1
T1
FINGER79X118
FINGER79X158
T2
FINGER79X118
FINGER79X158
Title
12 TO 5V
Size
Custom
Document Number
<Doc>
Rev
<RevCode>
Date: Wednesday, September 16, 2015
Sheet 10 of 12


R2 = R1 × (0.8 V / (V_O − 0.8 V))
U4
TPS54478RTET
VIN0
VIN1
VIN2
EN
RT/CLK
SS
GND0
GND1
AGND0
POWER_PAD
PH2
PH1
PH0
BOOT
VSENSE
PWRGD
COMP
L4
3.3uH,40mOhm,5.5A
DNP
IND_XAL5030-332ME
L5
5.6uH,103mOhm,3A
IND_IHLP2020CZ
3_3Vph
3_3Vunreg
3_3Vfb
3_3Vcomp
EN_3_3V
3_3Vclk
EN_1_5V
FB7
80R
LD4
LED, GRN
Vout=(R1/R2+1)*0.6
U30
TPS54478RTET
L15
3.3uH,40mOhm,5.5A
L14
1_5Vph
1_5Vunreg
1_5Vfb
1_5Vcomp
EN_1_8V
1_5Vclk
FB14
LD6
LED, GRN
Q12
MMBT2222LT1G
Q11
MMBT2222LT1G
U49
MCP1824T-2502E/OT
FB57
FERRITE BEAD
LDO_IN_R
2.5V_R
LDO_FB
FB5
LD5
LED, GRN
LD2
LED, GRN
DNP FB57 , C634 , R538 , C636 , U49 ,R537, C637,C635,R224 , LD2 ,FB5
Vo = (R1+R2)x0.8/R2
Vout=(R1/R2+1)*0.6
U16
TPS54478RTET
L8
4.7uH,77mOhm,3.5A
L9
5.6uH,103mOhm,3A
1_8Vph
1_8Vunreg
1_8Vfb
1_8Vcomp
EN_1_8V
1_8Vclk
FB6
PS_PGD_2V5
DDR3 Termination Voltage
U25
TPS51200DRCR
DDR_REF_OUT
REFIN
REFOUT
VLDOIN
VO
VOSNS
PGND
PGOOD
VTT_PGOOD
DDR3_VTT
U29
TPS54478RTET
L12
4.7uH,77mOhm,3.5A
L13
4.7uH,77mOhm,3.5A
1V2_Vph
1V2_Vunreg
1V2_Vclk
1V2_Vfb
1V2_Vcomp
EN_1_5V
EN_3_3V
EN_1V2
FB16
Vout=(R1/R2+1)*0.6
VTT_PGOOD_X
Q6A
FDY3000NZ
Q6B
FDY3000NZ
ANA_PWR_IN
MMSZ5227BT1G
LD8
LED, GRN
Q7
MMBT2222LT1G
POWER
<Variant Name>
Title
POWER
Size C
Document Number
Designed By A.G
Rev A
Date: Wednesday, September 16, 2015
Sheet 11 of 12


*Note that the SS signal pair Tx+/ are polarity swapped on Jx for better routing.
The same is true for the SS pair Rx+/-.
ADD
DNP R555
SPI Option
DNP u47
check footprint
check footprint
(Fill the GND FLAG with at least 20 GND vias.)
DNP R553,R554
USB3 HUB
<Variant Name>
Title
USB HUB
Size
C
Document Number
Designed By A.K
Rev
A
Date: Wednesday, September 16, 2015
Sheet 12 of 12