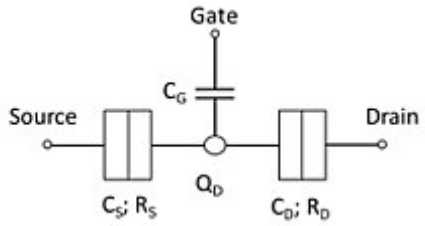
Single-electron transistor

A **single-electron transistor** (**SET**) is a sensitive electronic device based on the Coulomb blockade effect. In this device the electrons flow through a tunnel junction between source/drain to a quantum dot (conductive island). Moreover, the electrical potential of the island can be tuned by a third electrode, known as the gate, which is capacitively coupled to the island. The conductive island is sandwiched between two tunnel junctions, [1] which are modeled by a capacitor (C_D and C_S) and a resistor (R_D and R_S) in parallel.



Schematic of a basic SET and its internal electrical components.

Contents

History

When David Thouless pointed out in 1977 that the size of a conductor, if made small enough, will affect the electronic properties of the conductor, a new subfield of condensed matter physics was started.[2] The research that followed during the 1980s was known as the mesoscopic physics, based on the submicron-size systems investigated.[3] This was the starting point of the research related to the single-electron transistor.

The first single-electron transistor based on the Coulomb blockade was reported in 1986 by Soviet scientists K. K. Likharev and D. V. Averin.[4] A couple of years later, T. Fulton and G. Dolan at Bell Labs in the US fabricated and demonstrated how such a device works.[5] In 1992 Marc A. Kastner demonstrated the importance of the energy levels of the quantum dot.[6] In the late 1990s and early 2000s, Russian physicists S. P. Gubin, V. V. Kolesov, E. S. Soldatov, A. S. Trifonov, V. V. Khanin, G. B. Khomutov, and S. A. Yakovenko were the first ones to ever make a molecule based SET operational at room temperature.[7]

Relevance

The increasing relevance of the Internet of things and the healthcare applications give more relevant impact to the electronic device power consumption. For this purpose, ultra-low power consumption is one of the main research topics into the current electronics world. The amazing

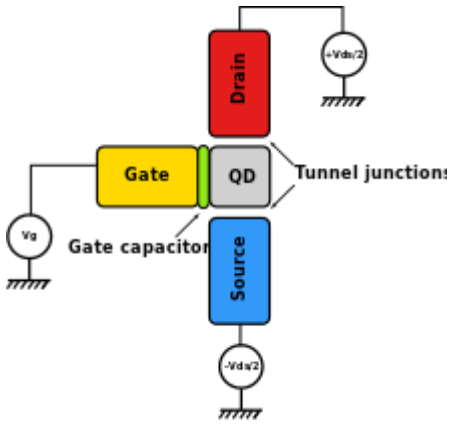
number of tiny computers used in the day-to-day world (e.g. mobile phones and home electronics) requires a significant power consumption level of the implemented devices. In this scenario, the SET has appeared as a suitable candidate to achieve this low power range with high level of device integration.

Applicable areas include: super-sensitive electrometers, single-electron spectroscopy, DC current standards, temperature standards, detection of infrared radiation, voltage state logics, charge state logics, programmable single-electron transistor logic.[8]

Device

Principle

The SET has, like the FET, three electrodes: source, drain, and a gate. The main technological difference between the transistor types is in the channel concept. While the channel changes from insulated to conductive with applied gate voltage in the FET, the SET is always insulated. The source and drain are coupled through two tunnel junctions, separated by a metallic or semiconductor-based quantum nanodot (QD),[9] also known as the "island". The electrical potential of the QD can be tuned with the capacitively coupled gate electrode to alter the resistance, by applying a positive voltage the QD will change from blocking to non-blocking state and electrons will start tunnelling to the QD. This phenomenon is known as the Coulomb blockade.



Schematic diagram of a single-electron transistor.

The current, I, from source to drain follows Ohm's law when V_{SD} is applied, and it equals $\frac{V_{\mathrm{SD}}}{R}$, where the main contribution of the resistance, R, comes from the tunnelling effects when electrons move from source to QD, and from QD to drain. V_{G} regulates the resistance of the QD, which regulates the current. This is the exact same behaviour as in regular FETs. However, when moving away from the macroscopic scale, the quantum effects will affect the current, I.

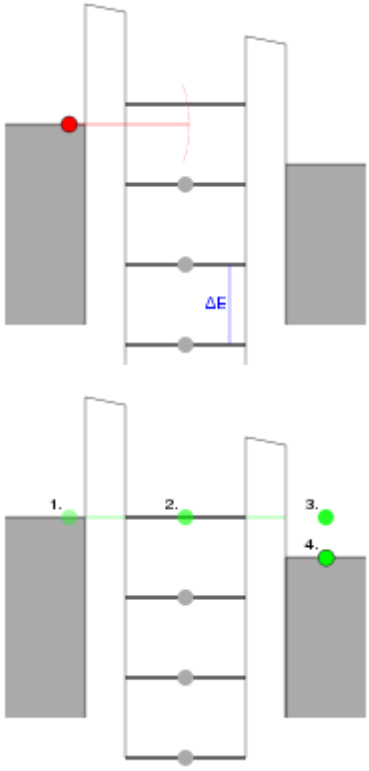
In the blocking state all lower energy levels are occupied at the QD and no unoccupied level is within tunnelling range of electrons originating from the source (green 1.). When an electron arrives at the QD (2.) in the non-blocking state it will fill the lowest available vacant energy level, which will raise the energy barrier of the QD, taking it out of tunnelling distance once again. The electron will continue to tunnel through the second tunnel junction (3.), after which it scatters inelastically and reaches the drain electrode Fermi level (4.).

The energy levels of the QD are evenly spaced with a separation of ΔE. This gives rise to a self-capacitance C of the island, defined as: $C = \frac{e^2}{\Delta E}$. To achieve the Coulomb blockade, three criteria need to be met:[10]

1. The bias voltage must be lower than the elementary charge divided by the self-capacitance of the island: $V_{\mathrm{bias}} < \frac{e}{C}$
2. The thermal energy in the source contact plus the thermal energy in the island, i.e. $k_{\mathrm{B}}T$, must be below the charging energy: $k_{\mathrm{B}}T \ll \frac{e^2}{2C}$, otherwise the electron will be able to pass the QD via thermal excitation.

3. The tunnelling resistance, R_t, should be greater than $\frac{h}{e^2}$, which is derived from Heisenberg's uncertainty principle.[11] $\Delta E \Delta t = \left(\frac{e^2}{2C}\right)(R_T C) > h$, where $(R_T C)$ corresponds to the tunnelling time τ and is shown as $C_S R_S$ and $C_D R_D$ in the schematic figure of the internal electrical components of the SET. The time (τ) of electron tunnelling through the barrier is assumed to be negligibly small in comparison with the other time scales. This assumption is valid for tunnel barriers used in single-electron devices of practical interest, where $\tau \approx 10^{-15}\mathrm{s}$.

If the resistance of all the tunnel barriers of the system is much higher than the quantum resistance $R_t = \frac{h}{e^2} = 25.813\,\mathrm{k\Omega}$, it is enough to confine the electrons to the island, and it is safe to ignore coherent quantum processes consisting of several simultaneous tunnelling events, i.e. co-tunnelling.



Left to right: energy levels of source, island and drain in a single-electron transistor for the blocking state (upper part) and transmitting state (lower part).

Theory

The background charge of the dielectric surrounding the QD is indicated by q_0. n_S and n_D denote the number of electrons tunnelling through the two tunnel junctions and the total number of electrons is n. The corresponding charges at the tunnel junctions can be written as:

$$q_S = C_S V_S$$

$$q_D = C_D V_D$$

$$q = q_D - q_S + q_0 = -ne + q_0,$$

where C_S and C_D are the parasitic leakage capacities of the tunnel junctions. Given the bias voltage, $V_{bias} = V_S + V_D$, you can solve the voltages at the tunnel junctions:

$$V_S = \frac{C_D V_{bias} + ne - q_0}{C_S + C_D},$$

$$V_D = \frac{C_S V_{bias} - ne + q_0}{C_S + C_D}.$$

The electrostatic energy of a double-connected tunnel junction (like the one in the schematical picture) will be

$$E_C = \frac{q_S^2}{2C_S} + \frac{q_D^2}{2C_D} = \frac{C_S C_D V_{bias}^2 + (ne - q_0)^2}{2(C_S + C_D)}.$$

The work performed during electron tunnelling through the first and second transitions will be:

$$W_S = \frac{n_S e V_{bias} C_D}{C_S + C_D},$$

$$W_{\mathrm{D}} = \frac{n_{\mathrm{D}} e V_{\mathrm{bias}} C_{\mathrm{S}}}{C_{\mathrm{S}} + C_{\mathrm{D}}}.$$

Given the standard definition of free energy in the form:

$$F = E_{\mathrm{tot}} - W,$$

where $E_{\mathrm{tot}} = E_C = \Delta E_F + E_N$, we find the free energy of a SET as:

$$F(n, n_{\mathrm{S}}, n_{\mathrm{D}}) = E_C - W = \frac{1}{C_{\mathrm{S}} + C_{\mathrm{D}}} \left(\frac{1}{2} C_{\mathrm{S}} C_{\mathrm{D}} V_{\mathrm{bias}}^2 + (ne - q_0)^2 + e V_{\mathrm{bias}} C_{\mathrm{S}} n_{\mathrm{D}} + C_{\mathrm{D}} n_{\mathrm{S}} \right).$$

For further consideration, it is necessary to know the change in free energy at zero temperatures at both tunnel junctions:

$$\Delta F_{\mathrm{S}}^{\pm} = F(n \pm 1, n_{\mathrm{S}} \pm 1, n_{\mathrm{D}}) - F(n, n_{\mathrm{S}}, n_{\mathrm{D}}) = \frac{e}{C_{\mathrm{S}} + C_{\mathrm{D}}} \left(\frac{e}{2} \pm (V_{\mathrm{bias}} C_{\mathrm{D}} + ne - q_0) \right),$$

$$\Delta F_{\mathrm{D}}^{\pm} = F(n \pm 1, n_{\mathrm{S}}, n_{\mathrm{D}} \pm 1) - F(n, n_{\mathrm{S}}, n_{\mathrm{D}}) = \frac{e}{C_{\mathrm{S}} + C_{\mathrm{D}}} \left(\frac{e}{2} \pm (V_{\mathrm{bias}} C_{\mathrm{S}} + ne - q_0) \right),$$

The probability of a tunnel transition will be high when the change in free energy is negative. The main term in the expressions above determines a positive value of ΔF as long as the applied voltage V_{bias} will not exceed the threshold value, which depends on the smallest capacity in the system. In general, for an uncharged QD ($n = 0$ and $q_0 = 0$) for symmetric transitions ($C_{\mathrm{S}} = C_{\mathrm{D}} = C$) we have the condition

$$V_{\mathrm{th}} = |V_{\mathrm{bias}}| \geq \frac{e}{2C},$$

(that is, the threshold voltage is reduced by half compared with a single transition).

When the applied voltage is zero, the Fermi level at the metal electrodes will be inside the energy gap. When the voltage increases to the threshold value, tunnelling from left to right occurs, and when the reversed voltage increases above the threshold level, tunnelling from right to left occurs.

The existence of the Coulomb blockade is clearly visible in the current–voltage characteristic of a SET (a graph showing how the drain current depends on the gate voltage). At low gate voltages (in absolute value), the drain current will be zero, and when the voltage increases above the threshold, the transitions behave like an ohmic resistance (both transitions have the same permeability) and the current increases linearly. The background charge in a dielectric can not only reduce, but completely block the Coulomb blockade. $q_0 = \pm(0.5 + m)e$.

In the case where the permeability of the tunnel barriers is very different $(R_{T1} \gg R_{T2} = R_T)$, a stepwise I-V characteristic of the SET arises. An electron tunnels to the island through the first transition and is retained on it, due to the high tunnel resistance of the second transition. After a certain period of time, the electron tunnels through the second transition, however, this process causes a second electron to tunnel to the island through the first transition. Therefore, most of the time the island is charged in excess of one charge. For the case with the inverse dependence of permeability $(R_{T1} \ll R_{T2} = R_T)$, the island will be unpopulated and its charge will decrease stepwise. Only now can we understand the principle of operation of a SET. Its equivalent circuit can be represented as two tunnel junctions connected in series via the QD, perpendicular to the tunnel junctions is another control electrode (gate) connected. The gate electrode is connected to

the island through a control tank C_{G}. The gate electrode can change the background charge in the dielectric, since the gate additionally polarizes the island so that the island charge becomes equal to

$$q = -ne + q_0 + C_{\mathrm{G}}(V_{\mathrm{G}} - V_2).$$

Substituting this value into the formulas found above, we find new values for the voltages at the transitions:

$$V_{\mathrm{S}} = \frac{(C_{\mathrm{D}} + C_{\mathrm{G}})V_{\mathrm{bias}} - C_{\mathrm{G}}V_{\mathrm{G}} + ne - q_0}{C_{\mathrm{S}} + C_{\mathrm{D}}},$$

$$V_{\mathrm{D}} = \frac{C_{\mathrm{S}}V_{\mathrm{bias}} + C_{\mathrm{G}}V_{\mathrm{G}} - ne + q_0}{C_{\mathrm{S}} + C_{\mathrm{D}}},$$

The electrostatic energy should include the energy stored on the gate capacitor, and the work performed by the voltage on the gate should be taken into account in the free energy:

$$\Delta F_{\mathrm{S}}^{\pm} = \frac{e}{C_{\mathrm{S}} + C_{\mathrm{D}}}\left(\frac{e}{2} \pm V_{\mathrm{bias}}(C_{\mathrm{D}} + C_{\mathrm{G}}) - V_{\mathrm{G}}C_{\mathrm{G}} + ne + q_0\right),$$

$$\Delta F_{\mathrm{D}}^{\pm} = \frac{e}{C_{\mathrm{S}} + C_{\mathrm{D}}}\left(\frac{e}{2} \pm V_{\mathrm{bias}}C_{\mathrm{S}} + V_{\mathrm{G}}C_{\mathrm{G}} - ne + q_0\right).$$

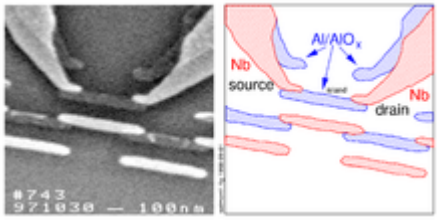
At zero temperatures, only transitions with negative free energy are allowed: $\Delta F_{\mathrm{S}} < 0$ or $\Delta F_{\mathrm{D}} < 0$. These conditions can be used to find areas of stability in the plane $V_{\mathrm{bias}} - V_{\mathrm{G}}$.

With increasing voltage at the gate electrode, when the supply voltage is maintainted below the voltage of the Coulomb blockade (i.e. $V_{\mathrm{bias}} < \frac{e}{C_{\mathrm{S}}+C_{\mathrm{D}}}$), the drain output current will oscillate with a period $\frac{e}{C_{\mathrm{S}}+C_{\mathrm{D}}}$. These areas correspond to failures in the field of stability. The oscillations of the tunnelling current occur in time, and the oscillations in two series-connected junctions have a periodicity in the gate control voltage. The thermal broadening of the oscillations increases to a large extent with increasing temperature.

Temperature dependence

Various materials have successfully been tested when creating single-electron transistors. However, temperature is a huge factor limiting implementation in available electronical devices. Most of the metallic-based SETs only work at extremely low temperatures.

As mentioned in bullet 2 in the list above: the electrostatic charging energy must be greater than $k_{\mathrm{B}}T$ to prevent thermal fluctuations affecting the Coulomb blockade. This in turn implies that the maximum allowed island capacitance is inversely proportional to the temperature, and needs to be below 1 aF to make the device operational at room temperature.

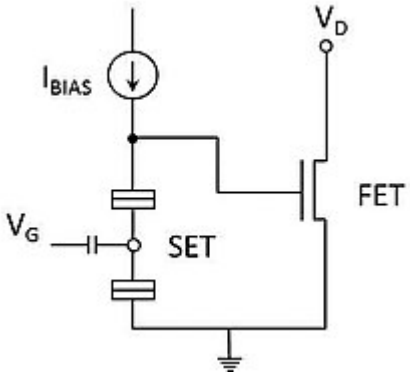


Single-electron transistor with niobium leads and aluminium island.

The island capacitance is a function of the QD size, and a QD diameter smaller than 10 nm is preferable when aiming for operation at room temperature. This in turn puts huge restraints on the manufacturability of integrated circuits because of reproducibility issues.

CMOS compatibility

The level of the electrical current of the SET can be amplified enough to work with available CMOS technology by generating a hybrid SET-FET device.[12][13]



Hybrid SET-FET circuit.

The EU funded, in 2016, project IONS4SET (#688072)[14] looks for the manufacturability of SET-FET circuits operative at room temperature. The main goal of this project is to design a SET-manufacturability process-flow for large-scale operations seeking to extend the use of the hybrid Set-CMOS architectures. To assure room temperature operation, single dots of diameters below 5 nm have to be fabricated and located between source and drain with tunnel distances of a few nanometers.[15] Up to now there is no reliable process-flow to manufacture a hybrid SET-FET circuit operative at room temperature. In this context, this EU project explores a more feasible way to manufacture the SET-FET circuit by using pillar dimensions of approximately 10 nm.[16]

See also

- Coulomb blockade
- MOSFET
- Transistor model

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