



PC0/TIM4_ETR/FSMC_NBL0/DCML_D2/EVENTOUT	97	X
PE1/FSMC_NBL1/DCML_D3/EVENTOUT	98	X
PE2/TRACEL1/FSMC_A23/ETH_MIL_TXD3/EVENTOUT	1	X
PE3/TRACED0/FSMC_A19/EVENTOUT	2	X
PE4/TRACED1/FSMC_A20/DCML_D4/EVENTOUT	3	X
PE5/TRACED2/FSMC_A21/TIM9_CH1/DCML_D5/EVENTOUT	4	X
PE6/TRACED3/FSMC_A22/TIM9_CH2/DCML_D7/EVENTOUT	5	X
PE7/FSMC_D4/TIM1_ETR/EVENTOUT	38	X
PE8/FSMC_D5/TIM1_CH3/EVENTOUT	39	X
PE9/FSMC_D6/TIM1_CH1/EVENTOUT	40	X
PE10/FSMC_D7/TIM1_CH2/EVENTOUT	41	X
PE11/FSMC_D8/TIM1_CH2/EVENTOUT	42	X
PE12/FSMC_D9/TIM1_CH3/EVENTOUT	43	X
PE13/FSMC_D10/TIM1_CH3/EVENTOUT	44	X
PE14/FSMC_D11/TIM1_CH4/EVENTOUT	45	X
PE15/FSMC_D12/TIM1_BKIN/EVENTOUT	46	X
PD0/FSMC_D2/CAN1_RX/EVENTOUT	81	X
PD1/FSMC_D3/CAN1_TX/EVENTOUT	82	X
PD2/TIM3_ETR/UART5_RX/SIO0_CK0/DCML_D11/EVENTOUT	83	X
PD3/FSMC_CLK/USART2_CTS/EVENTOUT	84	X
PD4/FSMC_NDE/USART2_RTS/EVENTOUT	85	X
PD5/FSMC_NWE/USART2_TX/EVENTOUT	86	X
PD6/FSMC_NWAIT/USART2_RX/EVENTOUT	87	X
PD7/USART2_CK/FSMC_NEL/FSMC_KCE2/EVENTOUT	88	X
PD8/FSMC_D15/USART2_TX/EVENTOUT	89	X
PD9/FSMC_D14/USART2_RX/EVENTOUT	90	X
PD10/FSMC_D15/USART2_CK/EVENTOUT	91	X
PD11/FSMC_CLE/FSMC_A16/USART3_CTS/EVENTOUT	92	X
PD12/FSMC_A17/TIM4_CH1/USART3_RTS/EVENTOUT	93	X
PD13/FSMC_A18/TIM4_CH2/EVENTOUT	94	X
PD14/FSMC_D0/TIM4_CH3/EVENTOUT/EVENTOUT	95	X
PD15/FSMC_D1/TIM4_CH4/EVENTOUT	96	X

