



» **DATA SHEET**  
*(DOC No. HX8394-D-DS )*

» **HX8394-D**

800RGB x 1280 dots, 16.7M color  
TFT Mobile Single Chip Driver  
*Preliminary version 00, October 2013*

# >> HX8394-D

800RGB x 1280 dots, 16.7M color,  
TFT Mobile Single Chip Driver



Himax Technologies, Inc.  
<http://www.himax.com.tw>

## ***Revision History***

*Preliminary version 00*

Version	Date	Description of Changes
00.00	2013/07/11	New setup

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## 1. General Description

This document describes Himax's HX8394-D supports WXGA resolution driving controller. The HX8394-D is designed to provide a single-chip solution that combines source driver control, gate driver control and power supply circuit to drive a TFT dot matrix LCD with 800RGB x 1280 dots at maximum.

The HX8394-D can be operated in low-voltage condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8394-D also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8394-D supports several interface modes, including MIPI DBI Type C interface mode and MIPI DSI (Display Serial Interface) interface mode.

The HX8394-D is suitable for any small portable battery-driven and long-term driving products, such as cellular phones, tablet and other mobile devices.

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## 2. Features

### 2.1 Display

- Single chip solution for a WXGA type TFT LCD display
- Resolution:
  - 800RGB x (480 + (8 x NL))
  - 768RGB x (480 + (8 x NL))
  - 720RGB x (480 + (8 x NL))
  - 640RGB x (480 + (8 x NL))
  - 600RGB x (480 + (8 x NL))
- Display color modes
  - Full color mode:
    - 16.7M colours (24-bit 8(R):8(G):8(B))
  - Reduce color mode:
    - 262k colours (18-bit 6(R):6(G):6(B))
    - 65k colours (16-bit 5(R):6(G):5(B))
    - 8 colors (Idle mode on): 8 colors (3-bit binary mode)

### 2.2 Display module

- Support 2402 source channel outputs
- Gate driver control signals for GIP
- Supports 1-dot / 2-dot / 4-dot / 8-dot / Zig-Zag / Column inversion
- Output voltage level
  - Positive source output voltage level: VSPR to VSSA.
  - Negative source output voltage level: VSNR to VSSA.
  - Positive gate driver output voltage level: VGH to VSSA.
  - Negative gate driver output voltage level: VGL to VSSA.
  - VCOM= -4V ~ -0.3V, each step=10mV

## 2.3 Display / control interface

- Display interface types supported
  - MIPI-DSI (Display Serial Interface) interface
    - Support DSI Version 1.1
    - Support D-PHY version 1.1

## 2.4 Input power

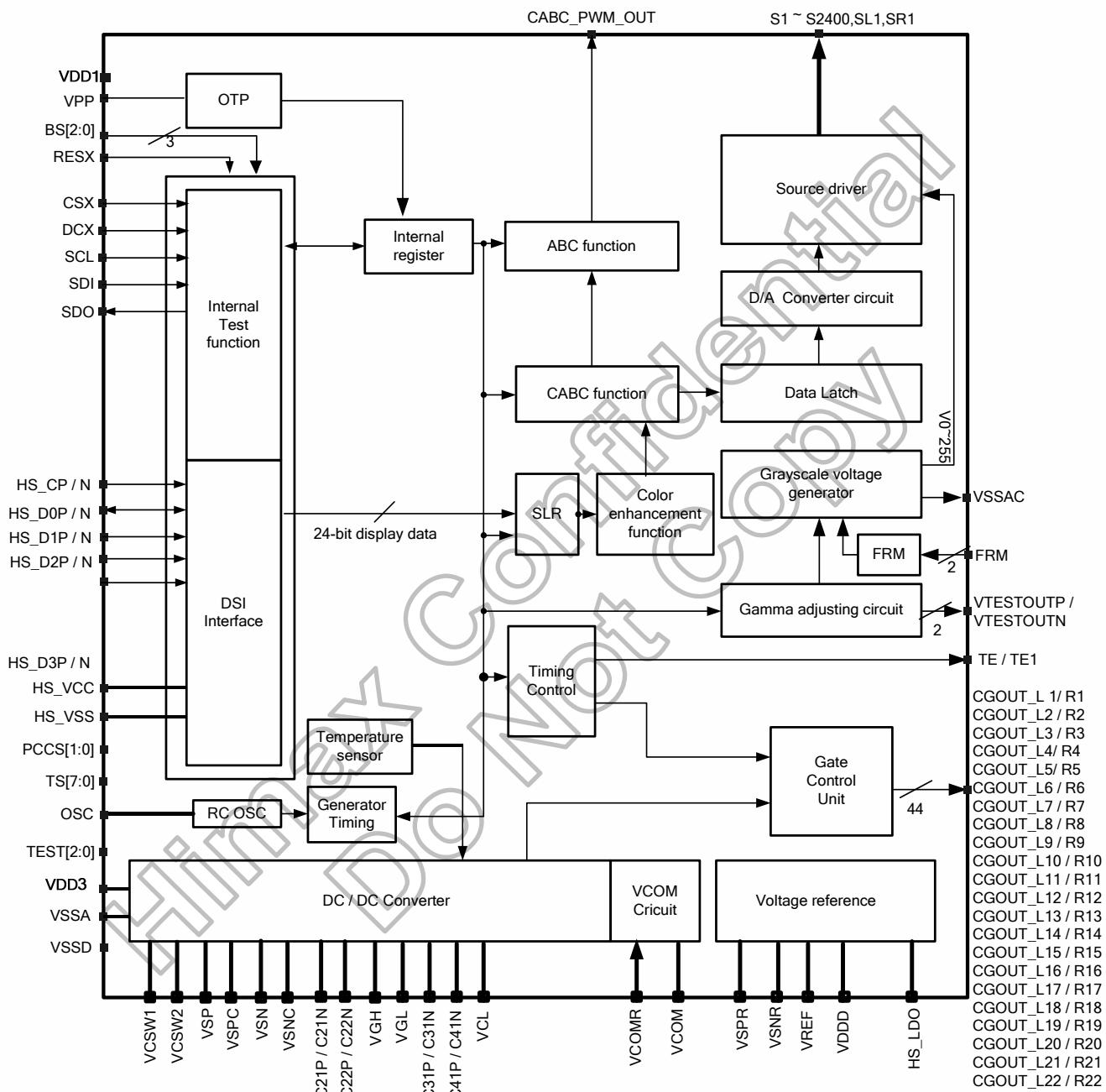
- Logic and interface power supply (VDD1): 1.65V to 3.3V
- Analog power supply (VDD3): 2.5V to 6.5V
  - (For PCCS[1:0]=10, VDD3 range is 2.5V ~ 3.3V)
  - For PCCS[1:0]=00, 01 and 11, VDD3 range is 2.5V ~6.5V)
- Positive source driver power (External input mode VSP): 3.0 to 6.5V
- Negative source driver power (External input mode VSN): -3.0 to -6.5V
- High speed interface power supply (HS\_VCC): 1.65V to 3.3V
- OTP programming voltage (VPP): 7.5V ± 0.2V
- VGH,VGL: VGH-VGL<32V

## 2.5 Miscellaneous

- Software programmable color depth mode
- Oscillator for display clock generation
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Proprietary multi phase driving for lower power consumption
- GAS function for preventing image sticking when abnormal power off
- Optimized layout for COG assembly
- Temperature range: -40 to +85 °C
- Support inversion mode
- DC/DC converter for source
- Support DC COM driving
- VCOM voltage generator
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 3 times MTP for VCOM setting, ID setting
- Support Content Adaptive Brightness Control(CABC) function
- Support DGC (Digital Gamma Correction) function
- Support CE (Color Enhancement) function
- Support SLR (SunLight Readable) function
- Support Temperature sensor function
- FRM

### 3. Device Overview

#### 3.1 Block diagram



### 3.2 Pin description

Host interface pins																																																																																																												
Signals	I/O	Pin no.	Connected with	Description																																																																																																								
BS2 ~ BS0	I	6	VSSD / VDD1	These pins must be connected to VDD1 or VSSD to set 1 or 0. BS2 ~ BS0 are used for the combination of polarity swap and data lane swap of DS1.																																																																																																								
				<table border="1"> <tr> <td>BS[2:0]</td><td>HS_D0N</td><td>HS_D0P</td><td>HS_D1N</td><td>HS_D1P</td><td>HS_CN</td><td>HS_CP</td><td>HS_D2N</td><td>HS_D2P</td><td>HS_D3N</td><td>HS_D3P</td></tr> <tr> <td>"000"</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td><td>CN</td><td>CP</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td></tr> <tr> <td>"001"</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>CP</td><td>CN</td><td>C1P</td><td>C1N</td><td>D0P</td><td>D0N</td></tr> <tr> <td>"010"</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>CN</td><td>CP</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td></tr> <tr> <td>"011"</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>CP</td><td>CN</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr> <tr> <td>"100"</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>CN</td><td>CP</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td></tr> <tr> <td>"101"</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>CP</td><td>CN</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr> <tr> <td>"110"</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td><td>CN</td><td>CP</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td></tr> <tr> <td>"111"</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>CP</td><td>CN</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr> </table>						BS[2:0]	HS_D0N	HS_D0P	HS_D1N	HS_D1P	HS_CN	HS_CP	HS_D2N	HS_D2P	HS_D3N	HS_D3P	"000"	D3N	D3P	D2N	D2P	CN	CP	D1N	D1P	D0N	D0P	"001"	D3P	D3N	D2P	D2N	CP	CN	C1P	C1N	D0P	D0N	"010"	D0N	D0P	D1N	D1P	CN	CP	D2N	D2P	D3N	D3P	"011"	D0P	D0N	D1P	D1N	CP	CN	D2P	D2N	D3P	D3N	"100"	D2N	D2P	D1N	D1P	CN	CP	D0N	D0P	D3N	D3P	"101"	D2P	D2N	D1P	D1N	CP	CN	D0P	D0N	D3P	D3N	"110"	D3N	D3P	D0N	D0P	CN	CP	D1N	D1P	D2N	D2P	"111"	D3P	D3N	D0P	D0N	CP	CN	D1P	D1N	D2P	D2N
BS[2:0]	HS_D0N	HS_D0P	HS_D1N	HS_D1P	HS_CN	HS_CP	HS_D2N	HS_D2P	HS_D3N	HS_D3P																																																																																																		
"000"	D3N	D3P	D2N	D2P	CN	CP	D1N	D1P	D0N	D0P																																																																																																		
"001"	D3P	D3N	D2P	D2N	CP	CN	C1P	C1N	D0P	D0N																																																																																																		
"010"	D0N	D0P	D1N	D1P	CN	CP	D2N	D2P	D3N	D3P																																																																																																		
"011"	D0P	D0N	D1P	D1N	CP	CN	D2P	D2N	D3P	D3N																																																																																																		
"100"	D2N	D2P	D1N	D1P	CN	CP	D0N	D0P	D3N	D3P																																																																																																		
"101"	D2P	D2N	D1P	D1N	CP	CN	D0P	D0N	D3P	D3N																																																																																																		
"110"	D3N	D3P	D0N	D0P	CN	CP	D1N	D1P	D2N	D2P																																																																																																		
"111"	D3P	D3N	D0P	D0N	CP	CN	D1P	D1N	D2P	D2N																																																																																																		
CSX	I	2	MPU	Chip select signal. For test only. Low: chip can be accessed; High: chip cannot be accessed. If this pin is not used, connect it to VDD1.																																																																																																								
DCX	I	2	MPU	Data / Command Selection pin. For test only. If this pin is not used, please connect it to VSSD or VDD1.																																																																																																								
RESX	I	4	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or VDD1).																																																																																																								
SCL	I	2	MPU	Serial Clock. For test only. If not use, connected to VDD1.																																																																																																								
SDI	I	2	MPU	Serial data input pin. If not used, let it to open. For test only.																																																																																																								
SDO	O	2	MPU	Serial data output pin. If not used, let it to open. For test only.																																																																																																								
HSYNC	I	2	MPU	Line synchronizing signal. For test only. If this pin is not used, connect it to VSSD or VDD1.																																																																																																								
DE	I	2	MPU	Data enable signal. For test only. If this pin is not used, connect it to VSSD or VDD1.																																																																																																								
VSYNC	I	2	MPU	Frame synchronizing signal. For test only. If this pin is not used, connect it to VSSD or VDD1.																																																																																																								
PCLK	I	2	MPU	Dot clock signal. For test only. If this pin is not used, connect it to VSSD or VDD1.																																																																																																								
DB23~0	I/O	24	MPU	Let the unused pins open for each mode.																																																																																																								
Source driver output pins																																																																																																												
S1 to S2400, SL1, SR1	O	2402	LCD	Output voltages applied to the liquid crystal.																																																																																																								
				Panel Resolution	Source channels																																																																																																							
					1 / 2 / 4 / 8 dot, Column inversion		Zig-Zag inversion																																																																																																					
				800RGB	S1 to 2400		S1 to S2400, SL1, SR1																																																																																																					
				768RGB	S1~S1152, S1249~S2400		S1~S1152, S1249~S2400, SL1, SR1																																																																																																					
				720RGB	S1~S1080, S1321~S2400		S1~S1080, S1321~S2400, SL1, SR1																																																																																																					
				640RGB	S1~S960, S1441~S2400		S1~S960, S1441~S2400, SL1, SR1																																																																																																					
				600RGB	S1~S900, S1501~S2400		S1~S900, S1501~S2400, SL1, SR1																																																																																																					
TE	O	6	MPU	Tearing Effect pin.																																																																																																								
TE1	O	6	MPU	Tearing Effect pin of each scan line.																																																																																																								

**GIP control singal and bias voltage**

CGOUT_L1~22	O	22	LCD	Signals for left side GIP on panel view (Left side in IC bump view). Unused pins should be left open.
CGOUT_R1~22	O	22	LCD	Signals for right side GIP on panel view (Right side in IC bump view), Unused pins should be left open.

**Power supply pins**

VDD1	I	31	Power supply	A power supply for the logic power and I/O circuit. VDD1=1.65 to 3.3V.
VDD3	I	19	Power supply	A power supply for the analog power. PCCS[1:0]=10, VDD3 range is 2.5V ~ 3.3V. PCCS[1:0]=00, 01 and 11, VDD3 range is 2.5V ~6.5V.
VSSA	P	17	Power supply	Analoge ground. VSSA=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSAC	P	4	Power supply	Analoge ground. Must connect to VSSA on the FPC.
VSSD	P	46	Power supply	Ground for the internal logic. VSSD=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VPP	I	6	Power supply	External high voltage pin used in OTP mode and operates at 7.5V. If not used, let it open.
VSP	I	5	Stabilizing capacitor	Input voltage from the set-up circuit (3.0V to 6.5V). It is generated from VDD3
VSN	I	5	Stabilizing capacitor	Input voltage from the set-up circuit (-3.0V to -6.5V). It is generated from VDD3.

**Output pins of power and reference voltage**

PCCS1 ~ PCCS0	I	4	VSSD / VDD1	Select the VSP/VSN bumping method as listed below:				
				PCCS [1:0]	Power mode			
				00	External VSP+VSN+ VGH+VGL			
				01	PFM-D			
				10	HX5186 or PFM-A or PFM-C			
				11	External VSP+VSN			
				VDD3(Note) VDD1				
				External	External			
				Internal PFM	Internal DC/DC			
				Internal PFM or HX5186	Internal DC/DC			
				External	Internal DC/DC			
Must be connected to VSSD or VDD1. Note. VDD3 is optional								
VCL	I	5	Stabilizing capacitor	Output voltage from the set-up circuit (-VDD3 or -2.5~-3.1V). It is generated from VDD3. It must be connected a stabilizing capacitor 1.0uF to VSSA.				
VSPC	I	2	VSP	Positive boosting reference voltage input.				
VSNC	I	2	VSN	Negative boosting reference voltage input.				
VSPR	O	3	Stabilizing capacitor	Positive regulated voltage output (3.5V to VSP - 0.5) It must be connected a stabilizing capacitor 1.0uF to VSSA.				
VSNR	O	3	Stabilizing capacitor	Negative regulated voltage output (-3.5V to VSN + 0.5) It must be connected a stabilizing capacitor 1.0uF to VSSA.				
VDDD	O	25	Stabilizing capacitor	Internal logic voltage output It must be connected a stabilizing capacitor 1.0uF to VSSA.				
VGH	O	6	Stabilizing capacitor	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGH.(refer to register B1h to reduce stabilizing capacitor )				
VGL	O	12	Stabilizing capacitor	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VSSA and VGL. (refer to register B1 to reduce stabilizing capacitor )				
VGL2	O	6	Stabilizing capacito	Output regulated voltage for panel voltage. It is generated from VGL. Connect to a stabilizing capacitor between VSSA and VGL2. Place a schottkey barrier diode between VSSA and VGL2. (refer to register B1 to reduce stabilizing capacitor )				
VCOM	O	6	Stabilizing capacitor	The power supply of common voltage in DC com driving. The voltage range is set between -4V to -0.3V. It must be connected a stabilizing capacitor 1.0uF to VSSA.				

VCOMR	I	2	Input	The input pad of external VCOM voltage.
VREF	O	3	Stabilizing capacitor	Internal reference voltage. It must be connected a stabilizing capacitor 1.0uF to VSSA.
<b>DC/DC pumping</b>				
C21P, C21N C22P, C22N	I/O	14 14	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH voltage.
C31P, C31N	I/O	14	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGL voltage.
C41P, C41N	I/O	14	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VCL voltage.
VCSW1, VCSW2	I	16	-	VCSW1 and VCSW2 connect to HX5186-A/B/C.

<b>CABC &amp; ABC</b>				
CABC_PWM_OUT	O	4	Led driver	Backlight on/off control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage range=0 to VDD1.
<b>High speed interface parts</b>				
HS_D0P, HS_D0N	I/O	6/6	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 0) if not used , Please connected to VSSD or open.
HS_CP, HS_CN	I	6/6	DSI Host	MIPI-DSI CLOCK differential signal input pins. If not used , Please connected to VSSD or open.
HS_D1P, HS_D1N	I	6/6	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 1) if not used , Please connected to VSSD or open.
HS_D2P, HS_D2N	I	6/6	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 2) if not used , Please connected to VSSD or open.
HS_D3P, HS_D3N	I	6/6	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 3) if not used , Please connected to VSSD or open.
HS_VCC	P	12	Power Supply	Power supply for the MIPI DSI analog power. VCC=1.65V to 3.3V
HS_VSS	P	17	Ground	MIPI DSI analogy ground. VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
HS_LDO	O	12	Capacitor	DSI regulator output pin. (1.5V) Connect to a stabilizing capacitor between VSS and LDO If not used, please open these pins.
<b>Test Pins</b>				
OSC	I	1	Open	Oscillator input for test purpose. If not used, please let it open or connected to VSSD (weak pull low).
TEST[2:0]	I	6	Open	A test pin. This pin is by internal logic function test.This pin can output on FPC. If not used, let it open or connected to VSSD(weak pull low).
TS0~7	O	8	Open	A test pin. This pin is by internal logic function test. This pin can output on FPC.
VTESTOUTP	O	2	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
VTESTOUTN	O	2	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
FRM	I	2	Open	A test pin. This pin is by internal logic function test. This pin can output on FPC. If not used, please open or connect it to VSSD (weak pull low).
DUMMYR1 DUMMYR2 DUMMYR3 DUMMYR4	-	16	Open	Dummy pads. Available for measuring the COG contact resistance. They are short-circuited within the chip.
DUMMY	-	155	Open	Not used. Let it open.

## 4. Interface

### 4.1 System interface

The HX8394-D supports MIPI DSI (Display Serial Interface) interface. BS2~BS0 are used for the combination of polarity swap and data lane swap of DSI.

BS[2:0]	HS_D0N	HS_D0P	HS_D1N	HS_D1P	HS_CN	HS_CP	HS_D2N	HS_D2P	HS_D3N	HS_D3P
"000"	D3N	D3P	D2N	D2P	CN	CP	D1N	D1P	D0N	D0P
"001"	D3P	D3N	D2P	D2N	CP	CN	C1P	C1N	D0P	D0N
"010"	D0N	D0P	D1N	D1P	CN	CP	D2N	D2P	D3N	D3P
"011"	D0P	D0N	D1P	D1N	CP	CN	D2P	D2N	D3P	D3N
"100"	D2N	D2P	D1N	D1P	CN	CP	D0N	D0P	D3N	D3P
"101"	D2P	D2N	D1P	D1N	CP	CN	D0P	D0N	D3P	D3N
"110"	D3N	D3P	D0N	D0P	CN	CP	D1N	D1P	D2N	D2P
"111"	D3P	D3N	D0P	D0N	CP	CN	D1P	D1N	D2P	D2N

Table 4.1: Interface selection

#### 4.1.1 Serial data transfer interface(MIPI DBI type C)

The HX8394-D supports DBI Type C option 1, 3-wire serial bus to access command set under DSI I/F. The 3-wire serial bus is use: chip select line(CSX), serial input data(SDI),serial output data(SDO) and serial transfer clock line(SCL).

#### 4.1.2 Serial data write mode

The 3-wire serial data packet contains a control bit D/CX and a transmission byte. If D/CX is low, the transmission byte is command byte. If D/CX is high, the transmission byte is stored in to command register. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (SDI and SDO) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

3-wire serial data stream format-DBI Type-C Option 1

Transmission byte (TB) may be Command or Data

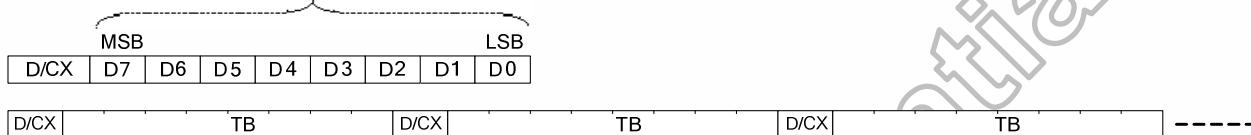


Figure 4.1: Serial data stream, write mode

DBI Type C: Interface protocol-Option 1 (3-wire)

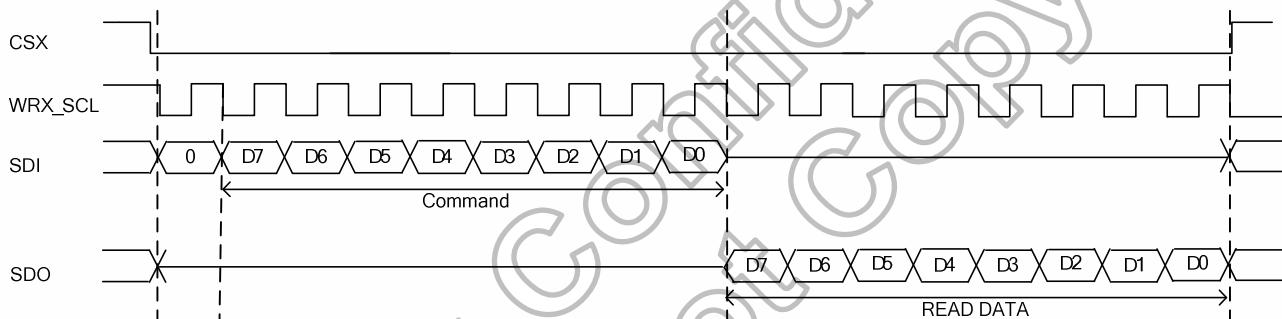


Figure 4.2: Serial data stream, write mode

#### 4.1.3 Serial data read mode

The micro-controller first has to send a command and then the following byte is transmitted in the opposite direction. The 3-wire serial read data format which just needs 8-bit.

DBI Type C: Interface protocol-Option 1 (3-wire)

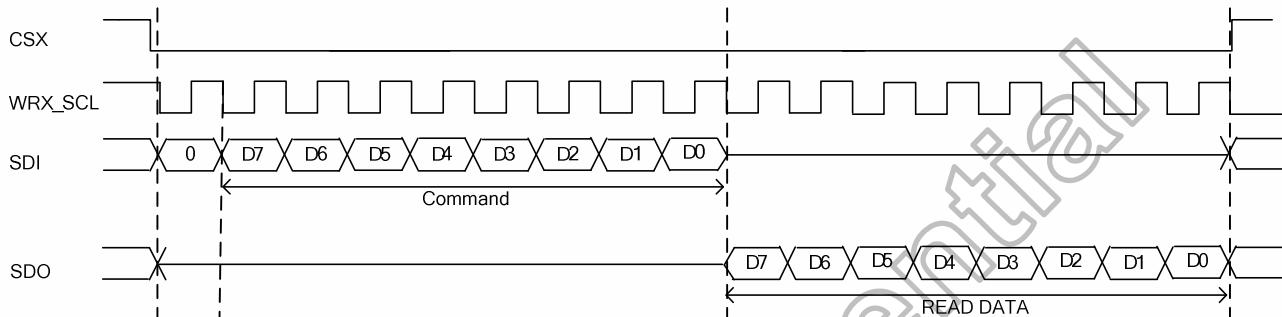


Figure 4.3: Type C:Serial interface protocol 3-wire/4-wire read mode

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

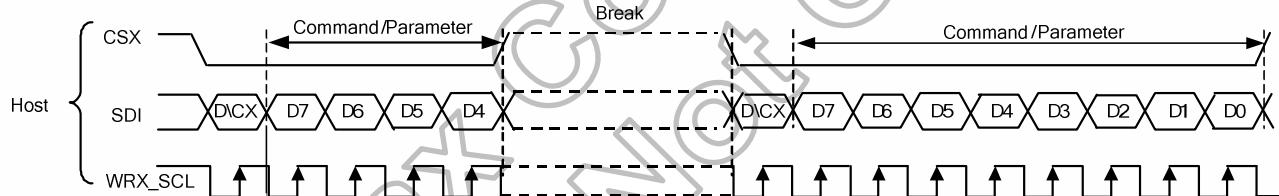


Figure 4.4: Display module data transfer recovery

## 4.2 DSI system interface

The selection of interface is by  $BS[2:0] = "000" \sim "111"$  the DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.5 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that.

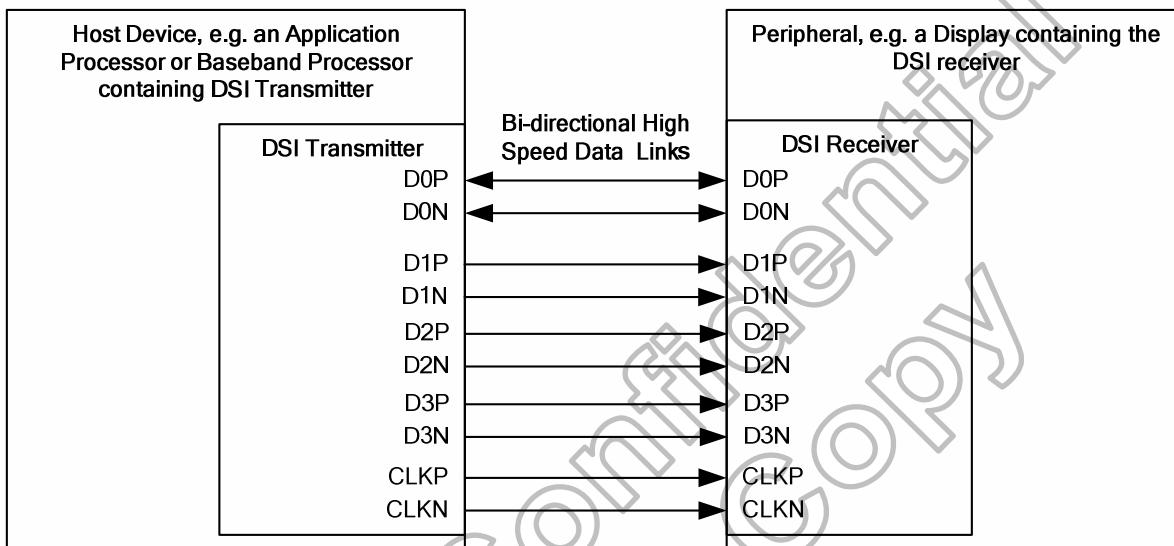


Figure 4.5: DSI transmitter and receiver interface

Please refer to “**DRAFT MIPI Alliance Standard for DSI**” for DSI detail specifications.

The data lane number is selected by register RBAh.

#### 4.2.1 DSI layer definitions

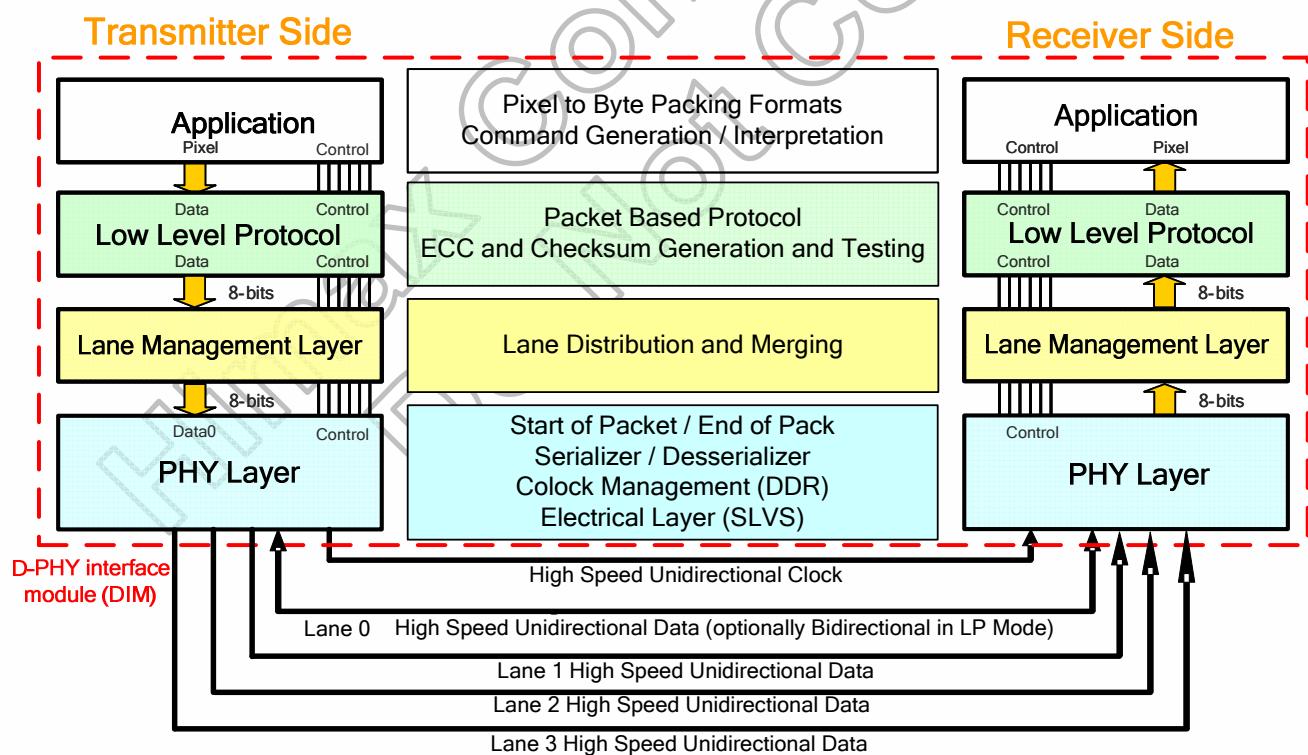
According Figure 4.6 DSI transmitter and receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four layers: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.



**Figure 4.6: DSI transmitter and receiver interface**

#### 4.2.2 Lane states

The HX8394-D uses Data Lane and Clock Lane differential pairs for DSI. Both differential lane pairs can be driven LP (Low Power) or HS (High Speed) mode.

LP mode means each line of the differential pairs are used in independently and single-ended. In LP mode differential receiver is disable( termination resistor of the receiver is disable). In LP mode there are four possible Low-Power Lane states (LP-00, LP-01, LP-10, LP-11).

HS mode means the differential pairs are not used in single-end and termination resistor of the receiver is enable. There are different modes and protocol in each mode when transfer display data from MCU to the display module.

The state code of HS and LP Lane pair are defined as below:

State Code	Line Voltage Levels		High-Speed Burst Mode	Low-Power	
	Dp-Line	Dn-Line		Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	Note1	Note1
HS-1	HS High	HS Low	Differential-1	Note1	Note1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note2

**Note:** (1) During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.

(2) If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

#### 4.2.3 Clock lane mode

Figure 4.7 shows the state diagram for Clock Lane Mode. The Clock Lane has three different power modes: Low Power Stop State, Ultra Low Power State(ULPS) and High Speed clock transmission.

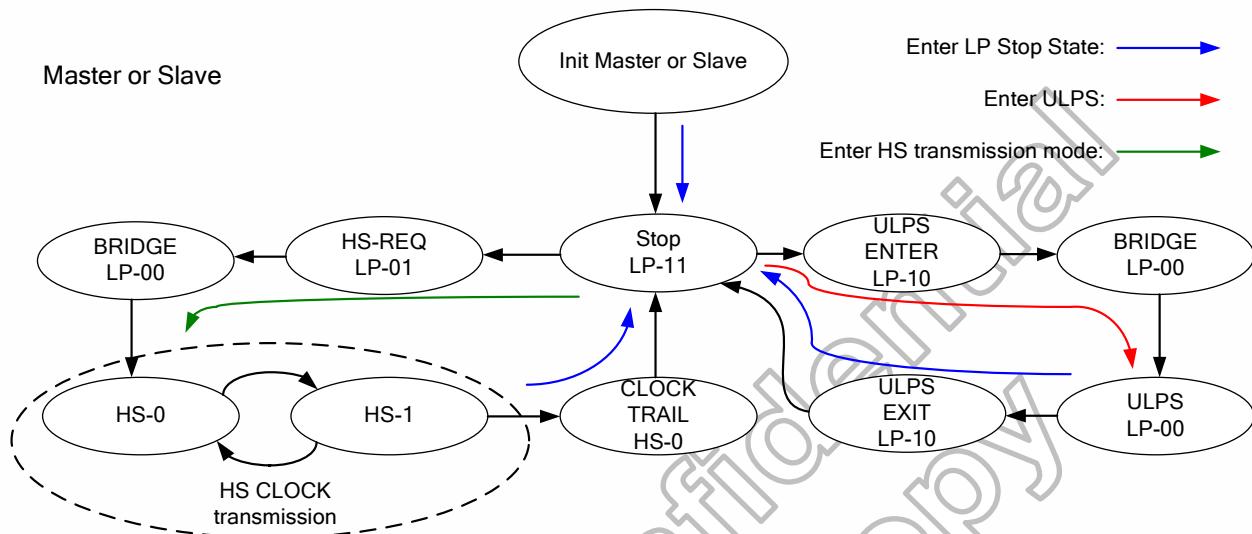
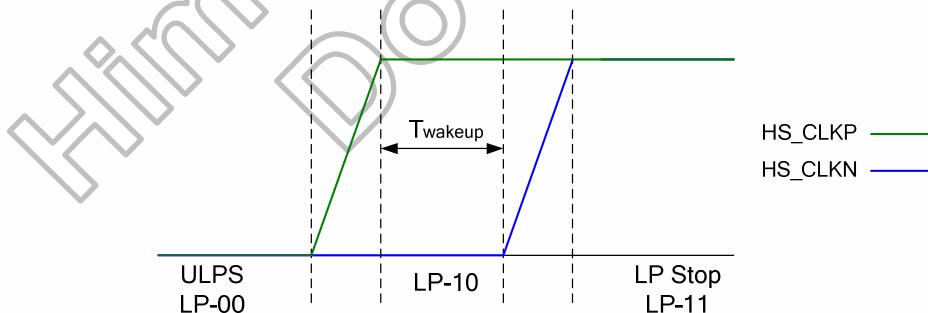


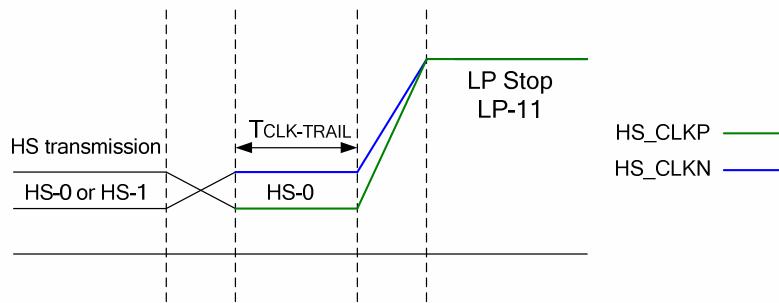
Figure 4.7: Clock lane mode state diagram

Clock Lane can be driven LP-11 to enter Low Power Stop State. There are three ways to enter Lower Power Stop State:

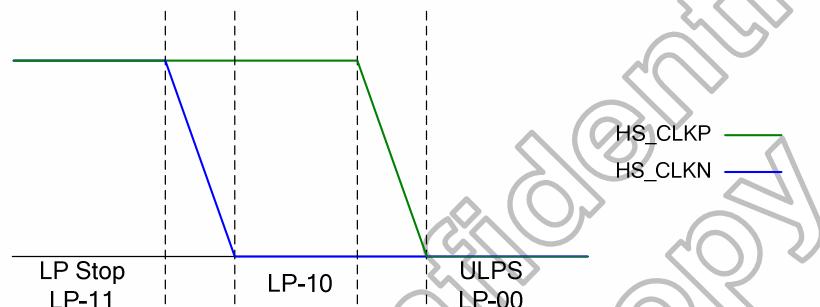
- (1) After Initial state(HW reset, SW reset, Power on sequence).
- (2) Leaving ULPS: ULPS LP-00 -> LP-10 -> Low Power Stop State LP-11.



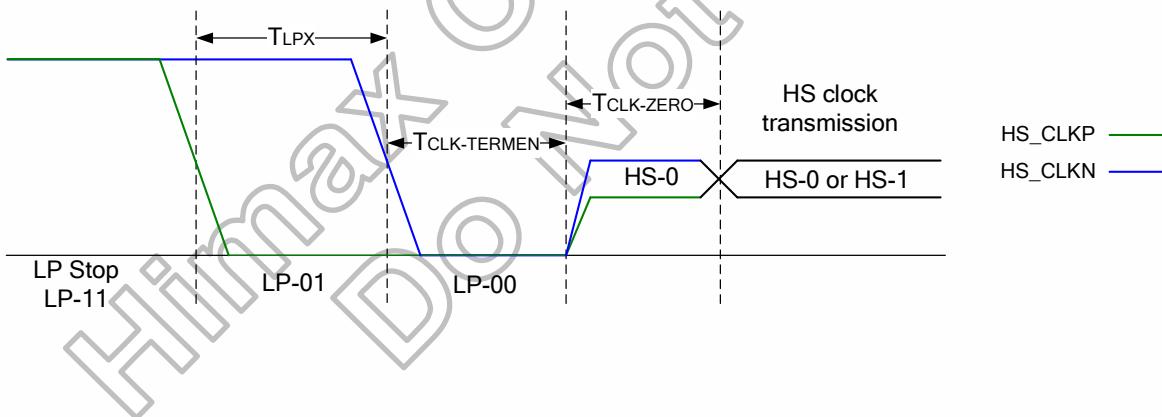
- (3) Leaving HS clock transmission mode: HS mode (HS-0 or HS-1) -> HS-0 -> Low Power Stop State LP-11.



Clock Lane can be driven LP-00 to enter Ultra Low Power State from Low Power Stop State. The flow is Low Power Stop State LP-11 -> LP-10 -> ULPS LP-00.

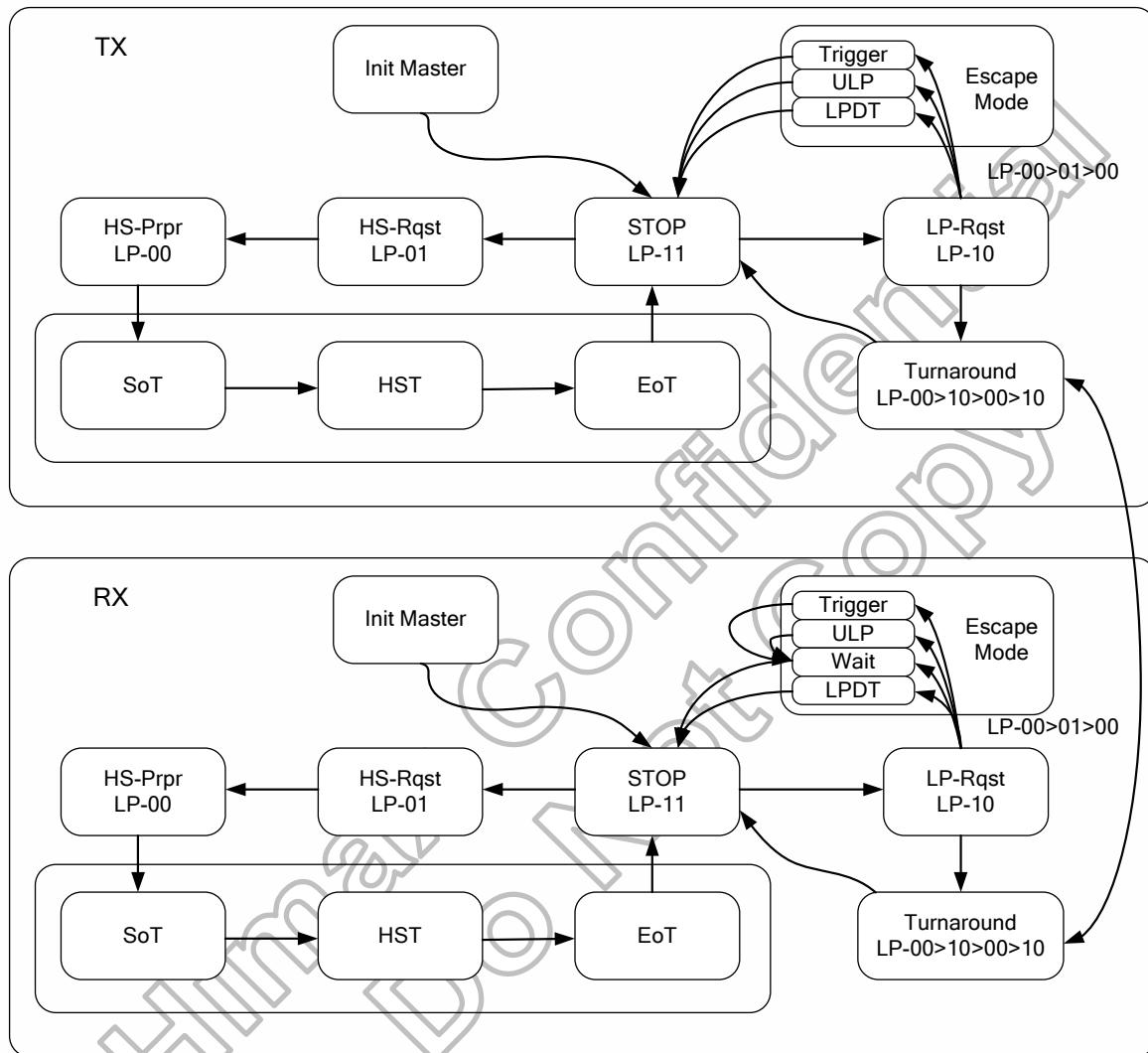


Clock Lane can be High Speed Clock transmission State from Low Power Stop State. The flow is Low Power Stop State LP-11 -> LP-01 -> LP-00 -> HS-0/1.



#### 4.2.4 Data lane mode

Figure 4.8 shows the operational flow diagram for Data Lane Mode. There are three operating modes in Data Lane: Escape mode, High-Speed transmission mode and Turnaround.



**Figure 4.8: Data lane mode state diagram**

#### 4.2.5 Escape Mode

Data Lane0 is used in Escape Mode when data lane in LP mode. Data Lane shall enter Escape mode via LP-11 -> LP-10 -> LP-00 -> LP-01 -> LP-00 and exit Escape mode via LP-10 -> LP-11.

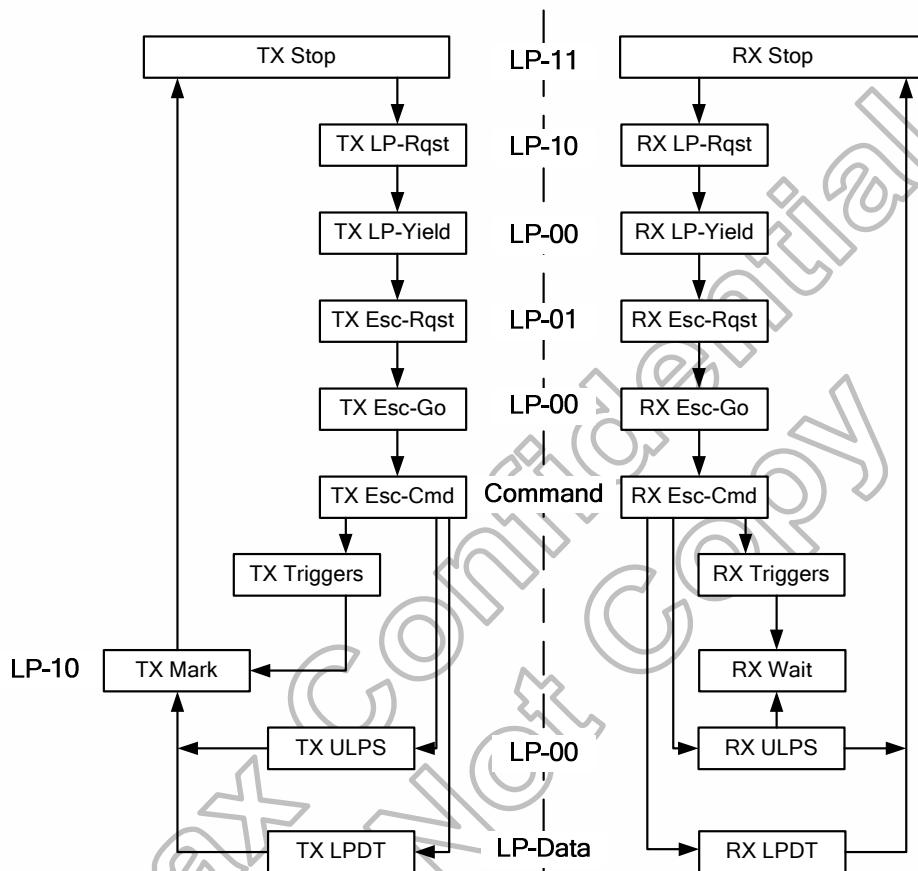
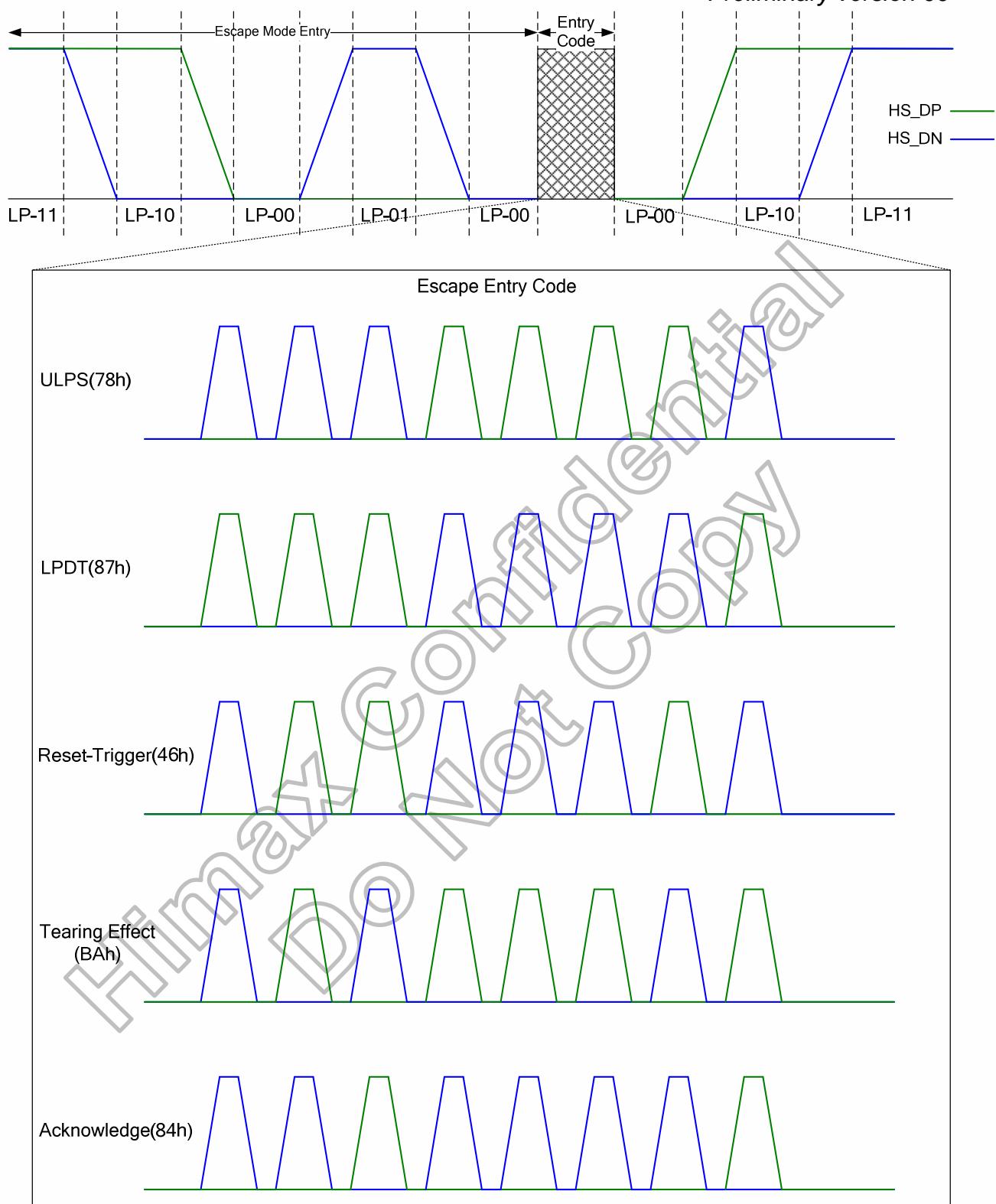


Figure 4.9: Escape mode state machine

Once Escape mode is entered, the transmitter shall send an 8-bit entry code to indicate the requested action. The Entry Code as follows:

- (1) Trigger (Reset-Trigger(46h), Tearing effect(BAh), Acknowledge(84h))
- (2) Drive Data Lane to Ultra Low Power State(78h)
- (3) Send Low Power Data Transmission(87h)

**Figure 4.10: Escape Mode timing sequence**

#### 4.2.6 High speed data transmission

The display module can enter High Speed Data Transmission when Clock Lane in the High Speed Clock Mode. All Data Lane enter High Speed Data Tranmission synchronously but may end at different time. Data Lane enter High Speed Data Transmission flow: LP-11 -> LP-01 -> LP-00 -> SoT(0001\_1101). And exit High Speed Data Transmission flow: Toggles differential state immediately after last payload data bit and keeps that state for a time  $T_{HS-TRAIL}$ .

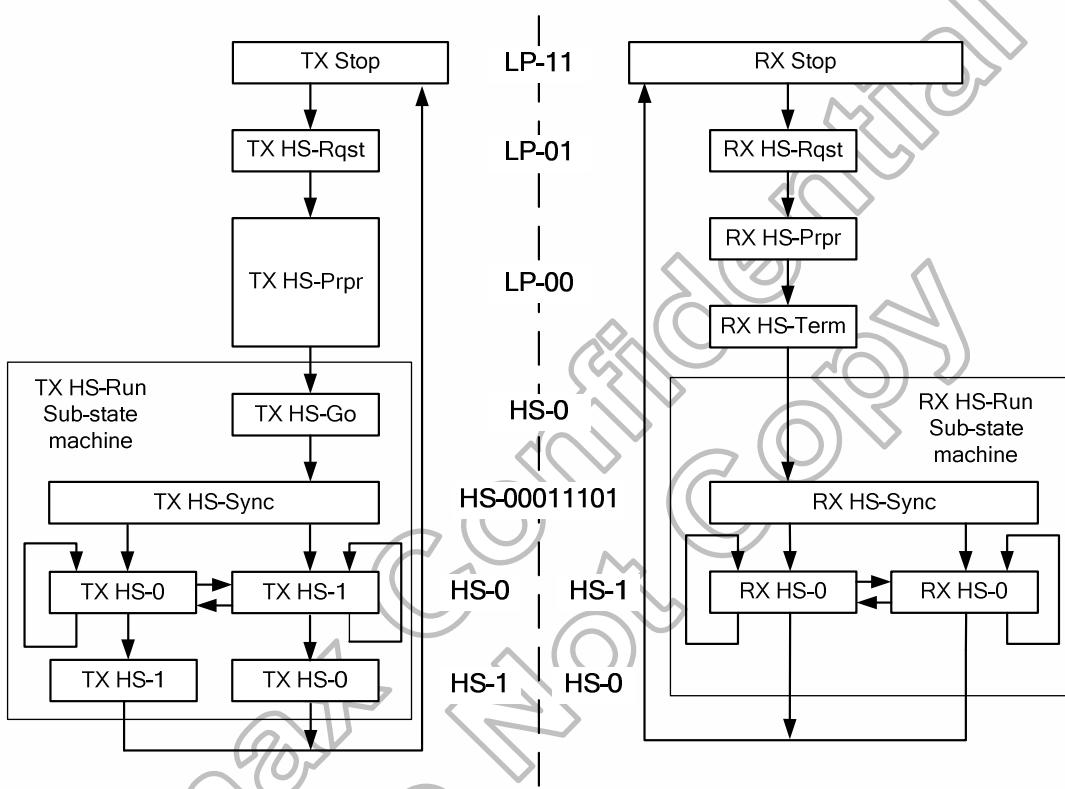


Figure 4.11: High speed data transmission state machine

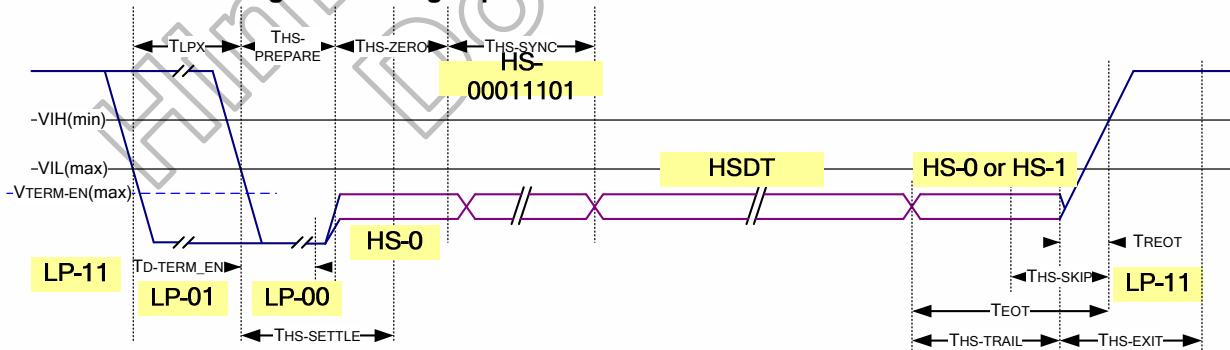


Figure 4.12: High speed data transmission timing sequence

#### 4.2.7 Bi-directional data lane turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction.

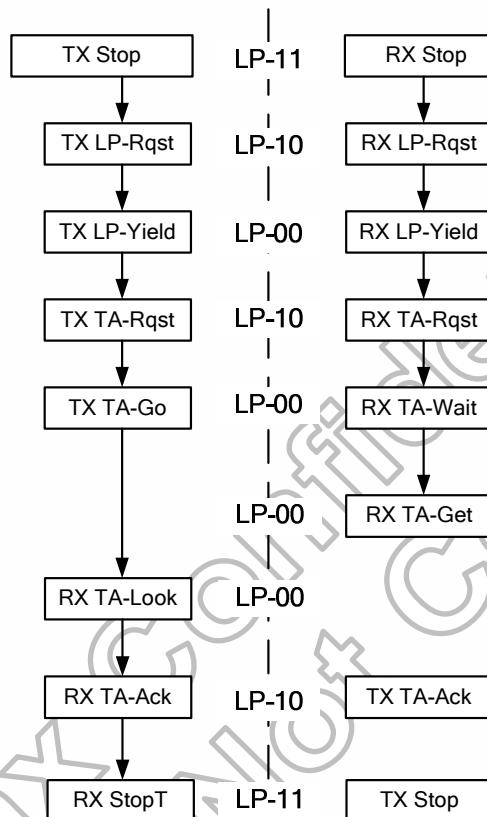


Figure 4.13: Turnaround state machine

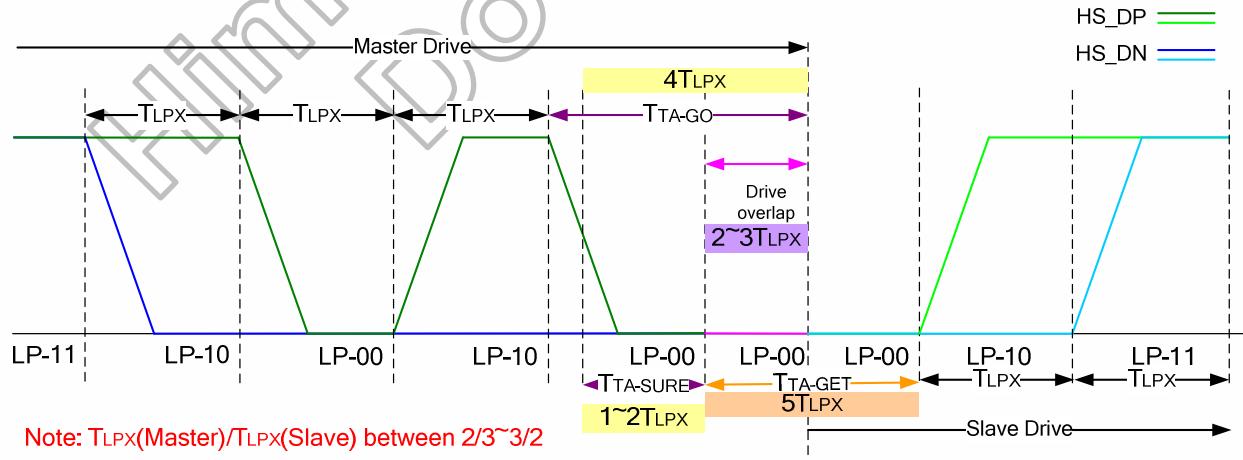
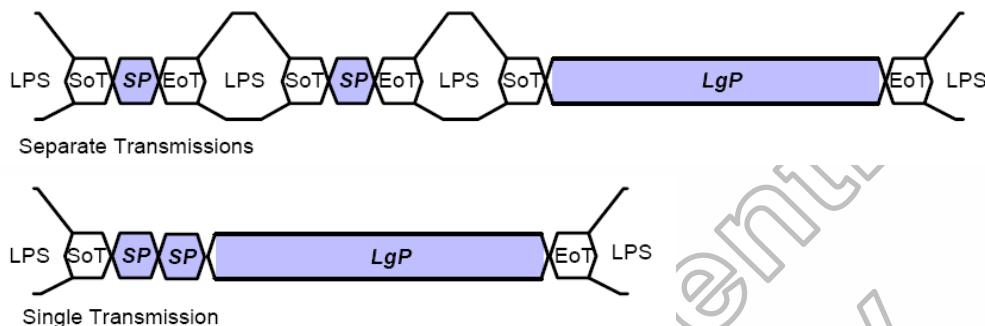


Figure 4.14: Turnaround timing sequence

#### 4.2.8 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 4.15 illustrates multiple HS Transmission packets.



LPS : Low power state

SoT : Start of Transmission

SP : Short Packet

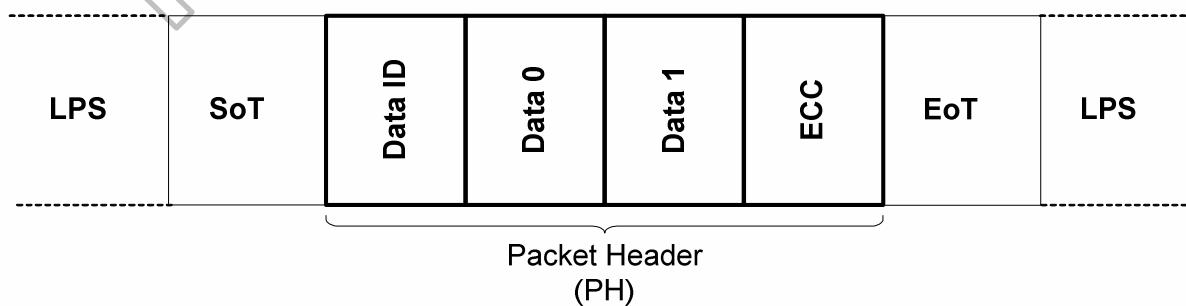
LgP : Long Packet

EoT : End of Transmission

**Figure 4.15: Multiple packets transmission**

The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Short packets are four bytes in length including the ECC. Short packet is used for most Command Mode commands and associated parameters. Where Short packets format include an 8-bit Data ID followed by two command or data and an 8-bit ECC. Figure 4.16 shows the structure of the Short packet.



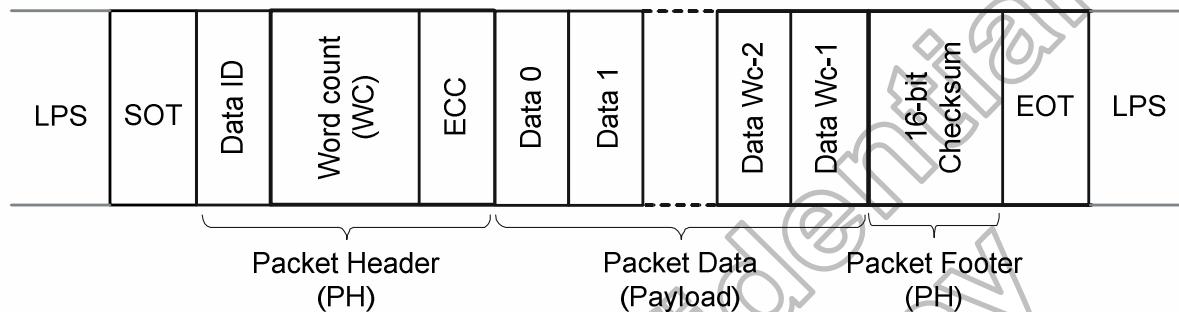
**Figure 4.16: Structure of the short packet**

**DI(Data ID)** : Contain Virtual Channel Identifier and Data Type.

**ECC(Error Correction Code)** : The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

**Long packets** specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,535 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Figure 4.17 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. An application-specific Data Payload has Word Count \* bytes following the Packet Header. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where  $65,541 \text{ bytes} = 4 \text{ bytes PH} + (2^{16}-1)\text{bytes Payload} + 2 \text{ bytes PF}$



**DI (Data ID)** : Contain Virtual Channel Identifier and Data Type.

**WC (Word Count)** : The receiver use WC to determine the packet end.

**ECC (Error Correction Code)** : The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

**PF(Packet Footer)** : Mean 16-bit Checksum.

Figure 4.17: Structure of the long packet

According to packet form, basic elements include DI and ECC. Figure 4.18 the shows format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)	DT (Data Type)						

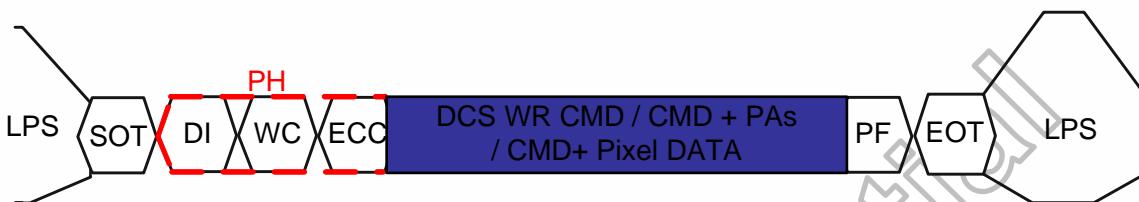
DI[7:6] → These two bits identify the data as directed to one of four virtual channels.

DI[5:0]: These six bits specify the Data Type.

Figure 4.18: The format of data ID

Due to Data Type (DT) mean format of transmission type, Figure 4.19 show Short- / Long-packet transmission command sequence.

#### Long packet write Command / Parameters / Pixel Data



DI Write suitable Data type.

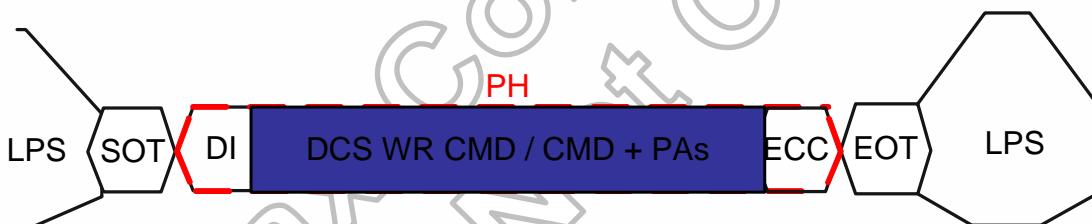
WC Write number of Payload Data.

Ex: One CMD write, WC setting as 1.

CMD + PAs write, WC setting as number of (CMD+PAs).

CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

#### Short packet write Command / Parameters



DI Write suitable Data type.

Ex: One CMD write, DI + DCS WR CMD

CMD + PAs write, DI + DCS WR CMD + PAs

**Figure 4.19: Show short- / long-packet transmission command sequence**

#### 4.2.9 Processor to peripheral (forward direction) packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.2 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet(EoTp)	Short
05h	000101	DCS WRITE, no parameter	Short
15h	010101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 4.2: Data types for processor-sourced packets

Under tables list all detail function of all data types

<b>Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)</b>		
<b>Data type, hex</b>	<b>Function description</b>	<b>Number of bytes</b>
01h	V Sync start, Start of VSA pulse.	4 bytes (DI+00h+00h+ECC)
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of I pulse.	
31h	H Sync End, End IHSA pulse.	

**Note:** V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the I, respectively.

<b>Display status (shutdown command, turn-on command )</b>		
<b>Data type, hex</b>	<b>Function description</b>	<b>Number of bytes</b>
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	4 bytes (DI+00h+00h+ECC)
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	

**Note:** When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.

<b>DCS command setting</b>		
<b>Data type, hex</b>	<b>Function description</b>	<b>Number of bytes</b>
06h	DCS Read command, the returned data <b>shall be Long packet format.</b>	4 bytes (DI+Data0+Data1+ECC)
05h and 15h	DCS Short Write command, 0 or 1 parameter, Data Types = 00 0101(05h), 01 0101 (15h), Respectively.	4 bytes (DI+Data0+Data1+ECC)
39h	DCS Long Write/ Write _LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF )

**Note:** (1) For write part, If DCS Short Write command, followed by BTA, the peripheral shall respond with ACK when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.

For example: 05h DCS WRITE for no parameter command set.

05h	CMD	0	ECC
-----	-----	---	-----

Ex. 05h, 29h, 00, 1Ch — Display On(29h)

For example: 15h DCS WRITE for only one parameter command set.

15h	CMD	Par	ECC
-----	-----	-----	-----

Ex. 15h, 36h, 08h, 11h — MADCTL(36h)-BGR bit=1

(2) When use DCS Read Command, the Set Max Return Packet Size command will limit the size of returning packets.

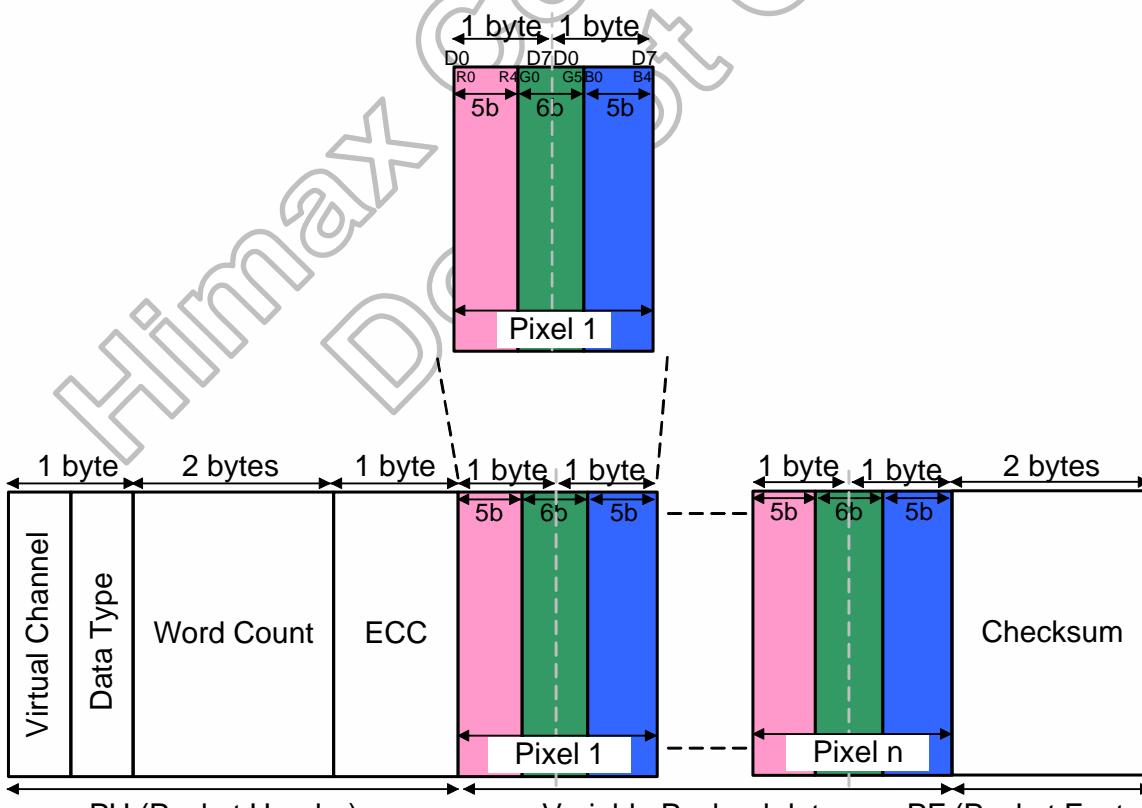
(3) The peripheral shall respond to DCS Read Command Request in one of the following ways:

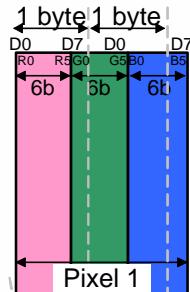
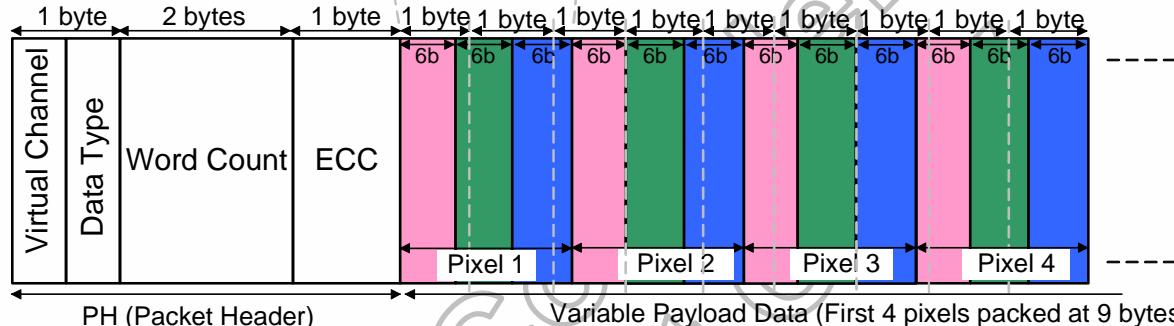
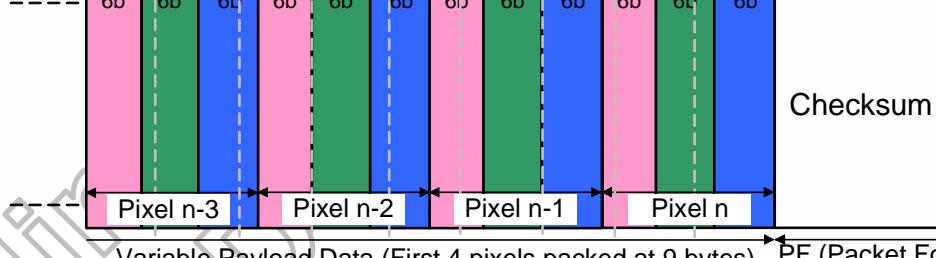
- ◆ If an error was detected by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- ◆ If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.

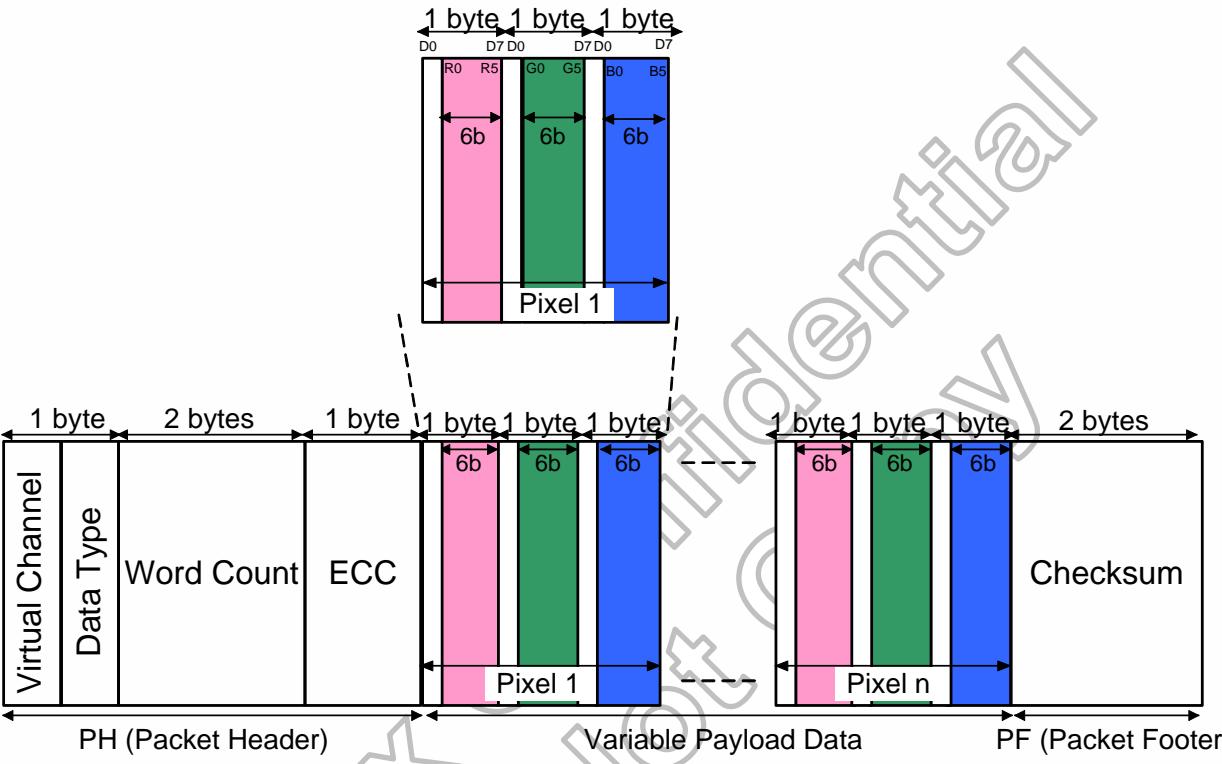
(4) One byte <= Length of payload DATA <=  $2^{16}-1$

<b>Maximum Return packet size setting</b>		
<b>Data type, hex</b>	<b>Function description</b>	<b>Number of bytes</b>
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes (DI + Maximum Return Packet Size + ECC)
<b>Note:</b> The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.		

<b>Variable data packet</b>		
<b>Data type, hex</b>	<b>Function description</b>	<b>Number of bytes</b>
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF )
19h	Blanking packet is used to convey blanking timing information in a Long packet.	
<b>Note:</b> (1) When Null Packet, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data. (2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display,		

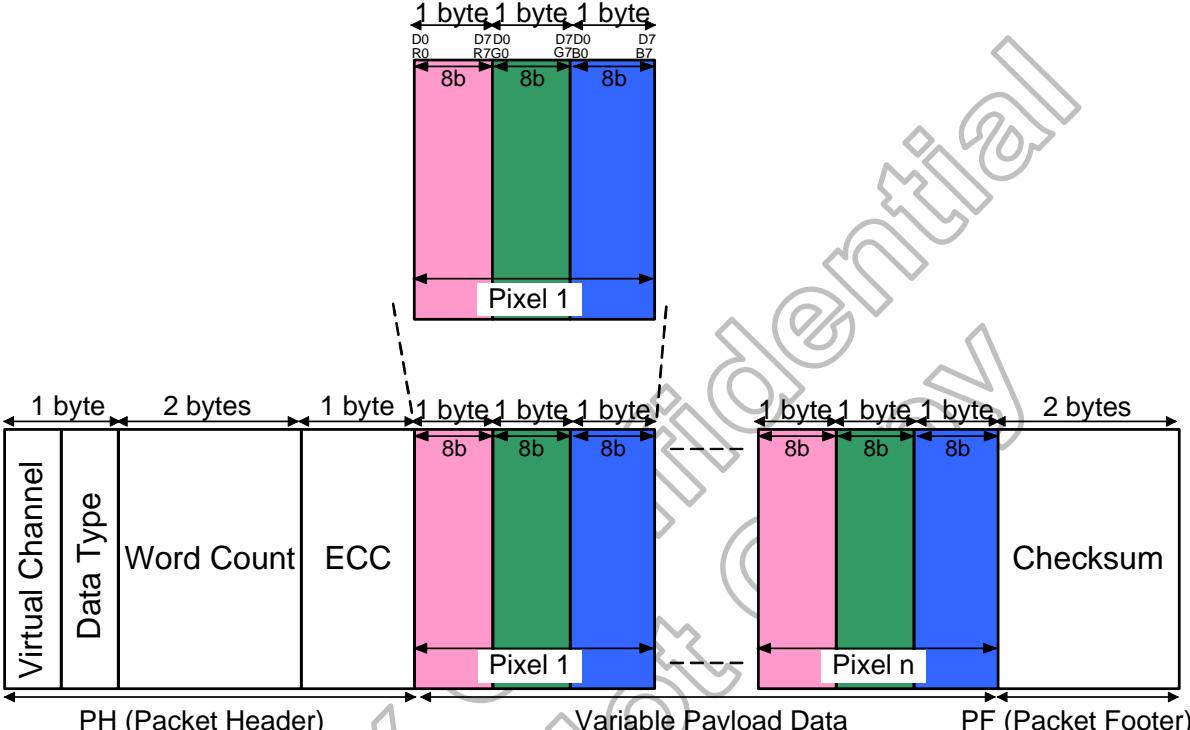
<b>Data stream format</b>		
<b>Data type, hex</b>	<b>Function description</b>	<b>Number of bytes</b>
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "(5 bits) red, (6 bits) green and (5 bits) blue".	Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF )
		
<b>Note:</b> Within a color component, the "LSB is sent first, the MSB last ".		

<b>Data stream format</b>		<b>Function description</b>	<b>Number of bytes</b>
1Eh		Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is “(6 bits) red, (6 bits) green and (6 bits) blue”.	Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF )
 <b>Pixel 1</b> : 1 byte (9 bytes total) = R0 (6b)   G0 (6b)   B0 (6b)			
 <b>PH (Packet Header)</b> : 1 byte (Virtual Channel)   2 bytes (Data Type)   1 byte (Word Count)   ECC			
 <b>Variable Payload Data (First 4 pixels packed at 9 bytes)</b> : Pixel 1   Pixel 2   Pixel 3   Pixel 4			
 <b>Variable Payload Data (First 4 pixels packed at 9 bytes)</b> : Pixel n-3   Pixel n-2   Pixel n-1   Pixel n   <b>Checksum</b>			
 <b>PF (Packet Footer)</b> : 2 bytes			
<p><b>Note:</b> Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a “clean start” for the next line.</p>			

Data stream format		
Data type, hex	Function description	Number of bytes
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue".	Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF )
 <p>The diagram illustrates the data stream format. At the top, a pixel is shown as a vertical stack of three 6-bit color components: Red (R0-R5), Green (G0-G5), and Blue (B0-B5). Below this, the data is organized into a packet structure. The packet header (PH) consists of four fields: Virtual Channel (1 byte), Data Type (2 bytes), Word Count (1 byte), and ECC (1 byte). The variable payload data section follows, containing multiple pixels. Each pixel is represented by its three color components. The payload section ends with a checksum field (2 bytes). The packet footer (PF) follows the payload.</p>		
<b>Note:</b> Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.		

**Packed pixel stream, 24-bit format**

Data type, hex	Function description	Number of bytes
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF )


  
**Pixel Structure:**  
Pixel 1: 8b (R), 8b (G), 8b (B). Bit labels: D0, R7, D7D0, G7B0, D7, B7.  
Pixel n: 8b (R), 8b (G), 8b (B). Bit labels: D0, R7, D7D0, G7B0, D7, B7.  
  
**Packet Structure:**  
PH (Packet Header): Virtual Channel (1 byte), Data Type (2 bytes), Word Count (1 byte), ECC (1 byte).  
Variable Payload Data: A sequence of pixels (Pixel 1, ..., Pixel n). Each pixel is 24 bits (3 bytes).  
PF (Packet Footer): Checksum (2 bytes).

**Note:** Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

#### 4.2.10 Peripheral to processor (reverse direction) packet data type

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets shall use ECC and may use Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

Peripheral-to-processor transactions are of four basic types:

- A. *Tearing Effect* is a Trigger message sent to convey display timing information to the host processor. Trigger messages are single byte packets sent by a peripheral's PHY layer in response to a signal from the DSI protocol layer.
- B. *Acknowledge* is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication is received by the peripheral with no errors.
- C. *Acknowledge and Error Report* is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
- D. *Response to Read Request* may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with BTA asserted, can contain under form.

- A. Following a non-Read command in which no error was detected, the peripheral shall respond with Acknowledge.
- B. Following a Read request in which no error was detected, the peripheral shall send the requested READ data.
- C. Following a Read request in which the ECC error was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
- D. Following a non-Read command in which the ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
- E. Following any command in which SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

Which,

- A. “Acknowledge” is sent using a Trigger message which is one byte: 00100001
- B. “Acknowledge with Error Report” include 4 bytes which are DI, 2 bytes Error report and ECC.
- C. “Response to Read Request” are Long packet format.

An error report is comprised of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.3 shows the Error Report Bit Definitions. And Table 4.4 list complete set of peripheral-to-processor Data Types.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	Reserved
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	Reserved
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Reserved
14	Reserved
15	Reserved

Table 4.3: Shows the error report bit definitions

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
1Ch	01 1100	DCS Long READ Response	Long
Others (00h→3Fh)		Reserved	-

Table 4.4: The complete set of peripheral-to-processor data types

<b>Acknowledge types</b>		
Data type, hex	Function description	Number of bytes
02	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
<b>Note:</b> When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error → Acknowledge with error report (Short packet), Without error → request READ data or Acknowledge (trigger message).		

<b>DCS Read types</b>		
Data type, hex	Function description	Number of bytes
1Ch	This is the Long-packet response to DCS Long Read Request.	Up to 65541 bytes ( DI + WC + ECC + DCS CMD. + Payload DATA + PF )
<b>Note:</b> (1)If the peripheral is Checksum capable, it shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent. (2)There is no dummy read byte in the read response packet.		

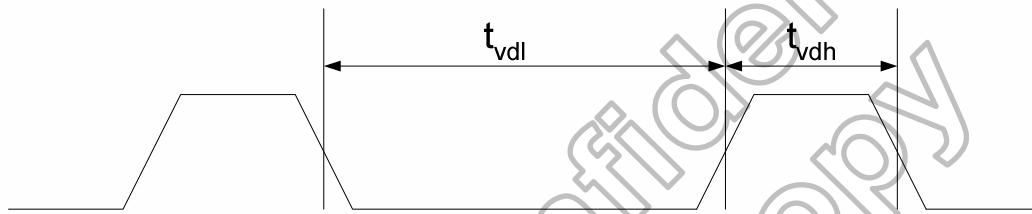
## 5. Function Description

### 5.1 Tearing effect output line

The Tearing Effect output line supplies a panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize frame memory writing when displaying video images.

#### Tearing Effect Line Modes

**Mode 1**, the Tearing Effect Output signal consists of V-Blinking Information only:



**Figure 5.1: Tearing effect output signal mode 1**

tvdh= The LCD display is not updated from the Frame Memory

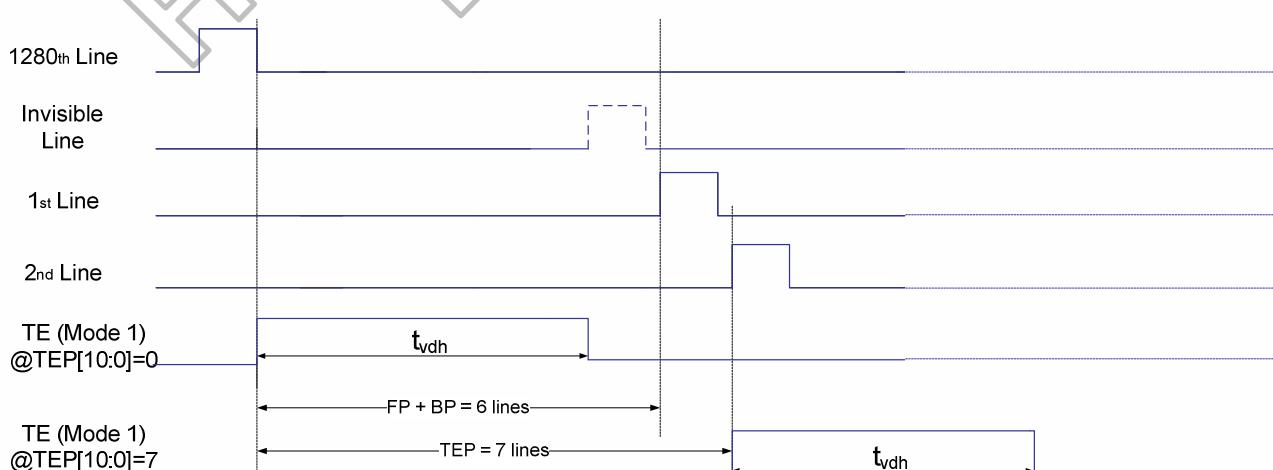
tvdI= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Under Mode1, the TE output timing will be defined by TEP[10:0] setting.

Ex: 1. FB=BP=0x01h (3 line) .

TEP[10:0]=0, then TE signal will output after last line finished.

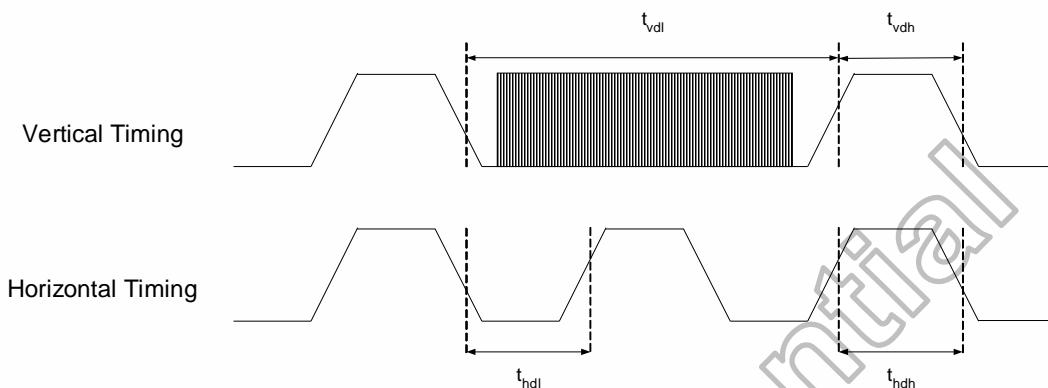
TEP[10:0]=7, then TE signal will output at second line start.



**Figure 5.2: TE delay output**

### 5.1.1 Tearing effect line timing

The Tearing Effect signal is described below:



**Figure 5.3: Tearing effect output line –tearing effect line timing**

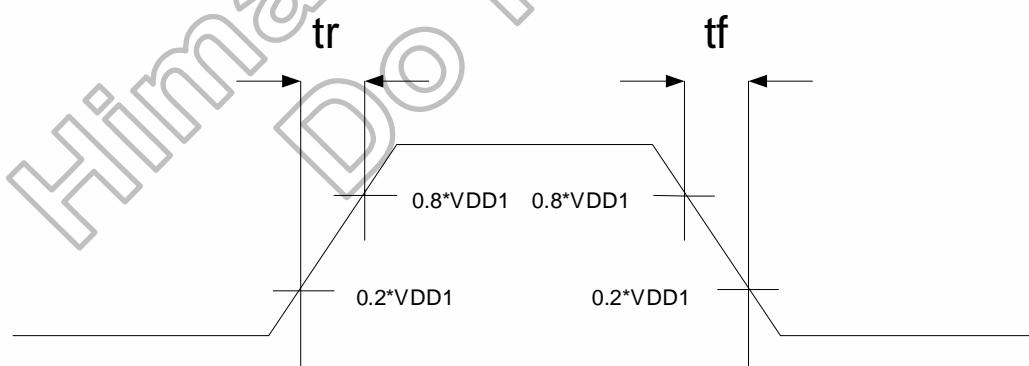
Idle Mode Off (Resolution 800x1280 RGB, Frame Rate = 60 Hz)

Symbol	Parameter	Min.	Max.	Unit
tvdl	Vertical Timing Low Duration	15	-	ms
tvdh	Vertical Timing High Duration	VFP+VHP+VBP	-	us
tr	Rise time	-	15	ns
tf	Fall time	-	15	ns

**Note:** The timings in Table 5.1 apply when MADCTL ML=0 and ML=1

**Table 5.1: AC characteristics of tearing effect signal**

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



**Figure 5.4: Tearing effect output line–definition of tf, tr**

## 5.2 Oscillator

The HX8394-D can oscillate an internal R-C oscillator with an internal oscillation resistor ( $R_f$ ). The oscillation frequency is changed according to the internal register if needed. The default frequency is 40MHz. The oscillation frequency tolerance is  $\pm 5\%$ .

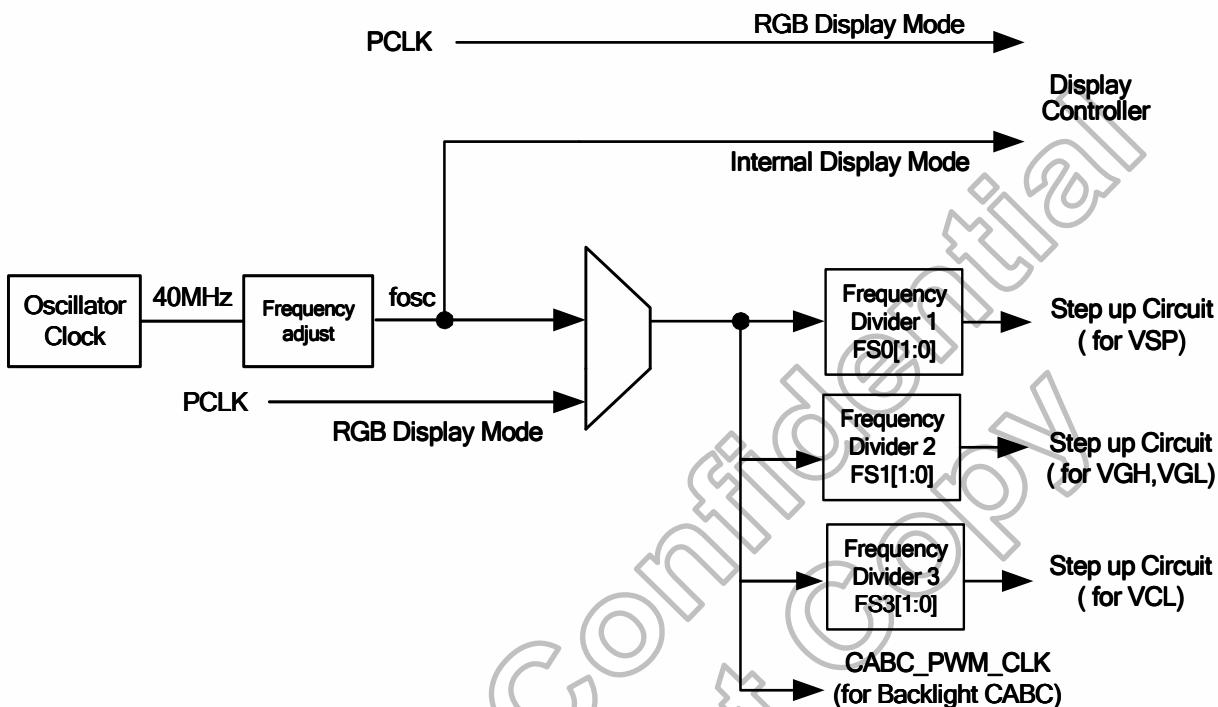


Figure 5.5: OSC architecture

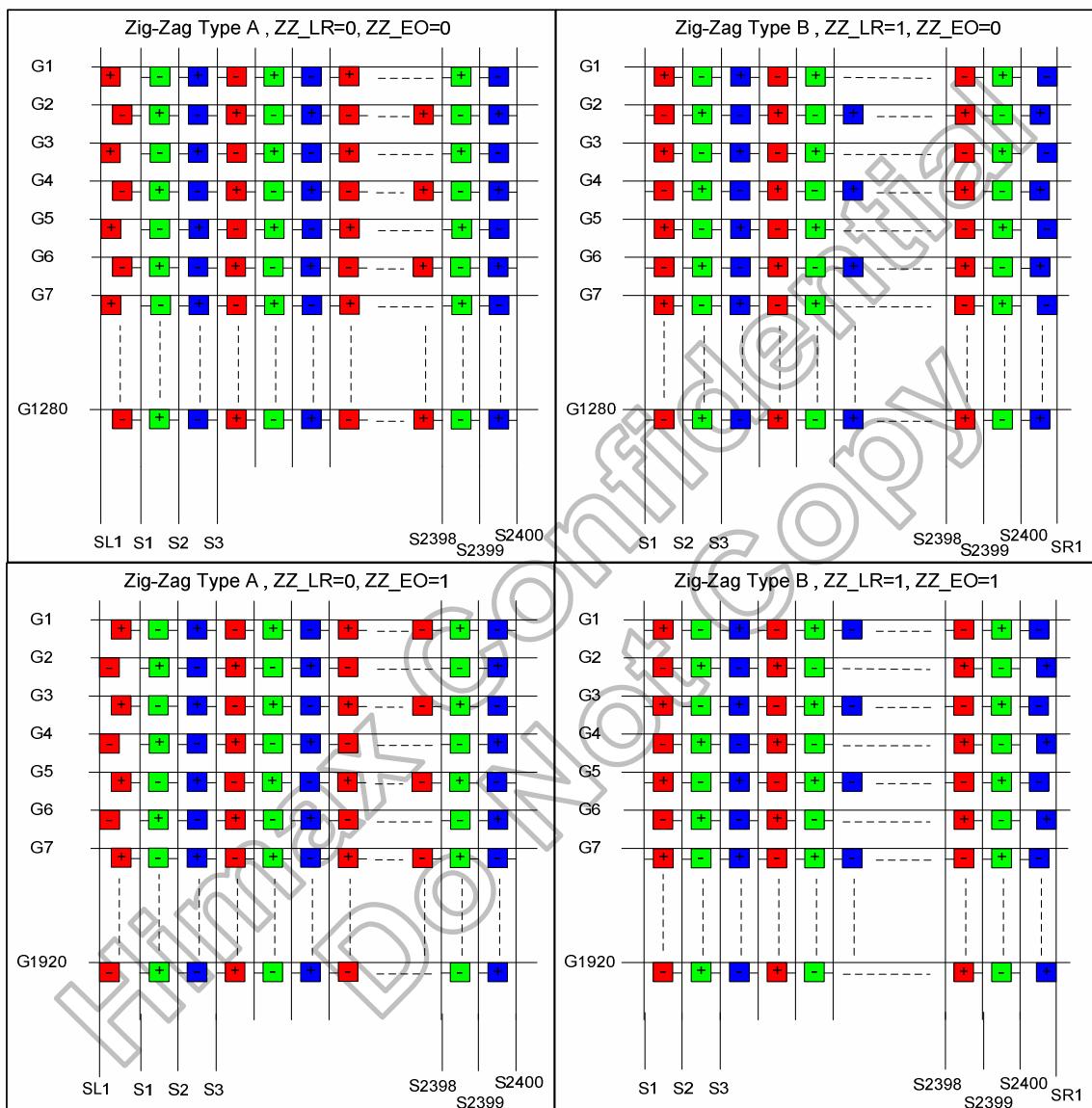
### 5.3 Source driver

The HX8394-D contains a 2402 channels of source driver (normal S1~S2400; Zig-zag S1~S2400,SL1,SR1) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data into the analog voltage for 2400 channels and generates corresponding gray scale voltage output, which can realize a 16.7M colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately output from each channel.

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### 5.3.1 Zig-Zag Inversion

The HX8394-D supports Zig-Zag inversion which can reduce power consumption. This inversion uses the same polarity as column inversion for data line and has almost the same display quality as 1-dot inversion.



**Figure 5.6: Zig-Zag inversion mode**

## 5.4 LCD power generation scheme

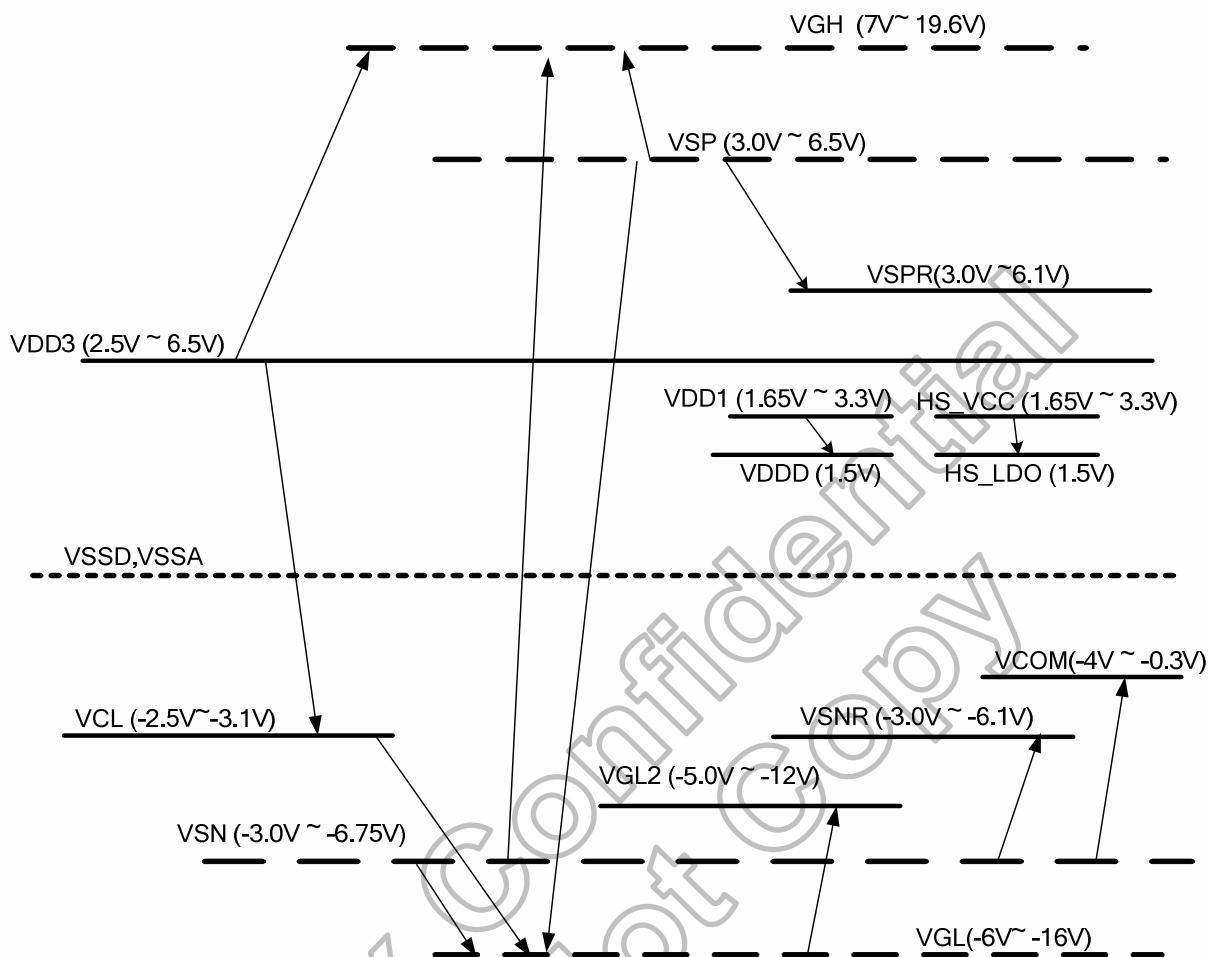


Figure 5.7: LCD power generation scheme

## 5.5 DC/DC converter circuit

### 5.5.1 Charge pump and step up circuit mode

HX8394-D supports various kinds of power generation mode, including PFM Type A, PFM Type C, PFM Type D and external HX5186-A/B/C and external VSP & VSN power mode. All power power mode can be set by hardware pins PCCS[1:0] as below:

PCCS [1:0]	Power mode	Input Power	VSP	VSN	VGH/VGL
00	External VSP+VSN+VGH +VGL	VDD3(Note) VDD1	External	External	External
01	PFM-D	VDD3(Note) VDD1	External	Internal PFM	Internal DC/DC
10	HX5186 or PFM-A or PFM-C	VDD3, VDD1	Internal PFM or HX5186	Internal PFM or HX5186	Internal DC/DC
11	External VSP+VSN	VDD3(Note) VDD1	External	External	Internal DC/DC

Note : VDD3 is optional

**Table 5.2: Power mode setting**

### 5.5.2 Use PFM DC/DC converter

The PFM DC-DC converter generates the high voltage level VSP/VSN required for source drivers. HX8394-D contains sub-circuits of the PFM boost converter, including a precision 1.8V reference voltage, comparator, PFM controlling logic, and the output buffer. The boost converter uses a external power transistor to provide maximum efficiency and to minimize the number of external components. The output voltage of the boost converter can be set from +3.0V to +6.6V (VSP) and -3.0V to -6.6V (VSN).

#### Use PFM DC/DC converter (PCCS[1:0] = "01")

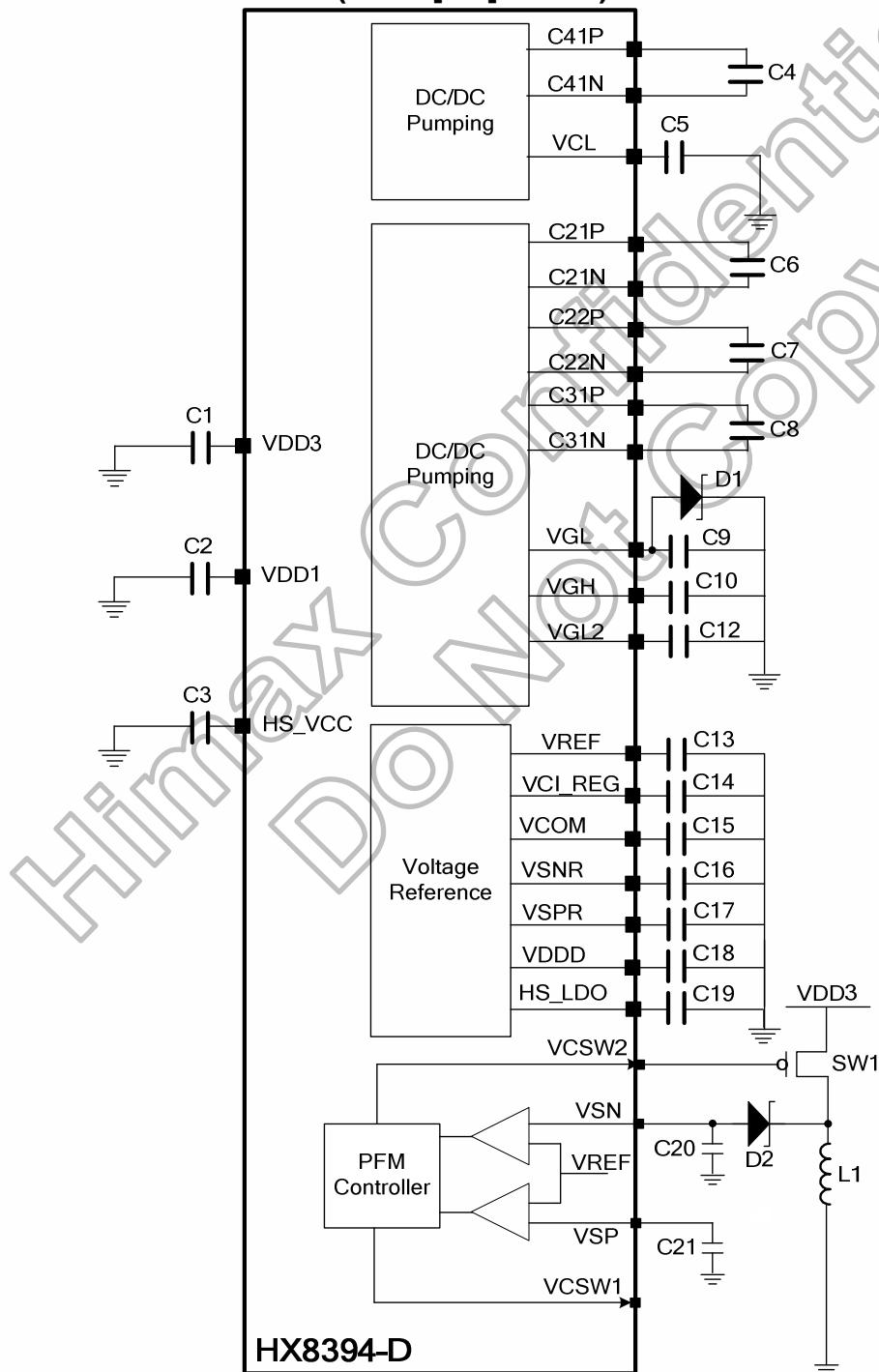


Figure 5.8: DC/DC converter circuit (PFM Type D)

Use PFM DC/DC converter (PCCS[1:0] = "10") and (POWMOD[1:0]= "00")

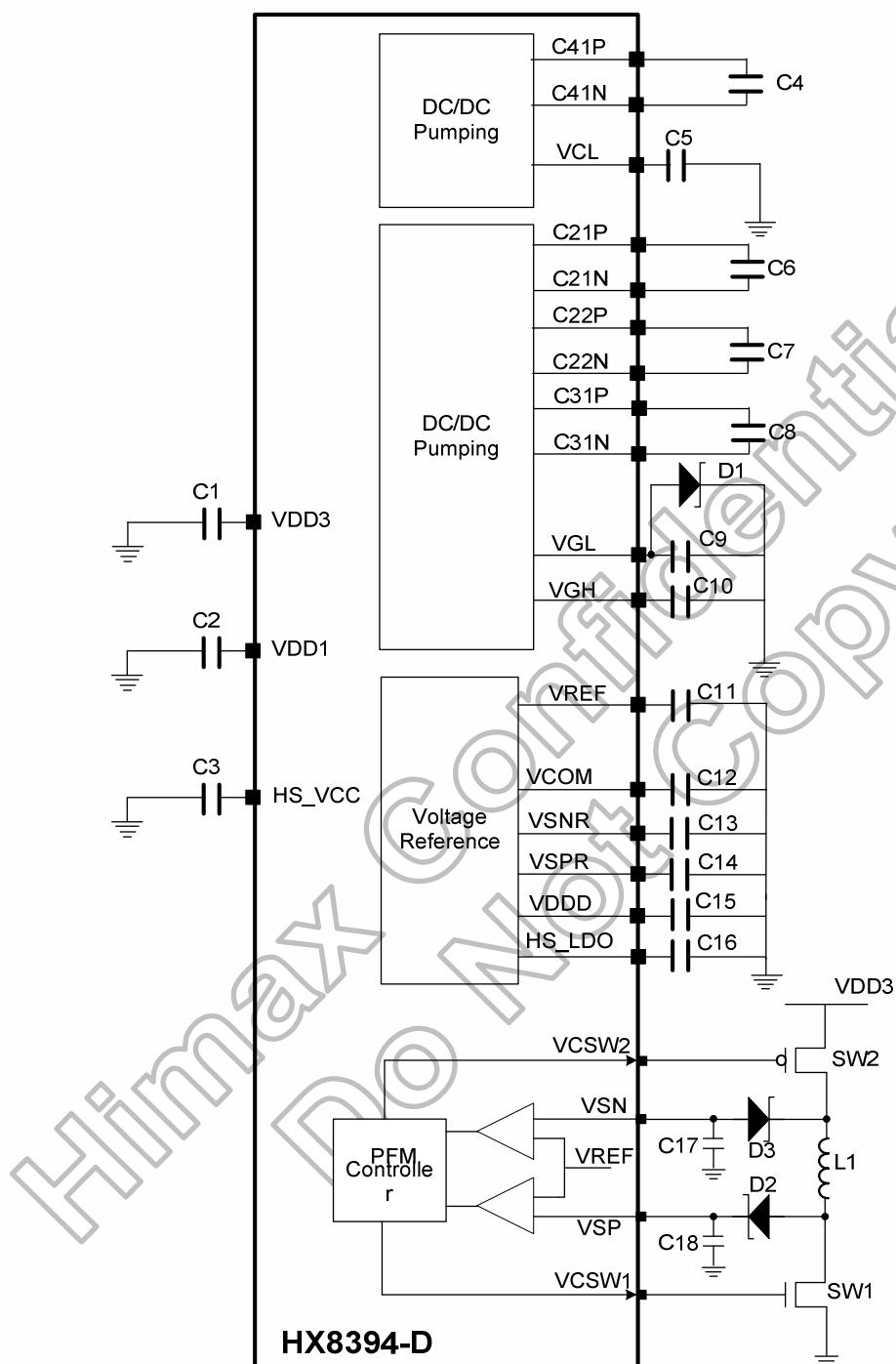
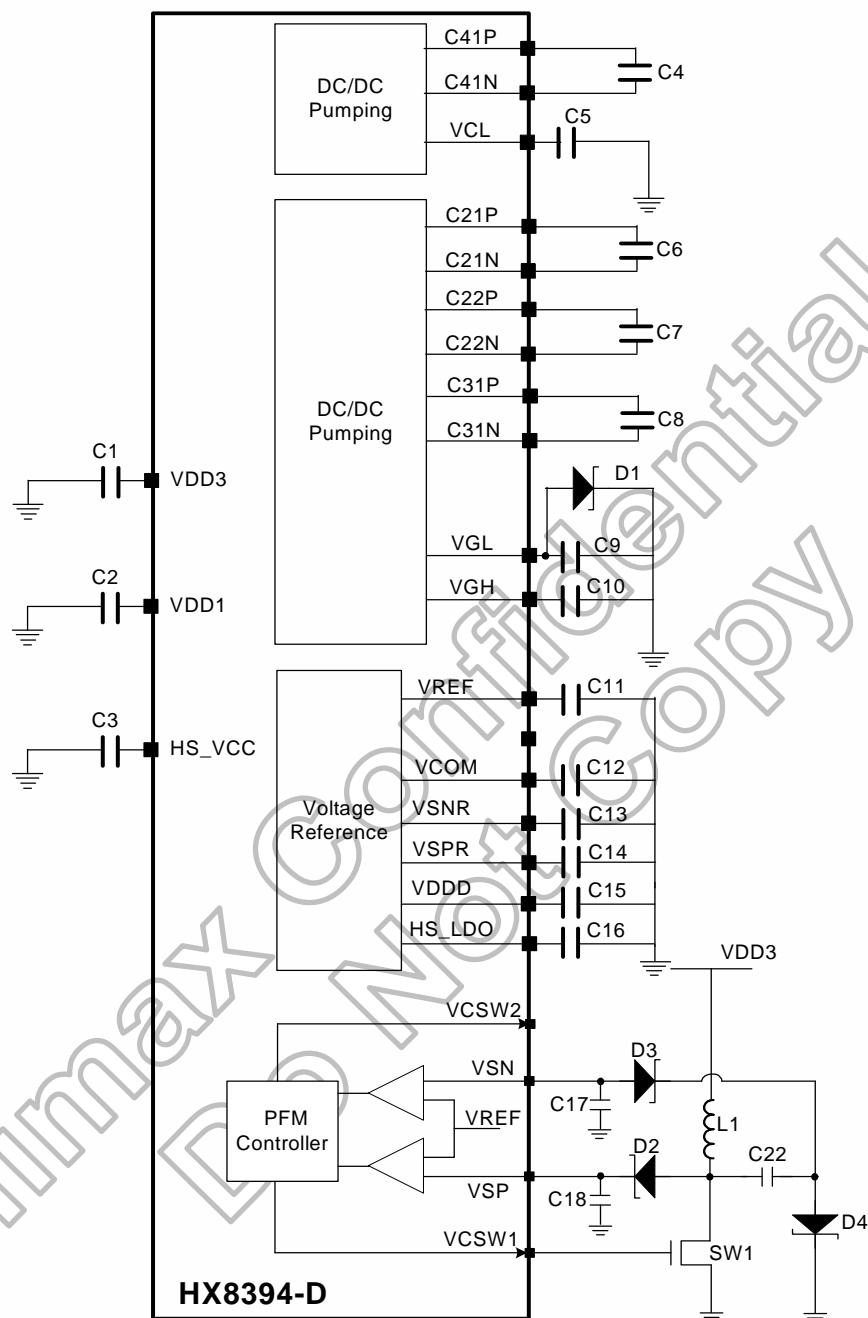


Figure 5.9: DC/DC converter circuit (PFM Type A)

**Use PFM DC/DC converter (PCCS[1:0] = "10") and (POWMOD[1:0]= "01")**



**Figure 5.10: DC/DC converter circuit (PFM Type C)**

### 5.5.3 Use HX5186-A/B/C

The HX5186-A/B/C is highly efficient switching voltage generator circuits that generate the high voltage level VSP/VSN required for source drivers. HX8394-D contains Charge Pump Controller for HX5186, including a comparator for VSP/VSN feedback control. HX5186-A/B/C can provide maximum efficiency and use minimum number of external components. The output voltage of the boost converter can be set from 3.0V to 7.5V (VSP) and -3.0V to -7.5V (VSN)

(PCCS[1:0] = "10") and (POWMOD[1:0]= "10", "11")

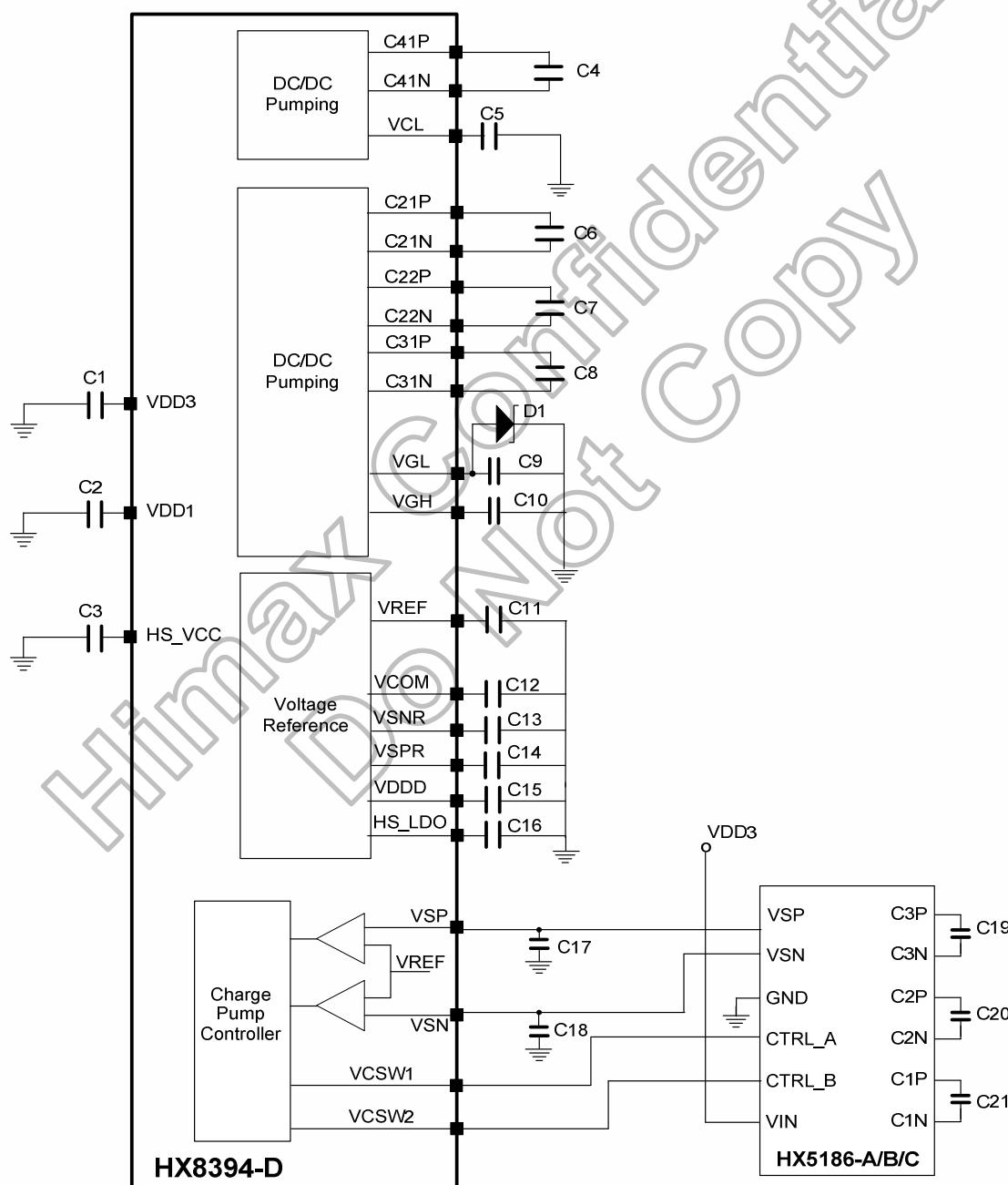


Figure 5.11: DC/DC converter circuit of HX5186-A/B/C

### 5.5.4 Use external VSP,VSN,VGH,VGL circuit

The input voltage range of VSP is from 4.5V ~ 6.75V. The input voltage range of VSN is from -4.5V ~ -6.75V.

(PCCS[1:0] = "11") and VSP,VSN circuit (PCCS[1:0] = "11")

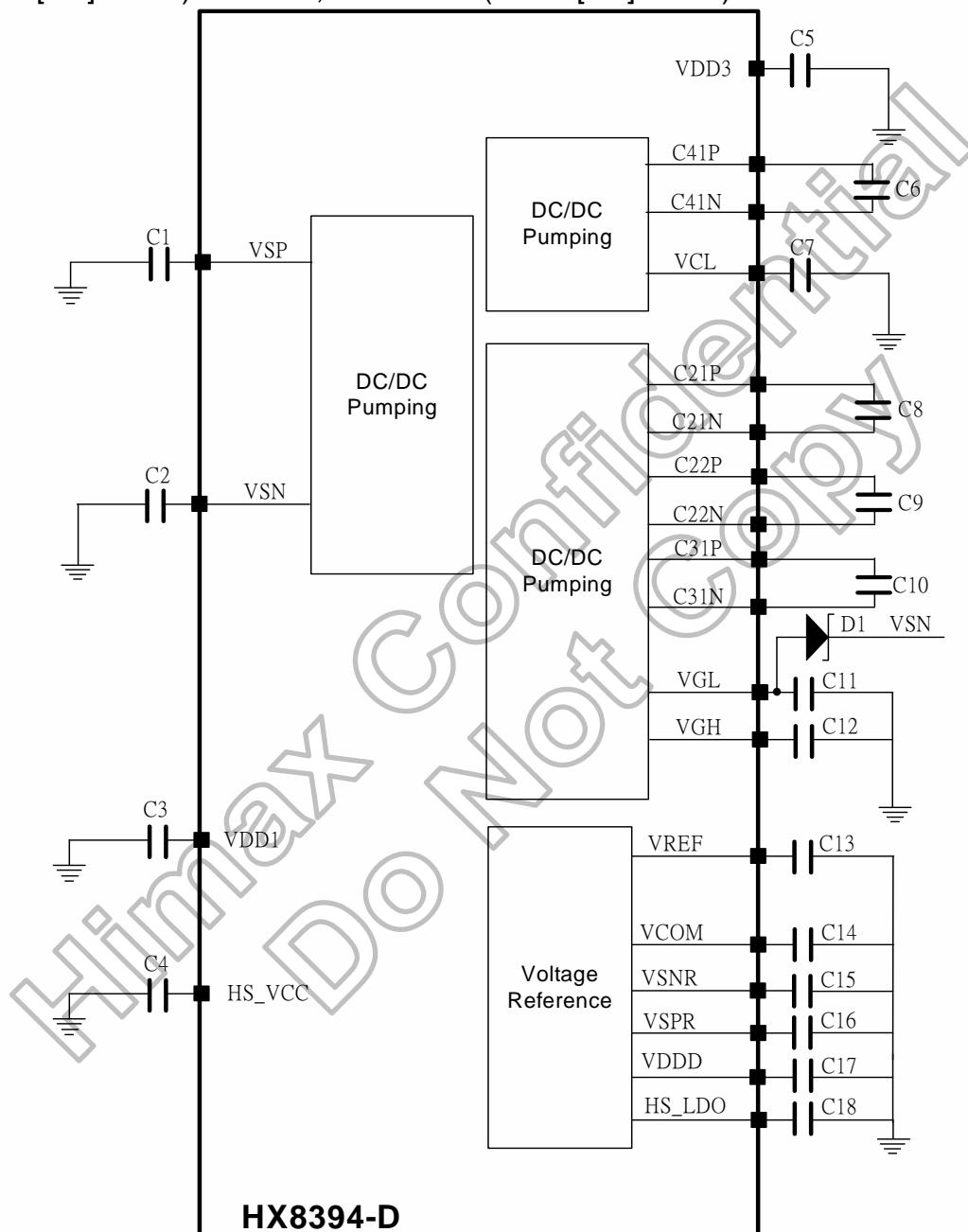


Figure 5.12: DC/DC converter circuit of external VSP/VSN/VGH/VGL

## 5.6 Idle display

The HX8394-D supports an idle display mode. The grayscale level to be used is V0 and V255 with R7, G7, B7 decoding, and the other levels (V1-V254) are halted to reduce power consumption. In idle display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

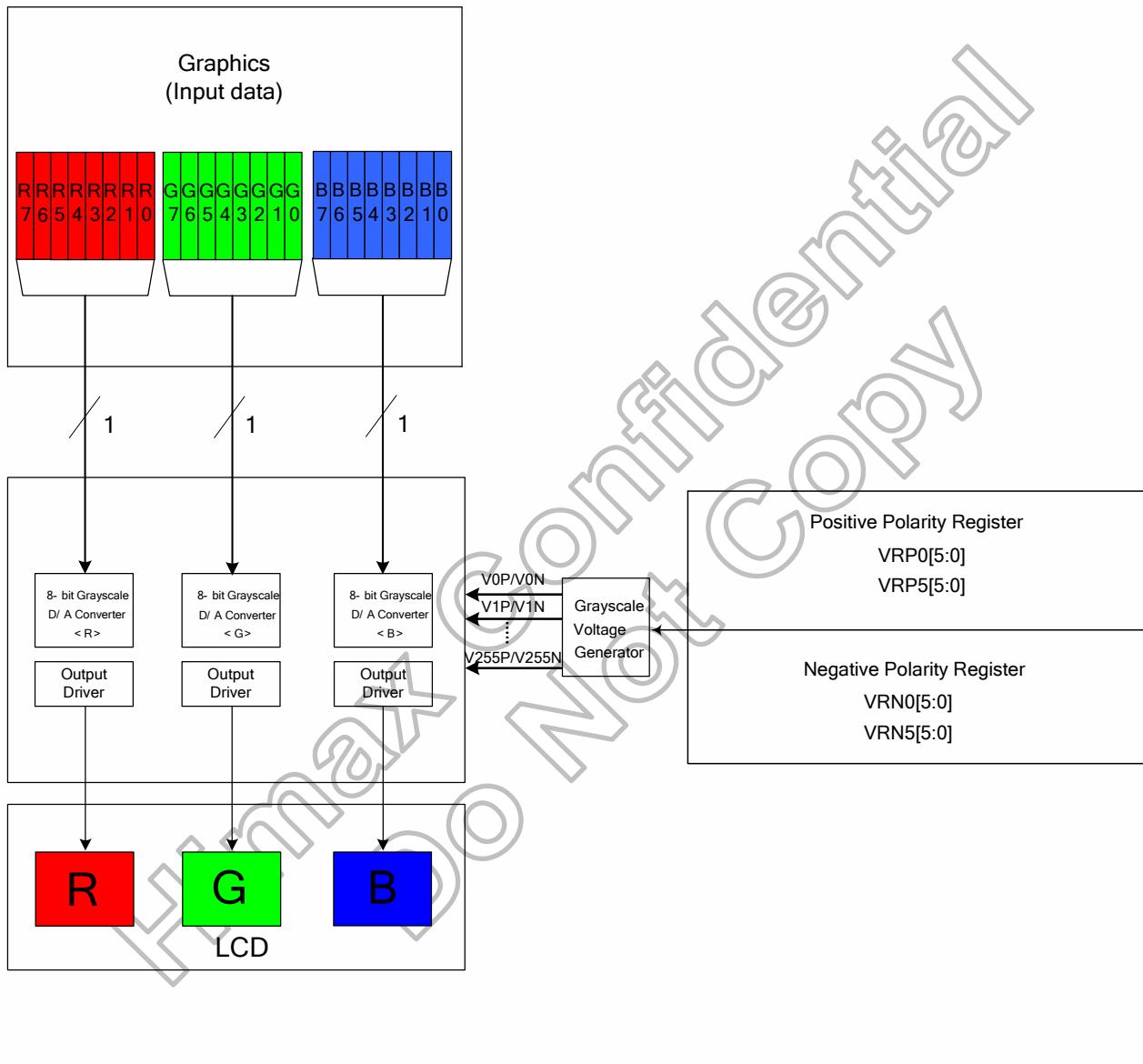
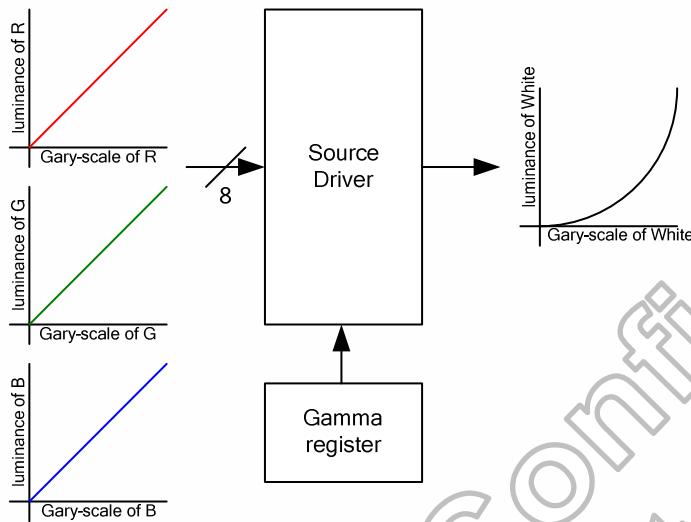


Figure 5.13 : Idle mode grayscale control

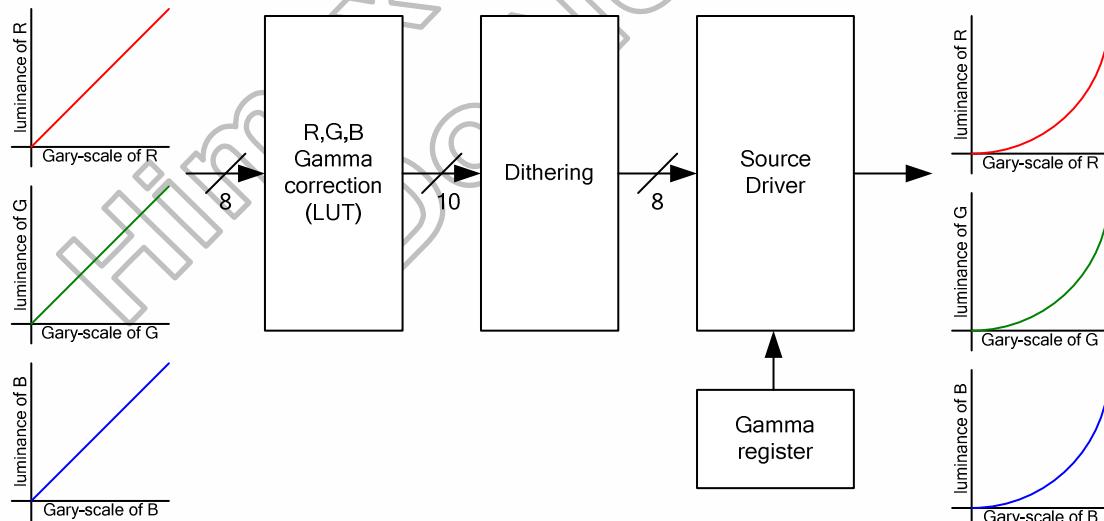
## 5.7 Gamma characteristic correction function

The HX8394-D offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is selected by internal register DGC\_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction



**Figure 5.14: Gamma adjustments different of source driver with digital gamma correction**

The HX8394-D incorporates gamma adjustment function for the 16,777,216-color display (256 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 16 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 512 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

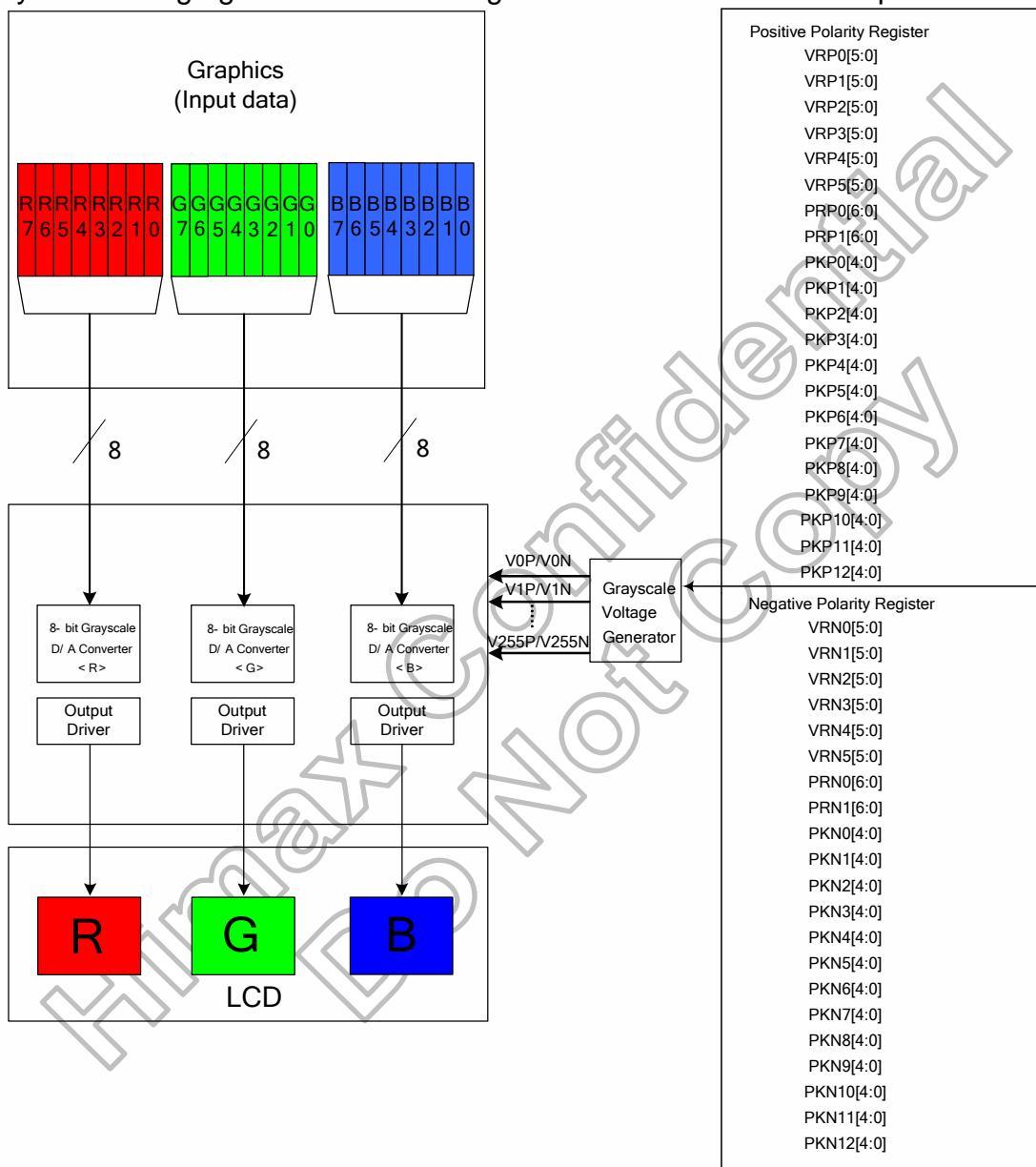


Figure 5.15: Grayscale control

## Gamma-Characteristics adjustment register

The HX8394-D has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

### (1) Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these selector in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

### (2) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 88 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

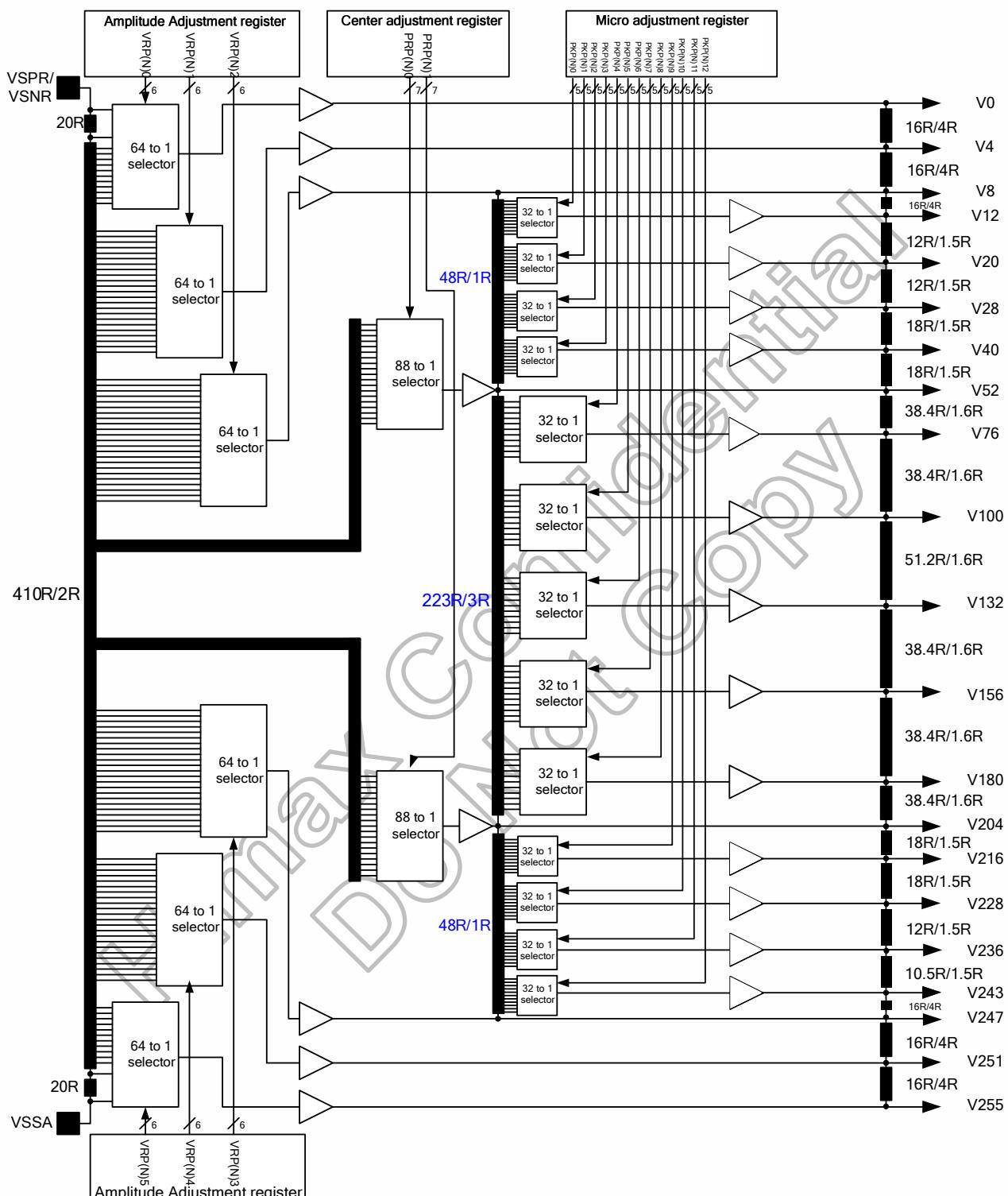
### (3) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~8 and PKP/N\_EX0~3), each of which has 5-bit inputs and generates one reference voltage output.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	88-to-1 selector (voltage level of grayscale 52)
	PRP1 6-0	PRN1 6-0	88-to-1 selector (voltage level of grayscale 204)
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 12)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 20)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 28)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 40)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 76)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 100)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 132)
	PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale 156)
	PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale 180)
	PKP9 4-0	PKN9 4-0	32-to-1 selector (voltage level of grayscale 216)
	PKP10 4-0	PKN10 4-0	32-to-1 selector (voltage level of grayscale 228)
	PKP11 4-0	PKN11 4-0	32-to-1 selector (voltage level of grayscale 236)
	PKP12 4-0	PKN12 4-0	32-to-1 selector (voltage level of grayscale 243)
Offset Adjustment	VRP0 5-0	VRN0 5-0	64-to-1 selector (voltage level of grayscale 0)
	VRP1 5-0	VRN1 5-0	64-to-1 selector (voltage level of grayscale 4)
	VRP2 5-0	VRN2 5-0	64-to-1 selector (voltage level of grayscale 8)
	VRP3 5-0	VRN3 5-0	64-to-1 selector (voltage level of grayscale 247)
	VRP4 5-0	VRN4 5-0	64-to-1 selector (voltage level of grayscale 251)
	VRP5 5-0	VRN5 5-0	64-to-1 selector (voltage level of grayscale 255)

Table 5.3: Gamma-Adjustment registers

### Gamma register stream and 8 to 1 selector



**Figure 5.16: Gamma register stream and gamma reference voltage**

## Variable resistor

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0
000000	0R
000001	20R
000010	22R
000011	24R
•	•
•	•
011101	76R
011110	78R
011111	80R
100000	82R
100001	84R
100010	86R
•	•
•	•
111101	140R
111110	142R
111111	144R

Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1
000000	0R
000001	2R
000010	4R
000011	6R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
000011	6R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	126R

Table 5.4: Offset adjustment 0~5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0
0000000	0R
0000001	2R
0000010	4R
•	•
•	•
1010101	170R
1010110	172R
1010111	174R

Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R
0000001	2R
0000010	4R
•	•
•	•
1010101	170R
1010110	172R
1010111	174R

Table 5.5: Center adjustmen

The grayscale levels are determined by the following formulas:

Reference voltage	Macro adjustment value	VinP0 formula
VinP0	VRP0 5-0 = 000000	VSPR
	VRP0 5-0 = 000001	((450R - 20R) / 450R) * VSPR
	VRP0 5-0 = 000010	((450R - 22R) / 450R) * VSPR
	VRP0 5-0 = 000011	((450R - 24R) / 450R) * VSPR
	VRP0 5-0 = 000100	((450R - 26R) / 450R) * VSPR
	VRP0 5-0 = 000101	((450R - 28R) / 450R) * VSPR
	VRP0 5-0 = 000110	((450R - 30R) / 450R) * VSPR
	VRP0 5-0 = 000111	((450R - 32R) / 450R) * VSPR
	VRP0 5-0 = 001000	((450R - 34R) / 450R) * VSPR
	VRP0 5-0 = 001001	((450R - 36R) / 450R) * VSPR
	VRP0 5-0 = 001010	((450R - 38R) / 450R) * VSPR
	VRP0 5-0 = 001011	((450R - 40R) / 450R) * VSPR
	VRP0 5-0 = 001100	((450R - 42R) / 450R) * VSPR
	VRP0 5-0 = 001101	((450R - 44R) / 450R) * VSPR
	VRP0 5-0 = 001110	((450R - 46R) / 450R) * VSPR
	VRP0 5-0 = 001111	((450R - 48R) / 450R) * VSPR
	VRP0 5-0 = 010000	((450R - 50R) / 450R) * VSPR
	VRP0 5-0 = 010001	((450R - 52R) / 450R) * VSPR
	VRP0 5-0 = 010010	((450R - 54R) / 450R) * VSPR
	VRP0 5-0 = 010011	((450R - 56R) / 450R) * VSPR
	VRP0 5-0 = 010100	((450R - 58R) / 450R) * VSPR
	VRP0 5-0 = 010101	((450R - 60R) / 450R) * VSPR
	VRP0 5-0 = 010110	((450R - 62R) / 450R) * VSPR
	VRP0 5-0 = 010111	((450R - 64R) / 450R) * VSPR
	VRP0 5-0 = 011000	((450R - 66R) / 450R) * VSPR
	VRP0 5-0 = 011001	((450R - 68R) / 450R) * VSPR
	VRP0 5-0 = 011010	((450R - 70R) / 450R) * VSPR
	VRP0 5-0 = 011011	((450R - 72R) / 450R) * VSPR
	VRP0 5-0 = 011100	((450R - 74R) / 450R) * VSPR
	VRP0 5-0 = 011101	((450R - 76R) / 450R) * VSPR
	VRP0 5-0 = 011110	((450R - 78R) / 450R) * VSPR
	VRP0 5-0 = 011111	((450R - 80R) / 450R) * VSPR
	VRP0 5-0 = 100000	((450R - 82R) / 450R) * VSPR
	VRP0 5-0 = 100001	((450R - 84R) / 450R) * VSPR
	VRP0 5-0 = 100010	((450R - 86R) / 450R) * VSPR
	VRP0 5-0 = 100011	((450R - 88R) / 450R) * VSPR
	VRP0 5-0 = 100100	((450R - 90R) / 450R) * VSPR
	VRP0 5-0 = 100101	((450R - 92R) / 450R) * VSPR
	VRP0 5-0 = 100110	((450R - 94R) / 450R) * VSPR
	VRP0 5-0 = 100111	((450R - 96R) / 450R) * VSPR
	VRP0 5-0 = 101000	((450R - 98R) / 450R) * VSPR
	VRP0 5-0 = 101001	((450R - 100R) / 450R) * VSPR
	VRP0 5-0 = 101010	((450R - 102R) / 450R) * VSPR
	VRP0 5-0 = 101011	((450R - 104R) / 450R) * VSPR
	VRP0 5-0 = 101100	((450R - 106R) / 450R) * VSPR
	VRP0 5-0 = 101101	((450R - 108R) / 450R) * VSPR
	VRP0 5-0 = 101110	((450R - 110R) / 450R) * VSPR
	VRP0 5-0 = 101111	((450R - 112R) / 450R) * VSPR
	VRP0 5-0 = 110000	((450R - 114R) / 450R) * VSPR
	VRP0 5-0 = 110001	((450R - 116R) / 450R) * VSPR
	VRP0 5-0 = 110010	((450R - 118R) / 450R) * VSPR
	VRP0 5-0 = 110011	((450R - 120R) / 450R) * VSPR
	VRP0 5-0 = 110100	((450R - 122R) / 450R) * VSPR
	VRP0 5-0 = 110101	((450R - 124R) / 450R) * VSPR
	VRP0 5-0 = 110110	((450R - 126R) / 450R) * VSPR
	VRP0 5-0 = 110111	((450R - 128R) / 450R) * VSPR
	VRP0 5-0 = 111000	((450R - 130R) / 450R) * VSPR
	VRP0 5-0 = 111001	((450R - 132R) / 450R) * VSPR
	VRP0 5-0 = 111010	((450R - 134R) / 450R) * VSPR
	VRP0 5-0 = 111011	((450R - 136R) / 450R) * VSPR
	VRP0 5-0 = 111100	((450R - 138R) / 450R) * VSPR
	VRP0 5-0 = 111101	((450R - 140R) / 450R) * VSPR
	VRP0 5-0 = 111110	((450R - 142R) / 450R) * VSPR
	VRP0 5-0 = 111111	((450R - 144R) / 450R) * VSPR

Table 5.6: VinP0

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Reference voltage	Macro adjustment value	VinP1 formula
VinP1	VRP1 5-0 = 000000	(430R / 450R) * VSPR
	VRP1 5-0 = 000001	((430R - 2R ) / 450R) * VSPR
	VRP1 5-0 = 000010	((430R - 4R ) / 450R) * VSPR
	VRP1 5-0 = 000011	((430R - 6R ) / 450R) * VSPR
	VRP1 5-0 = 000100	((430R - 8R ) / 450R) * VSPR
	VRP1 5-0 = 000101	((430R - 10R ) / 450R) * VSPR
	VRP1 5-0 = 000110	((430R - 12R ) / 450R) * VSPR
	VRP1 5-0 = 000111	((430R - 14R ) / 450R) * VSPR
	VRP1 5-0 = 001000	((430R - 16R ) / 450R) * VSPR
	VRP1 5-0 = 001001	((430R - 18R ) / 450R) * VSPR
	VRP1 5-0 = 001010	((430R - 20R ) / 450R) * VSPR
	VRP1 5-0 = 001011	((430R - 22R ) / 450R) * VSPR
	VRP1 5-0 = 001100	((430R - 24R ) / 450R) * VSPR
	VRP1 5-0 = 001101	((430R - 26R ) / 450R) * VSPR
	VRP1 5-0 = 001110	((430R - 28R ) / 450R) * VSPR
	VRP1 5-0 = 001111	((430R - 30R ) / 450R) * VSPR
	VRP1 5-0 = 010000	((430R - 32R ) / 450R) * VSPR
	VRP1 5-0 = 010001	((430R - 34R ) / 450R) * VSPR
	VRP1 5-0 = 010010	((430R - 36R ) / 450R) * VSPR
	VRP1 5-0 = 010011	((430R - 38R ) / 450R) * VSPR
	VRP1 5-0 = 010100	((430R - 40R ) / 450R) * VSPR
	VRP1 5-0 = 010101	((430R - 42R ) / 450R) * VSPR
	VRP1 5-0 = 010110	((430R - 44R ) / 450R) * VSPR
	VRP1 5-0 = 010111	((430R - 46R ) / 450R) * VSPR
	VRP1 5-0 = 011000	((430R - 48R ) / 450R) * VSPR
	VRP1 5-0 = 011001	((430R - 50R ) / 450R) * VSPR
	VRP1 5-0 = 011010	((430R - 52R ) / 450R) * VSPR
	VRP1 5-0 = 011011	((430R - 54R ) / 450R) * VSPR
	VRP1 5-0 = 011100	((430R - 56R ) / 450R) * VSPR
	VRP1 5-0 = 011101	((430R - 58R ) / 450R) * VSPR
	VRP1 5-0 = 011110	((430R - 60R ) / 450R) * VSPR
	VRP1 5-0 = 011111	((430R - 62R ) / 450R) * VSPR
	VRP1 5-0 = 100000	((430R - 64R ) / 450R) * VSPR
	VRP1 5-0 = 100001	((430R - 66R ) / 450R) * VSPR
	VRP1 5-0 = 100010	((430R - 68R ) / 450R) * VSPR
	VRP1 5-0 = 100011	((430R - 70R ) / 450R) * VSPR
	VRP1 5-0 = 100100	((430R - 72R ) / 450R) * VSPR
	VRP1 5-0 = 100101	((430R - 74R ) / 450R) * VSPR
	VRP1 5-0 = 100110	((430R - 76R ) / 450R) * VSPR
	VRP1 5-0 = 100111	((430R - 78R ) / 450R) * VSPR
	VRP1 5-0 = 101000	((430R - 80R ) / 450R) * VSPR
	VRP1 5-0 = 101001	((430R - 82R ) / 450R) * VSPR
	VRP1 5-0 = 101010	((430R - 84R ) / 450R) * VSPR
	VRP1 5-0 = 101011	((430R - 86R ) / 450R) * VSPR
	VRP1 5-0 = 101100	((430R - 88R ) / 450R) * VSPR
	VRP1 5-0 = 101101	((430R - 90R ) / 450R) * VSPR
	VRP1 5-0 = 101110	((430R - 92R ) / 450R) * VSPR
	VRP1 5-0 = 101111	((430R - 94R ) / 450R) * VSPR
	VRP1 5-0 = 110000	((430R - 96R ) / 450R) * VSPR
	VRP1 5-0 = 110001	((430R - 98R ) / 450R) * VSPR
	VRP1 5-0 = 110010	((430R - 100R ) / 450R) * VSPR
	VRP1 5-0 = 110011	((430R - 102R ) / 450R) * VSPR
	VRP1 5-0 = 110100	((430R - 104R ) / 450R) * VSPR
	VRP1 5-0 = 110101	((430R - 106R ) / 450R) * VSPR
	VRP1 5-0 = 110110	((430R - 108R ) / 450R) * VSPR
	VRP1 5-0 = 110111	((430R - 110R ) / 450R) * VSPR
	VRP1 5-0 = 111000	((430R - 112R ) / 450R) * VSPR
	VRP1 5-0 = 111001	((430R - 114R ) / 450R) * VSPR
	VRP1 5-0 = 111010	((430R - 116R ) / 450R) * VSPR
	VRP1 5-0 = 111011	((430R - 118R ) / 450R) * VSPR
	VRP1 5-0 = 111100	((430R - 120R ) / 450R) * VSPR
	VRP1 5-0 = 111101	((430R - 122R ) / 450R) * VSPR
	VRP1 5-0 = 111110	((430R - 124R ) / 450R) * VSPR
	VRP1 5-0 = 111111	((430R - 126R ) / 450R) * VSPR

Table 5.7: VinP1

Reference voltage	Macro adjustment value	VinP2 formula
VinP2	VRP2 5-0 = 000000	(420R / 450R) * VSPR
	VRP2 5-0 = 000001	((420R - 2R ) / 450R) * VSPR
	VRP2 5-0 = 000010	((420R - 4R ) / 450R) * VSPR
	VRP2 5-0 = 000011	((420R - 6R ) / 450R) * VSPR
	VRP2 5-0 = 000100	((420R - 8R ) / 450R) * VSPR
	VRP2 5-0 = 000101	((420R - 10R ) / 450R) * VSPR
	VRP2 5-0 = 000110	((420R - 12R ) / 450R) * VSPR
	VRP2 5-0 = 000111	((420R - 14R ) / 450R) * VSPR
	VRP2 5-0 = 001000	((420R - 16R ) / 450R) * VSPR
	VRP2 5-0 = 001001	((420R - 18R ) / 450R) * VSPR
	VRP2 5-0 = 001010	((420R - 20R ) / 450R) * VSPR
	VRP2 5-0 = 001011	((420R - 22R ) / 450R) * VSPR
	VRP2 5-0 = 001100	((420R - 24R ) / 450R) * VSPR
	VRP2 5-0 = 001101	((420R - 26R ) / 450R) * VSPR
	VRP2 5-0 = 001110	((420R - 28R ) / 450R) * VSPR
	VRP2 5-0 = 001111	((420R - 30R ) / 450R) * VSPR
	VRP2 5-0 = 010000	((420R - 32R ) / 450R) * VSPR
	VRP2 5-0 = 010001	((420R - 34R ) / 450R) * VSPR
	VRP2 5-0 = 010010	((420R - 36R ) / 450R) * VSPR
	VRP2 5-0 = 010011	((420R - 38R ) / 450R) * VSPR
	VRP2 5-0 = 010100	((420R - 40R ) / 450R) * VSPR
	VRP2 5-0 = 010101	((420R - 42R ) / 450R) * VSPR
	VRP2 5-0 = 010110	((420R - 44R ) / 450R) * VSPR
	VRP2 5-0 = 010111	((420R - 46R ) / 450R) * VSPR
	VRP2 5-0 = 011000	((420R - 48R ) / 450R) * VSPR
	VRP2 5-0 = 011001	((420R - 50R ) / 450R) * VSPR
	VRP2 5-0 = 011010	((420R - 52R ) / 450R) * VSPR
	VRP2 5-0 = 011011	((420R - 54R ) / 450R) * VSPR
	VRP2 5-0 = 011100	((420R - 56R ) / 450R) * VSPR
	VRP2 5-0 = 011101	((420R - 58R ) / 450R) * VSPR
	VRP2 5-0 = 011110	((420R - 60R ) / 450R) * VSPR
	VRP2 5-0 = 011111	((420R - 62R ) / 450R) * VSPR
	VRP2 5-0 = 100000	((420R - 64R ) / 450R) * VSPR
	VRP2 5-0 = 100001	((420R - 66R ) / 450R) * VSPR
	VRP2 5-0 = 100010	((420R - 68R ) / 450R) * VSPR
	VRP2 5-0 = 100011	((420R - 70R ) / 450R) * VSPR
	VRP2 5-0 = 100100	((420R - 72R ) / 450R) * VSPR
	VRP2 5-0 = 100101	((420R - 74R ) / 450R) * VSPR
	VRP2 5-0 = 100110	((420R - 76R ) / 450R) * VSPR
	VRP2 5-0 = 100111	((420R - 78R ) / 450R) * VSPR
	VRP2 5-0 = 101000	((420R - 80R ) / 450R) * VSPR
	VRP2 5-0 = 101001	((420R - 82R ) / 450R) * VSPR
	VRP2 5-0 = 101010	((420R - 84R ) / 450R) * VSPR
	VRP2 5-0 = 101011	((420R - 86R ) / 450R) * VSPR
	VRP2 5-0 = 101100	((420R - 88R ) / 450R) * VSPR
	VRP2 5-0 = 101101	((420R - 90R ) / 450R) * VSPR
	VRP2 5-0 = 101110	((420R - 92R ) / 450R) * VSPR
	VRP2 5-0 = 101111	((420R - 94R ) / 450R) * VSPR
	VRP2 5-0 = 110000	((420R - 96R ) / 450R) * VSPR
	VRP2 5-0 = 110001	((420R - 98R ) / 450R) * VSPR
	VRP2 5-0 = 110010	((420R - 100R ) / 450R) * VSPR
	VRP2 5-0 = 110011	((420R - 102R ) / 450R) * VSPR
	VRP2 5-0 = 110100	((420R - 104R ) / 450R) * VSPR
	VRP2 5-0 = 110101	((420R - 106R ) / 450R) * VSPR
	VRP2 5-0 = 110110	((420R - 108R ) / 450R) * VSPR
	VRP2 5-0 = 110111	((420R - 110R ) / 450R) * VSPR
	VRP2 5-0 = 111000	((420R - 112R ) / 450R) * VSPR
	VRP2 5-0 = 111001	((420R - 114R ) / 450R) * VSPR
	VRP2 5-0 = 111010	((420R - 116R ) / 450R) * VSPR
	VRP2 5-0 = 111011	((420R - 118R ) / 450R) * VSPR
	VRP2 5-0 = 111100	((420R - 120R ) / 450R) * VSPR
	VRP2 5-0 = 111101	((420R - 122R ) / 450R) * VSPR
	VRP2 5-0 = 111110	((420R - 124R ) / 450R) * VSPR
	VRP2 5-0 = 111111	((420R - 126R ) / 450R) * VSPR

Table 5.8: VinP2

Reference voltage	Macro adjustment value	VinP18 formula
VinP18	VRP3 5-0 = 000000	((156R / 450R) * VSPR
	VRP3 5-0 = 000001	((156R - 2R ) / 450R) * VSPR
	VRP3 5-0 = 000010	((156R - 4R ) / 450R) * VSPR
	VRP3 5-0 = 000011	((156R - 6R ) / 450R) * VSPR
	VRP3 5-0 = 000100	((156R - 8R ) / 450R) * VSPR
	VRP3 5-0 = 000101	((156R - 10R ) / 450R) * VSPR
	VRP3 5-0 = 000110	((156R - 12R ) / 450R) * VSPR
	VRP3 5-0 = 000111	((156R - 14R ) / 450R) * VSPR
	VRP3 5-0 = 001000	((156R - 16R ) / 450R) * VSPR
	VRP3 5-0 = 001001	((156R - 18R ) / 450R) * VSPR
	VRP3 5-0 = 001010	((156R - 20R ) / 450R) * VSPR
	VRP3 5-0 = 001011	((156R - 22R ) / 450R) * VSPR
	VRP3 5-0 = 001100	((156R - 24R ) / 450R) * VSPR
	VRP3 5-0 = 001101	((156R - 26R ) / 450R) * VSPR
	VRP3 5-0 = 001110	((156R - 28R ) / 450R) * VSPR
	VRP3 5-0 = 001111	((156R - 30R ) / 450R) * VSPR
	VRP3 5-0 = 010000	((156R - 32R ) / 450R) * VSPR
	VRP3 5-0 = 010001	((156R - 34R ) / 450R) * VSPR
	VRP3 5-0 = 010010	((156R - 36R ) / 450R) * VSPR
	VRP3 5-0 = 010011	((156R - 38R ) / 450R) * VSPR
	VRP3 5-0 = 010100	((156R - 40R ) / 450R) * VSPR
	VRP3 5-0 = 010101	((156R - 42R ) / 450R) * VSPR
	VRP3 5-0 = 010110	((156R - 44R ) / 450R) * VSPR
	VRP3 5-0 = 010111	((156R - 46R ) / 450R) * VSPR
	VRP3 5-0 = 011000	((156R - 48R ) / 450R) * VSPR
	VRP3 5-0 = 011001	((156R - 50R ) / 450R) * VSPR
	VRP3 5-0 = 011010	((156R - 52R ) / 450R) * VSPR
	VRP3 5-0 = 011011	((156R - 54R ) / 450R) * VSPR
	VRP3 5-0 = 011100	((156R - 56R ) / 450R) * VSPR
	VRP3 5-0 = 011101	((156R - 58R ) / 450R) * VSPR
	VRP3 5-0 = 011110	((156R - 60R ) / 450R) * VSPR
	VRP3 5-0 = 011111	((156R - 62R ) / 450R) * VSPR
	VRP3 5-0 = 100000	((156R - 64R ) / 450R) * VSPR
	VRP3 5-0 = 100001	((156R - 66R ) / 450R) * VSPR
	VRP3 5-0 = 100010	((156R - 68R ) / 450R) * VSPR
	VRP3 5-0 = 100011	((156R - 70R ) / 450R) * VSPR
	VRP3 5-0 = 100100	((156R - 72R ) / 450R) * VSPR
	VRP3 5-0 = 100101	((156R - 74R ) / 450R) * VSPR
	VRP3 5-0 = 100110	((156R - 76R ) / 450R) * VSPR
	VRP3 5-0 = 100111	((156R - 78R ) / 450R) * VSPR
	VRP3 5-0 = 101000	((156R - 80R ) / 450R) * VSPR
	VRP3 5-0 = 101001	((156R - 82R ) / 450R) * VSPR
	VRP3 5-0 = 101010	((156R - 84R ) / 450R) * VSPR
	VRP3 5-0 = 101011	((156R - 86R ) / 450R) * VSPR
	VRP3 5-0 = 101100	((156R - 88R ) / 450R) * VSPR
	VRP3 5-0 = 101101	((156R - 90R ) / 450R) * VSPR
	VRP3 5-0 = 101110	((156R - 92R ) / 450R) * VSPR
	VRP3 5-0 = 101111	((156R - 94R ) / 450R) * VSPR
	VRP3 5-0 = 110000	((156R - 96R ) / 450R) * VSPR
	VRP3 5-0 = 110001	((156R - 98R ) / 450R) * VSPR
	VRP3 5-0 = 110010	((156R - 100R ) / 450R) * VSPR
	VRP3 5-0 = 110011	((156R - 102R ) / 450R) * VSPR
	VRP3 5-0 = 110100	((156R - 104R ) / 450R) * VSPR
	VRP3 5-0 = 110101	((156R - 106R ) / 450R) * VSPR
	VRP3 5-0 = 110110	((156R - 108R ) / 450R) * VSPR
	VRP3 5-0 = 110111	((156R - 110R ) / 450R) * VSPR
	VRP3 5-0 = 111000	((156R - 112R ) / 450R) * VSPR
	VRP3 5-0 = 111001	((156R - 114R ) / 450R) * VSPR
	VRP3 5-0 = 111010	((156R - 116R ) / 450R) * VSPR
	VRP3 5-0 = 111011	((156R - 118R ) / 450R) * VSPR
	VRP3 5-0 = 111100	((156R - 120R ) / 450R) * VSPR
	VRP3 5-0 = 111101	((156R - 122R ) / 450R) * VSPR
	VRP3 5-0 = 111110	((156R - 124R ) / 450R) * VSPR
	VRP3 5-0 = 111111	((156R - 126R ) / 450R) * VSPR

Table 5.9: VinP18

Reference voltage	Macro adjustment value	VinP19 formula
VinP19	VRP4 5-0 = 000000	((146R / 450R) * VSPR
	VRP4 5-0 = 000001	((146R - 2R ) / 450R) * VSPR
	VRP4 5-0 = 000010	((146R - 4R ) / 450R) * VSPR
	VRP4 5-0 = 000011	((146R - 6R ) / 450R) * VSPR
	VRP4 5-0 = 000100	((146R - 8R ) / 450R) * VSPR
	VRP4 5-0 = 000101	((146R - 10R ) / 450R) * VSPR
	VRP4 5-0 = 000110	((146R - 12R ) / 450R) * VSPR
	VRP4 5-0 = 000111	((146R - 14R ) / 450R) * VSPR
	VRP4 5-0 = 001000	((146R - 16R ) / 450R) * VSPR
	VRP4 5-0 = 001001	((146R - 18R ) / 450R) * VSPR
	VRP4 5-0 = 001010	((146R - 20R ) / 450R) * VSPR
	VRP4 5-0 = 001011	((146R - 22R ) / 450R) * VSPR
	VRP4 5-0 = 001100	((146R - 24R ) / 450R) * VSPR
	VRP4 5-0 = 001101	((146R - 26R ) / 450R) * VSPR
	VRP4 5-0 = 001110	((146R - 28R ) / 450R) * VSPR
	VRP4 5-0 = 001111	((146R - 30R ) / 450R) * VSPR
	VRP4 5-0 = 010000	((146R - 32R ) / 450R) * VSPR
	VRP4 5-0 = 010001	((146R - 34R ) / 450R) * VSPR
	VRP4 5-0 = 010010	((146R - 36R ) / 450R) * VSPR
	VRP4 5-0 = 010011	((146R - 38R ) / 450R) * VSPR
	VRP4 5-0 = 010100	((146R - 40R ) / 450R) * VSPR
	VRP4 5-0 = 010101	((146R - 42R ) / 450R) * VSPR
	VRP4 5-0 = 010110	((146R - 44R ) / 450R) * VSPR
	VRP4 5-0 = 010111	((146R - 46R ) / 450R) * VSPR
	VRP4 5-0 = 011000	((146R - 48R ) / 450R) * VSPR
	VRP4 5-0 = 011001	((146R - 50R ) / 450R) * VSPR
	VRP4 5-0 = 011010	((146R - 52R ) / 450R) * VSPR
	VRP4 5-0 = 011011	((146R - 54R ) / 450R) * VSPR
	VRP4 5-0 = 011100	((146R - 56R ) / 450R) * VSPR
	VRP4 5-0 = 011101	((146R - 58R ) / 450R) * VSPR
	VRP4 5-0 = 011110	((146R - 60R ) / 450R) * VSPR
	VRP4 5-0 = 011111	((146R - 62R ) / 450R) * VSPR
	VRP4 5-0 = 100000	((146R - 64R ) / 450R) * VSPR
	VRP4 5-0 = 100001	((146R - 66R ) / 450R) * VSPR
	VRP4 5-0 = 100010	((146R - 68R ) / 450R) * VSPR
	VRP4 5-0 = 100011	((146R - 70R ) / 450R) * VSPR
	VRP4 5-0 = 100100	((146R - 72R ) / 450R) * VSPR
	VRP4 5-0 = 100101	((146R - 74R ) / 450R) * VSPR
	VRP4 5-0 = 100110	((146R - 76R ) / 450R) * VSPR
	VRP4 5-0 = 100111	((146R - 78R ) / 450R) * VSPR
	VRP4 5-0 = 101000	((146R - 80R ) / 450R) * VSPR
	VRP4 5-0 = 101001	((146R - 82R ) / 450R) * VSPR
	VRP4 5-0 = 101010	((146R - 84R ) / 450R) * VSPR
	VRP4 5-0 = 101011	((146R - 86R ) / 450R) * VSPR
	VRP4 5-0 = 101100	((146R - 88R ) / 450R) * VSPR
	VRP4 5-0 = 101101	((146R - 90R ) / 450R) * VSPR
	VRP4 5-0 = 101110	((146R - 92R ) / 450R) * VSPR
	VRP4 5-0 = 101111	((146R - 94R ) / 450R) * VSPR
	VRP4 5-0 = 110000	((146R - 96R ) / 450R) * VSPR
	VRP4 5-0 = 110001	((146R - 98R ) / 450R) * VSPR
	VRP4 5-0 = 110010	((146R - 100R ) / 450R) * VSPR
	VRP4 5-0 = 110011	((146R - 102R ) / 450R) * VSPR
	VRP4 5-0 = 110100	((146R - 104R ) / 450R) * VSPR
	VRP4 5-0 = 110101	((146R - 106R ) / 450R) * VSPR
	VRP4 5-0 = 110110	((146R - 108R ) / 450R) * VSPR
	VRP4 5-0 = 110111	((146R - 110R ) / 450R) * VSPR
	VRP4 5-0 = 111000	((146R - 112R ) / 450R) * VSPR
	VRP4 5-0 = 111001	((146R - 114R ) / 450R) * VSPR
	VRP4 5-0 = 111010	((146R - 116R ) / 450R) * VSPR
	VRP4 5-0 = 111011	((146R - 118R ) / 450R) * VSPR
	VRP4 5-0 = 111100	((146R - 120R ) / 450R) * VSPR
	VRP4 5-0 = 111101	((146R - 122R ) / 450R) * VSPR
	VRP4 5-0 = 111110	((146R - 124R ) / 450R) * VSPR
	VRP4 5-0 = 111111	((146R - 126R ) / 450R) * VSPR

Table 5.10: VinP19

Reference voltage	Macro adjustment value	VinP20 formula
VinP20	VRP5 5-0 = 000000	((144R / 450R) * VSPR
	VRP5 5-0 = 000001	((144R - 2R) / 450R) * VSPR
	VRP5 5-0 = 000010	((144R - 4R) / 450R) * VSPR
	VRP5 5-0 = 000011	((144R - 6R) / 450R) * VSPR
	VRP5 5-0 = 000100	((144R - 8R) / 450R) * VSPR
	VRP5 5-0 = 000101	((144R - 10R) / 450R) * VSPR
	VRP5 5-0 = 000110	((144R - 12R) / 450R) * VSPR
	VRP5 5-0 = 000111	((144R - 14R) / 450R) * VSPR
	VRP5 5-0 = 001000	((144R - 16R) / 450R) * VSPR
	VRP5 5-0 = 001001	((144R - 18R) / 450R) * VSPR
	VRP5 5-0 = 001010	((144R - 20R) / 450R) * VSPR
	VRP5 5-0 = 001011	((144R - 22R) / 450R) * VSPR
	VRP5 5-0 = 001100	((144R - 24R) / 450R) * VSPR
	VRP5 5-0 = 001101	((144R - 26R) / 450R) * VSPR
	VRP5 5-0 = 001110	((144R - 28R) / 450R) * VSPR
	VRP5 5-0 = 001111	((144R - 30R) / 450R) * VSPR
	VRP5 5-0 = 010000	((144R - 32R) / 450R) * VSPR
	VRP5 5-0 = 010001	((144R - 34R) / 450R) * VSPR
	VRP5 5-0 = 010010	((144R - 36R) / 450R) * VSPR
	VRP5 5-0 = 010011	((144R - 38R) / 450R) * VSPR
	VRP5 5-0 = 010100	((144R - 40R) / 450R) * VSPR
	VRP5 5-0 = 010101	((144R - 42R) / 450R) * VSPR
	VRP5 5-0 = 010110	((144R - 44R) / 450R) * VSPR
	VRP5 5-0 = 010111	((144R - 46R) / 450R) * VSPR
	VRP5 5-0 = 011000	((144R - 48R) / 450R) * VSPR
	VRP5 5-0 = 011001	((144R - 50R) / 450R) * VSPR
	VRP5 5-0 = 011010	((144R - 52R) / 450R) * VSPR
	VRP5 5-0 = 011011	((144R - 54R) / 450R) * VSPR
	VRP5 5-0 = 011100	((144R - 56R) / 450R) * VSPR
	VRP5 5-0 = 011101	((144R - 58R) / 450R) * VSPR
	VRP5 5-0 = 011110	((144R - 60R) / 450R) * VSPR
	VRP5 5-0 = 011111	((144R - 62R) / 450R) * VSPR
	VRP5 5-0 = 100000	((144R - 64R) / 450R) * VSPR
	VRP5 5-0 = 100001	((144R - 66R) / 450R) * VSPR
	VRP5 5-0 = 100010	((144R - 68R) / 450R) * VSPR
	VRP5 5-0 = 100011	((144R - 70R) / 450R) * VSPR
	VRP5 5-0 = 100100	((144R - 72R) / 450R) * VSPR
	VRP5 5-0 = 100101	((144R - 74R) / 450R) * VSPR
	VRP5 5-0 = 100110	((144R - 76R) / 450R) * VSPR
	VRP5 5-0 = 100111	((144R - 78R) / 450R) * VSPR
	VRP5 5-0 = 101000	((144R - 80R) / 450R) * VSPR
	VRP5 5-0 = 101001	((144R - 82R) / 450R) * VSPR
	VRP5 5-0 = 101010	((144R - 84R) / 450R) * VSPR
	VRP5 5-0 = 101011	((144R - 86R) / 450R) * VSPR
	VRP5 5-0 = 101100	((144R - 88R) / 450R) * VSPR
	VRP5 5-0 = 101101	((144R - 90R) / 450R) * VSPR
	VRP5 5-0 = 101110	((144R - 92R) / 450R) * VSPR
	VRP5 5-0 = 101111	((144R - 94R) / 450R) * VSPR
	VRP5 5-0 = 110000	((144R - 96R) / 450R) * VSPR
	VRP5 5-0 = 110001	((144R - 98R) / 450R) * VSPR
	VRP5 5-0 = 110010	((144R - 100R) / 450R) * VSPR
	VRP5 5-0 = 110011	((144R - 102R) / 450R) * VSPR
	VRP5 5-0 = 110100	((144R - 104R) / 450R) * VSPR
	VRP5 5-0 = 110101	((144R - 106R) / 450R) * VSPR
	VRP5 5-0 = 110110	((144R - 108R) / 450R) * VSPR
	VRP5 5-0 = 110111	((144R - 110R) / 450R) * VSPR
	VRP5 5-0 = 111000	((144R - 112R) / 450R) * VSPR
	VRP5 5-0 = 111001	((144R - 114R) / 450R) * VSPR
	VRP5 5-0 = 111010	((144R - 116R) / 450R) * VSPR
	VRP5 5-0 = 111011	((144R - 118R) / 450R) * VSPR
	VRP5 5-0 = 111100	((144R - 120R) / 450R) * VSPR
	VRP5 5-0 = 111101	((144R - 122R) / 450R) * VSPR
	VRP5 5-0 = 111110	((144R - 124R) / 450R) * VSPR
	VRP5 5-0 = 111111	VGSP

Table 5.11: VinP20

Reference voltage	Macro adjustment value	VinP7 formula
VinP7	PRP0 6-0 = 0000000	((350R / 450R) * VSPR)
	PRP0 6-0 = 0000001	((350R - 2R) / 450R) * VSPR
	PRP0 6-0 = 0000010	((350R - 4R) / 450R) * VSPR
	PRP0 6-0 = 0000011	((350R - 6R) / 450R) * VSPR
	PRP0 6-0 = 00000100	((350R - 8R) / 450R) * VSPR
	PRP0 6-0 = 00000101	((350R - 10R) / 450R) * VSPR
	PRP0 6-0 = 00000110	((350R - 12R) / 450R) * VSPR
	PRP0 6-0 = 00000111	((350R - 14R) / 450R) * VSPR
	PRP0 6-0 = 0001000	((350R - 16R) / 450R) * VSPR
	PRP0 6-0 = 0001001	((350R - 18R) / 450R) * VSPR
	PRP0 6-0 = 0001010	((350R - 20R) / 450R) * VSPR
	PRP0 6-0 = 0001011	((350R - 22R) / 450R) * VSPR
	PRP0 6-0 = 0001100	((350R - 24R) / 450R) * VSPR
	PRP0 6-0 = 0001101	((350R - 26R) / 450R) * VSPR
	PRP0 6-0 = 0001110	((350R - 28R) / 450R) * VSPR
	PRP0 6-0 = 0001111	((350R - 30R) / 450R) * VSPR
	PRP0 6-0 = 0010000	((350R - 32R) / 450R) * VSPR
	PRP0 6-0 = 0010001	((350R - 34R) / 450R) * VSPR
	PRP0 6-0 = 0010010	((350R - 36R) / 450R) * VSPR
	PRP0 6-0 = 0010011	((350R - 38R) / 450R) * VSPR
	PRP0 6-0 = 0010100	((350R - 40R) / 450R) * VSPR
	PRP0 6-0 = 0010101	((350R - 42R) / 450R) * VSPR
	PRP0 6-0 = 0010110	((350R - 44R) / 450R) * VSPR
	PRP0 6-0 = 0010111	((350R - 46R) / 450R) * VSPR
	PRP0 6-0 = 0011000	((350R - 48R) / 450R) * VSPR
	PRP0 6-0 = 0011001	((350R - 50R) / 450R) * VSPR
	PRP0 6-0 = 0011010	((350R - 52R) / 450R) * VSPR
	PRP0 6-0 = 0011011	((350R - 54R) / 450R) * VSPR
	PRP0 6-0 = 0011100	((350R - 56R) / 450R) * VSPR
	PRP0 6-0 = 0011101	((350R - 58R) / 450R) * VSPR
	PRP0 6-0 = 0011110	((350R - 60R) / 450R) * VSPR
	PRP0 6-0 = 0011111	((350R - 62R) / 450R) * VSPR
	PRP0 6-0 = 0100000	((350R - 64R) / 450R) * VSPR
	PRP0 6-0 = 0100001	((350R - 66R) / 450R) * VSPR
	PRP0 6-0 = 0100010	((350R - 68R) / 450R) * VSPR
	PRP0 6-0 = 0100011	((350R - 70R) / 450R) * VSPR
	PRP0 6-0 = 0100100	((350R - 72R) / 450R) * VSPR
	PRP0 6-0 = 0100101	((350R - 74R) / 450R) * VSPR
	PRP0 6-0 = 0100110	((350R - 76R) / 450R) * VSPR
	PRP0 6-0 = 0100111	((350R - 78R) / 450R) * VSPR
	PRP0 6-0 = 0101000	((350R - 80R) / 450R) * VSPR
	PRP0 6-0 = 0101001	((350R - 82R) / 450R) * VSPR
	PRP0 6-0 = 0101010	((350R - 84R) / 450R) * VSPR
	PRP0 6-0 = 0101011	((350R - 86R) / 450R) * VSPR
	PRP0 6-0 = 0101100	((350R - 88R) / 450R) * VSPR
	PRP0 6-0 = 0101101	((350R - 90R) / 450R) * VSPR
	PRP0 6-0 = 0101110	((350R - 92R) / 450R) * VSPR
	PRP0 6-0 = 0101111	((350R - 94R) / 450R) * VSPR
	PRP0 6-0 = 0110000	((350R - 96R) / 450R) * VSPR
	PRP0 6-0 = 0110001	((350R - 98R) / 450R) * VSPR
	PRP0 6-0 = 0110010	((350R - 100R) / 450R) * VSPR
	PRP0 6-0 = 0110011	((350R - 102R) / 450R) * VSPR
	PRP0 6-0 = 0110100	((350R - 104R) / 450R) * VSPR
	PRP0 6-0 = 0110101	((350R - 106R) / 450R) * VSPR
	PRP0 6-0 = 0110110	((350R - 108R) / 450R) * VSPR
	PRP0 6-0 = 0110111	((350R - 110R) / 450R) * VSPR
	PRP0 6-0 = 0111000	((350R - 112R) / 450R) * VSPR
	PRP0 6-0 = 0111001	((350R - 114R) / 450R) * VSPR
	PRP0 6-0 = 0111010	((350R - 116R) / 450R) * VSPR
	PRP0 6-0 = 0111011	((350R - 118R) / 450R) * VSPR
	PRP0 6-0 = 0111100	((350R - 120R) / 450R) * VSPR
	PRP0 6-0 = 0111101	((350R - 122R) / 450R) * VSPR
	PRP0 6-0 = 0111110	((350R - 124R) / 450R) * VSPR
	PRP0 6-0 = 0111111	((350R - 126R) / 450R) * VSPR
PRP0 6-0 = 1000000	((350R - 128R) / 450R) * VSPR	
PRP0 6-0 = 1000001	((350R - 130R) / 450R) * VSPR	
PRP0 6-0 = 1000010	((350R - 132R) / 450R) * VSPR	
PRP0 6-0 = 1000011	((350R - 134R) / 450R) * VSPR	
PRP0 6-0 = 1000100	((350R - 136R) / 450R) * VSPR	

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Reference voltage	Macro adjustment value	VinP7 formula
	PRP0 6-0 = 1000101	$((350R - 138R) / 450R) * VSPR$
	PRP0 6-0 = 1000110	$((350R - 140R) / 450R) * VSPR$
	PRP0 6-0 = 1000111	$((350R - 142R) / 450R) * VSPR$
	PRP0 6-0 = 1001000	$((350R - 144R) / 450R) * VSPR$
	PRP0 6-0 = 1001001	$((350R - 146R) / 450R) * VSPR$
	PRP0 6-0 = 1001010	$((350R - 148R) / 450R) * VSPR$
	PRP0 6-0 = 1001011	$((350R - 150R) / 450R) * VSPR$
	PRP0 6-0 = 1001100	$((350R - 152R) / 450R) * VSPR$
	PRP0 6-0 = 1001101	$((350R - 154R) / 450R) * VSPR$
	PRP0 6-0 = 1001110	$((350R - 156R) / 450R) * VSPR$
	PRP0 6-0 = 1001111	$((350R - 158R) / 450R) * VSPR$
	PRP0 6-0 = 1010000	$((350R - 160R) / 450R) * VSPR$
	PRP0 6-0 = 1010001	$((350R - 162R) / 450R) * VSPR$
	PRP0 6-0 = 1010010	$((350R - 164R) / 450R) * VSPR$
	PRP0 6-0 = 1010011	$((350R - 166R) / 450R) * VSPR$
	PRP0 6-0 = 1010100	$((350R - 168R) / 450R) * VSPR$
	PRP0 6-0 = 1010101	$((350R - 170R) / 450R) * VSPR$
	PRP0 6-0 = 1010110	$((350R - 172R) / 450R) * VSPR$
	PRP0 6-0 = 1010111	$((350R - 174R) / 450R) * VSPR$
	PRP0 6-0 = 1011000	inhibit
	PRP0 6-0 = 1011001	inhibit
	PRP0 6-0 = 1011010	inhibit
	PRP0 6-0 = 1011011	inhibit
	PRP0 6-0 = 1011100	inhibit
	PRP0 6-0 = 1011101	inhibit
	PRP0 6-0 = 1011110	inhibit
	PRP0 6-0 = 1011111	inhibit
	PRP0 6-0 = 1100000	inhibit
	PRP0 6-0 = 1100001	inhibit
	PRP0 6-0 = 1100010	inhibit
	PRP0 6-0 = 1100011	inhibit
	PRP0 6-0 = 1100100	inhibit
	PRP0 6-0 = 1100101	inhibit
	PRP0 6-0 = 1100110	inhibit
	PRP0 6-0 = 1100111	inhibit
	PRP0 6-0 = 1101000	inhibit
	PRP0 6-0 = 1101001	inhibit
	PRP0 6-0 = 1101010	inhibit
	PRP0 6-0 = 1101011	inhibit
	PRP0 6-0 = 1101100	inhibit
	PRP0 6-0 = 1101101	inhibit
	PRP0 6-0 = 1101110	inhibit
	PRP0 6-0 = 1101111	inhibit
	PRP0 6-0 = 1110000	inhibit
	PRP0 6-0 = 1110001	inhibit
	PRP0 6-0 = 1110010	inhibit
	PRP0 6-0 = 1110011	inhibit
	PRP0 6-0 = 1110100	inhibit
	PRP0 6-0 = 1110101	inhibit
	PRP0 6-0 = 1110110	inhibit
	PRP0 6-0 = 1110111	inhibit
	PRP0 6-0 = 1111000	inhibit
	PRP0 6-0 = 1111001	inhibit
	PRP0 6-0 = 1111010	inhibit
	PRP0 6-0 = 1111011	inhibit
	PRP0 6-0 = 1111100	inhibit
	PRP0 6-0 = 1111101	inhibit
	PRP0 6-0 = 1111110	inhibit
	PRP0 6-0 = 1111111	inhibit

Table 5.12: VinP7

Reference voltage	Macro adjustment value	VinP13 formula
VinP13	PRP1 6-0 = 0000000	((274R / 450R) * VSPR)
	PRP1 6-0 = 0000001	((274R - 2R) / 450R) * VSPR
	PRP1 6-0 = 0000010	((274R - 4R) / 450R) * VSPR
	PRP1 6-0 = 0000011	((274R - 6R) / 450R) * VSPR
	PRP1 6-0 = 00000100	((274R - 8R) / 450R) * VSPR
	PRP1 6-0 = 00000101	((274R - 10R) / 450R) * VSPR
	PRP1 6-0 = 00000110	((274R - 12R) / 450R) * VSPR
	PRP1 6-0 = 00000111	((274R - 14R) / 450R) * VSPR
	PRP1 6-0 = 0001000	((274R - 16R) / 450R) * VSPR
	PRP1 6-0 = 0001001	((274R - 18R) / 450R) * VSPR
	PRP1 6-0 = 0001010	((274R - 20R) / 450R) * VSPR
	PRP1 6-0 = 0001011	((274R - 22R) / 450R) * VSPR
	PRP1 6-0 = 0001100	((274R - 24R) / 450R) * VSPR
	PRP1 6-0 = 0001101	((274R - 26R) / 450R) * VSPR
	PRP1 6-0 = 0001110	((274R - 28R) / 450R) * VSPR
	PRP1 6-0 = 0001111	((274R - 30R) / 450R) * VSPR
	PRP1 6-0 = 0010000	((274R - 32R) / 450R) * VSPR
	PRP1 6-0 = 0010001	((274R - 34R) / 450R) * VSPR
	PRP1 6-0 = 0010010	((274R - 36R) / 450R) * VSPR
	PRP1 6-0 = 0010011	((274R - 38R) / 450R) * VSPR
	PRP1 6-0 = 0010100	((274R - 40R) / 450R) * VSPR
	PRP1 6-0 = 0010101	((274R - 42R) / 450R) * VSPR
	PRP1 6-0 = 0010110	((274R - 44R) / 450R) * VSPR
	PRP1 6-0 = 0010111	((274R - 46R) / 450R) * VSPR
	PRP1 6-0 = 0011000	((274R - 48R) / 450R) * VSPR
	PRP1 6-0 = 0011001	((274R - 50R) / 450R) * VSPR
	PRP1 6-0 = 0011010	((274R - 52R) / 450R) * VSPR
	PRP1 6-0 = 0011011	((274R - 54R) / 450R) * VSPR
	PRP1 6-0 = 0011100	((274R - 56R) / 450R) * VSPR
	PRP1 6-0 = 0011101	((274R - 58R) / 450R) * VSPR
	PRP1 6-0 = 0011110	((274R - 60R) / 450R) * VSPR
	PRP1 6-0 = 0011111	((274R - 62R) / 450R) * VSPR
	PRP1 6-0 = 0100000	((274R - 64R) / 450R) * VSPR
	PRP1 6-0 = 0100001	((274R - 66R) / 450R) * VSPR
	PRP1 6-0 = 0100010	((274R - 68R) / 450R) * VSPR
	PRP1 6-0 = 0100011	((274R - 70R) / 450R) * VSPR
	PRP1 6-0 = 0100100	((274R - 72R) / 450R) * VSPR
	PRP1 6-0 = 0100101	((274R - 74R) / 450R) * VSPR
	PRP1 6-0 = 0100110	((274R - 76R) / 450R) * VSPR
	PRP1 6-0 = 0100111	((274R - 78R) / 450R) * VSPR
	PRP1 6-0 = 0101000	((274R - 80R) / 450R) * VSPR
	PRP1 6-0 = 0101001	((274R - 82R) / 450R) * VSPR
	PRP1 6-0 = 0101010	((274R - 84R) / 450R) * VSPR
	PRP1 6-0 = 0101011	((274R - 86R) / 450R) * VSPR
	PRP1 6-0 = 0101100	((274R - 88R) / 450R) * VSPR
	PRP1 6-0 = 0101101	((274R - 90R) / 450R) * VSPR
	PRP1 6-0 = 0101110	((274R - 92R) / 450R) * VSPR
	PRP1 6-0 = 0101111	((274R - 94R) / 450R) * VSPR
	PRP1 6-0 = 0110000	((274R - 96R) / 450R) * VSPR
	PRP1 6-0 = 0110001	((274R - 98R) / 450R) * VSPR
	PRP1 6-0 = 0110010	((274R - 100R) / 450R) * VSPR
	PRP1 6-0 = 0110011	((274R - 102R) / 450R) * VSPR
	PRP1 6-0 = 0110100	((274R - 104R) / 450R) * VSPR
	PRP1 6-0 = 0110101	((274R - 106R) / 450R) * VSPR
	PRP1 6-0 = 0110110	((274R - 108R) / 450R) * VSPR
	PRP1 6-0 = 0110111	((274R - 110R) / 450R) * VSPR
	PRP1 6-0 = 0111000	((274R - 112R) / 450R) * VSPR
	PRP1 6-0 = 0111001	((274R - 114R) / 450R) * VSPR
	PRP1 6-0 = 0111010	((274R - 116R) / 450R) * VSPR
	PRP1 6-0 = 0111011	((274R - 118R) / 450R) * VSPR
	PRP1 6-0 = 0111100	((274R - 120R) / 450R) * VSPR
	PRP1 6-0 = 0111101	((274R - 122R) / 450R) * VSPR
	PRP1 6-0 = 0111110	((274R - 124R) / 450R) * VSPR
	PRP1 6-0 = 0111111	((274R - 126R) / 450R) * VSPR
	PRP1 6-0 = 1000000	((274R - 128R) / 450R) * VSPR
	PRP1 6-0 = 1000001	((274R - 130R) / 450R) * VSPR
	PRP1 6-0 = 1000010	((274R - 132R) / 450R) * VSPR
	PRP1 6-0 = 1000011	((274R - 134R) / 450R) * VSPR
	PRP1 6-0 = 1000100	((274R - 136R) / 450R) * VSPR

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Reference voltage	Macro adjustment value	VinP13 formula
	PRP1 6-0 = 1000101	$((274R - 138R) / 450R) * VSPR$
	PRP1 6-0 = 1000110	$((274R - 140R) / 450R) * VSPR$
	PRP1 6-0 = 1000111	$((274R - 142R) / 450R) * VSPR$
	PRP1 6-0 = 1001000	$((274R - 144R) / 450R) * VSPR$
	PRP1 6-0 = 1001001	$((274R - 146R) / 450R) * VSPR$
	PRP1 6-0 = 1001010	$((274R - 148R) / 450R) * VSPR$
	PRP1 6-0 = 1001011	$((274R - 150R) / 450R) * VSPR$
	PRP1 6-0 = 1001100	$((274R - 152R) / 450R) * VSPR$
	PRP1 6-0 = 1001101	$((274R - 154R) / 450R) * VSPR$
	PRP1 6-0 = 1001110	$((274R - 156R) / 450R) * VSPR$
	PRP1 6-0 = 1001111	$((274R - 158R) / 450R) * VSPR$
	PRP1 6-0 = 1010000	$((274R - 160R) / 450R) * VSPR$
	PRP1 6-0 = 1010001	$((274R - 162R) / 450R) * VSPR$
	PRP1 6-0 = 1010010	$((274R - 164R) / 450R) * VSPR$
	PRP1 6-0 = 1010011	$((274R - 166R) / 450R) * VSPR$
	PRP1 6-0 = 1010100	$((274R - 168R) / 450R) * VSPR$
	PRP1 6-0 = 1010101	$((274R - 170R) / 450R) * VSPR$
	PRP1 6-0 = 1010110	$((274R - 172R) / 450R) * VSPR$
	PRP1 6-0 = 1010111	$((274R - 174R) / 450R) * VSPR$
	PRP1 6-0 = 1011000	inhibit
	PRP1 6-0 = 1011001	inhibit
	PRP1 6-0 = 1011010	inhibit
	PRP1 6-0 = 1011011	inhibit
	PRP1 6-0 = 1011100	inhibit
	PRP1 6-0 = 1011101	inhibit
	PRP1 6-0 = 1011110	inhibit
	PRP1 6-0 = 1011111	inhibit
	PRP1 6-0 = 1100000	inhibit
	PRP1 6-0 = 1100001	inhibit
	PRP1 6-0 = 1100010	inhibit
	PRP1 6-0 = 1100011	inhibit
	PRP1 6-0 = 1100100	inhibit
	PRP1 6-0 = 1100101	inhibit
	PRP1 6-0 = 1100110	inhibit
	PRP1 6-0 = 1100111	inhibit
	PRP1 6-0 = 1101000	inhibit
	PRP1 6-0 = 1101001	inhibit
	PRP1 6-0 = 1101010	inhibit
	PRP1 6-0 = 1101011	inhibit
	PRP1 6-0 = 1101100	inhibit
	PRP1 6-0 = 1101101	inhibit
	PRP1 6-0 = 1101110	inhibit
	PRP1 6-0 = 1101111	inhibit
	PRP1 6-0 = 1110000	inhibit
	PRP1 6-0 = 1110001	inhibit
	PRP1 6-0 = 1110010	inhibit
	PRP1 6-0 = 1110011	inhibit
	PRP1 6-0 = 1110100	inhibit
	PRP1 6-0 = 1110101	inhibit
	PRP1 6-0 = 1110110	inhibit
	PRP1 6-0 = 1110111	inhibit
	PRP1 6-0 = 1111000	inhibit
	PRP1 6-0 = 1111001	inhibit
	PRP1 6-0 = 1111010	inhibit
	PRP1 6-0 = 1111011	inhibit
	PRP1 6-0 = 1111100	inhibit
	PRP1 6-0 = 1111101	inhibit
	PRP1 6-0 = 1111110	inhibit
	PRP1 6-0 = 1111111	inhibit

Table 5.13: VinP13

Reference voltage	Macro adjustment value	VinP3 formula
VinP3	PKP0 4-0 = 00000	$(47R / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 00001	$((47R - 1R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 00010	$((47R - 2R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 00011	$((47R - 3R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 00100	$((47R - 4R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 00101	$((47R - 5R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 00110	$((47R - 6R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 00111	$((47R - 7R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 01000	$((47R - 8R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 01001	$((47R - 9R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 01010	$((47R - 10R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 01011	$((47R - 11R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 01100	$((47R - 12R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 01101	$((47R - 13R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 01110	$((47R - 14R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 01111	$((47R - 15R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 10000	$((47R - 16R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 10001	$((47R - 17R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 10010	$((47R - 18R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 10011	$((47R - 19R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 10100	$((47R - 20R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 10101	$((47R - 21R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 10110	$((47R - 22R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 10111	$((47R - 23R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 11000	$((47R - 24R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 11001	$((47R - 25R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 11010	$((47R - 26R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 11011	$((47R - 27R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 11100	$((47R - 28R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 11101	$((47R - 29R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 11110	$((47R - 30R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP0 4-0 = 11111	$((47R - 31R) / 48R) * (VinP2 - VinP7) + VinP7$

Table 5.14: VinP3

Reference voltage	Macro adjustment value	VinP4 formula
VinP4	PKP1 4-0 = 00000	$(39R / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 00001	$((39R - 1R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 00010	$((39R - 2R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 00011	$((39R - 3R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 00100	$((39R - 4R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 00101	$((39R - 5R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 00110	$((39R - 6R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 00111	$((39R - 7R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 01000	$((39R - 8R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 01001	$((39R - 9R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 01010	$((39R - 10R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 01011	$((39R - 11R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 01100	$((39R - 12R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 01101	$((39R - 13R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 01110	$((39R - 14R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 01111	$((39R - 15R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 10000	$((39R - 16R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 10001	$((39R - 17R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 10010	$((39R - 18R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 10011	$((39R - 19R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 10100	$((39R - 20R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 10101	$((39R - 21R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 10110	$((39R - 22R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 10111	$((39R - 23R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 11000	$((39R - 24R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 11001	$((39R - 25R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 11010	$((39R - 26R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 11011	$((39R - 27R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 11100	$((39R - 28R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 11101	$((39R - 29R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 11110	$((39R - 30R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP1 4-0 = 11111	$((39R - 31R) / 48R) * (VinP2 - VinP7) + VinP7$

Table 5.15: VinP4

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Reference voltage	Macro adjustment value	VinP5 formula
VinP5	PKP2 4-0 = 00000	$(32R / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 00001	$((32R - 1R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 00010	$((32R - 2R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 00011	$((32R - 3R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 00100	$((32R - 4R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 00101	$((32R - 5R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 00110	$((32R - 6R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 00111	$((32R - 7R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 01000	$((32R - 8R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 01001	$((32R - 9R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 01010	$((32R - 10R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 01011	$((32R - 11R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 01100	$((32R - 12R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 01101	$((32R - 13R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 01110	$((32R - 14R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 01111	$((32R - 15R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 10000	$((32R - 16R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 10001	$((32R - 17R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 10010	$((32R - 18R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 10011	$((32R - 19R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 10100	$((32R - 20R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 10101	$((32R - 21R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 10110	$((32R - 22R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 10111	$((32R - 23R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 11000	$((32R - 24R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 11001	$((32R - 25R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 11010	$((32R - 26R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 11011	$((32R - 27R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 11100	$((32R - 28R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 11101	$((32R - 29R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 11110	$((32R - 30R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP2 4-0 = 11111	$((32R - 31R) / 48R) * (VinP2 - VinP7) + VinP7$

Table 5.16: VinP5

Reference voltage	Macro adjustment value	VinP6 formula
VinP6	PKP3 4-0 = 00000	$(32R / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 00001	$((32R - 1R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 00010	$((32R - 2R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 00011	$((32R - 3R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 00100	$((32R - 4R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 00101	$((32R - 5R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 00110	$((32R - 6R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 00111	$((32R - 7R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 01000	$((32R - 8R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 01001	$((32R - 9R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 01010	$((32R - 10R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 01011	$((32R - 11R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 01100	$((32R - 12R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 01101	$((32R - 13R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 01110	$((32R - 14R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 01111	$((32R - 15R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 10000	$((32R - 16R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 10001	$((32R - 17R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 10010	$((32R - 18R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 10011	$((32R - 19R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 10100	$((32R - 20R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 10101	$((32R - 21R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 10110	$((32R - 22R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 10111	$((32R - 23R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 11000	$((32R - 24R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 11001	$((32R - 25R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 11010	$((32R - 26R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 11011	$((32R - 27R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 11100	$((32R - 28R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 11101	$((32R - 29R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 11110	$((32R - 30R) / 48R) * (VinP2 - VinP7) + VinP7$
	PKP3 4-0 = 11111	$((32R - 31R) / 48R) * (VinP2 - VinP7) + VinP7$

Table 5.17: VinP6

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Reference voltage	Macro adjustment value	VinP8 formula
VinP8	PKP4 4-0 = 00000	$(220R / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 00001	$((220R - 3R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 00010	$((220R - 6R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 00011	$((220R - 9R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 00100	$((220R - 12R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 00101	$((220R - 15R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 00110	$((220R - 18R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 00111	$((220R - 21R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 01000	$((220R - 24R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 01001	$((220R - 27R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 01010	$((220R - 30R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 01011	$((220R - 33R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 01100	$((220R - 36R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 01101	$((220R - 39R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 01110	$((220R - 42R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 01111	$((220R - 45R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 10000	$((220R - 48R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 10001	$((220R - 51R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 10010	$((220R - 54R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 10011	$((220R - 57R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 10100	$((220R - 60R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 10101	$((220R - 63R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 10110	$((220R - 66R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 10111	$((220R - 69R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 11000	$((220R - 72R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 11001	$((220R - 75R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 11010	$((220R - 78R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 11011	$((220R - 81R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 11100	$((220R - 84R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 11101	$((220R - 87R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 11110	$((220R - 90R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP4 4-0 = 11111	$((220R - 93R) / 223R) * (VinP7 - VinP13) + VinP13$

Table 5.18: VinP8

Reference voltage	Macro adjustment value	VinP9 formula
VinP9	PKP5 4-0 = 00000	$(193R / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 00001	$((193R - 3R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 00010	$((193R - 6R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 00011	$((193R - 9R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 00100	$((193R - 12R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 00101	$((193R - 15R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 00110	$((193R - 18R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 00111	$((193R - 21R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 01000	$((193R - 24R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 01001	$((193R - 27R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 01010	$((193R - 30R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 01011	$((193R - 33R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 01100	$((193R - 36R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 01101	$((193R - 39R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 01110	$((193R - 42R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 01111	$((193R - 45R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 10000	$((193R - 48R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 10001	$((193R - 51R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 10010	$((193R - 54R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 10011	$((193R - 57R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 10100	$((193R - 60R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 10101	$((193R - 63R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 10110	$((193R - 66R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 10111	$((193R - 69R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 11000	$((193R - 72R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 11001	$((193R - 75R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 11010	$((193R - 78R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 11011	$((193R - 81R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 11100	$((193R - 84R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 11101	$((193R - 87R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 11110	$((193R - 90R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP5 4-0 = 11111	$((193R - 93R) / 223R) * (VinP7 - VinP13) + VinP13$

Table 5.19: VinP9

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Reference voltage	Macro adjustment value	VinP10 formula
VinP10	PKP6 4-0 = 00000	$(158R / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 00001	$((158R - 3R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 00010	$((158R - 6R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 00011	$((158R - 9R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 00100	$((158R - 12R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 00101	$((158R - 15R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 00110	$((158R - 18R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 00111	$((158R - 21R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 01000	$((158R - 24R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 01001	$((158R - 27R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 01010	$((158R - 30R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 01011	$((158R - 33R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 01100	$((158R - 36R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 01101	$((158R - 39R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 01110	$((158R - 42R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 01111	$((158R - 45R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 10000	$((158R - 48R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 10001	$((158R - 51R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 10010	$((158R - 54R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 10011	$((158R - 57R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 10100	$((158R - 60R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 10101	$((158R - 63R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 10110	$((158R - 66R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 10111	$((158R - 69R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 11000	$((158R - 72R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 11001	$((158R - 75R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 11010	$((158R - 78R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 11011	$((158R - 81R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 11100	$((158R - 84R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 11101	$((158R - 87R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 11110	$((158R - 90R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP6 4-0 = 11111	$((158R - 93R) / 223R) * (VinP7 - VinP13) + VinP13$

Table 5.20: VinP10

Reference voltage	Macro adjustment value	VinP11 formula
VinP11	PKP7 4-0 = 00000	$(123R / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 00001	$((123R - 3R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 00010	$((123R - 6R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 00011	$((123R - 9R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 00100	$((123R - 12R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 00101	$((123R - 15R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 00110	$((123R - 18R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 00111	$((123R - 21R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 01000	$((123R - 24R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 01001	$((123R - 27R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 01010	$((123R - 30R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 01011	$((123R - 33R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 01100	$((123R - 36R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 01101	$((123R - 39R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 01110	$((123R - 42R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 01111	$((123R - 45R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 10000	$((123R - 48R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 10001	$((123R - 51R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 10010	$((123R - 54R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 10011	$((123R - 57R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 10100	$((123R - 60R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 10101	$((123R - 63R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 10110	$((123R - 66R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 10111	$((123R - 69R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 11000	$((123R - 72R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 11001	$((123R - 75R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 11010	$((123R - 78R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 11011	$((123R - 81R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 11100	$((123R - 84R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 11101	$((123R - 87R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 11110	$((123R - 90R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP7 4-0 = 11111	$((123R - 93R) / 223R) * (VinP7 - VinP13) + VinP13$

Table 5.21: VinP11

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Reference voltage	Macro adjustment value	VinP12 formula
VinP12	PKP8 4-0 = 00000	$(96R / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 00001	$((96R - 3R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 00010	$((96R - 6R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 00011	$((96R - 9R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 00100	$((96R - 12R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 00101	$((96R - 15R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 00110	$((96R - 18R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 00111	$((96R - 21R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 01000	$((96R - 24R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 01001	$((96R - 27R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 01010	$((96R - 30R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 01011	$((96R - 33R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 01100	$((96R - 36R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 01101	$((96R - 39R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 01110	$((96R - 42R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 01111	$((96R - 45R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 10000	$((96R - 48R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 10001	$((96R - 51R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 10010	$((96R - 54R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 10011	$((96R - 57R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 10100	$((96R - 60R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 10101	$((96R - 63R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 10110	$((96R - 66R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 10111	$((96R - 69R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 11000	$((96R - 72R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 11001	$((96R - 75R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 11010	$((96R - 78R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 11011	$((96R - 81R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 11100	$((96R - 84R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 11101	$((96R - 87R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 11110	$((96R - 90R) / 223R) * (VinP7 - VinP13) + VinP13$
	PKP8 4-0 = 11111	$((96R - 93R) / 223R) * (VinP7 - VinP13) + VinP13$

Table 5.22: VinP12

Reference voltage	Macro adjustment value	VinP14 formula
VinP14	PKP9 4-0 = 00000	$(47R / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 00001	$((47R - 1R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 00010	$((47R - 2R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 00011	$((47R - 3R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 00100	$((47R - 4R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 00101	$((47R - 5R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 00110	$((47R - 6R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 00111	$((47R - 7R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 01000	$((47R - 8R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 01001	$((47R - 9R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 01010	$((47R - 10R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 01011	$((47R - 11R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 01100	$((47R - 12R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 01101	$((47R - 13R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 01110	$((47R - 14R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 01111	$((47R - 15R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 10000	$((47R - 16R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 10001	$((47R - 17R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 10010	$((47R - 18R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 10011	$((47R - 19R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 10100	$((47R - 20R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 10101	$((47R - 21R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 10110	$((47R - 22R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 10111	$((47R - 23R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 11000	$((47R - 24R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 11001	$((47R - 25R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 11010	$((47R - 26R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 11011	$((47R - 27R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 11100	$((47R - 28R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 11101	$((47R - 29R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 11110	$((47R - 30R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP9 4-0 = 11111	$((47R - 31R) / 48R) * (VinP13 - VinP18) + VinP18$

Table 5.23: VinP14

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Reference voltage	Macro adjustment value	VinP15 formula
VinP15	PKP10 4-0 = 00000	$(47R / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 00001	$((47R - 1R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 00010	$((47R - 2R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 00011	$((47R - 3R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 00100	$((47R - 4R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 00101	$((47R - 5R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 00110	$((47R - 6R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 00111	$((47R - 7R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 01000	$((47R - 8R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 01001	$((47R - 9R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 01010	$((47R - 10R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 01011	$((47R - 11R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 01100	$((47R - 12R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 01101	$((47R - 13R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 01110	$((47R - 14R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 01111	$((47R - 15R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 10000	$((47R - 16R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 10001	$((47R - 17R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 10010	$((47R - 18R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 10011	$((47R - 19R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 10100	$((47R - 20R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 10101	$((47R - 21R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 10110	$((47R - 22R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 10111	$((47R - 23R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 11000	$((47R - 24R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 11001	$((47R - 25R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 11010	$((47R - 26R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 11011	$((47R - 27R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 11100	$((47R - 28R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 11101	$((47R - 29R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 11110	$((47R - 30R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP10 4-0 = 11111	$((47R - 31R) / 48R) * (VinP13 - VinP18) + VinP18$

Table 5.24: VinP15

Reference voltage	Macro adjustment value	VinP16 formula
VinP16	PKP11 4-0 = 00000	$(39R / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 00001	$((39R - 1R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 00010	$((39R - 2R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 00011	$((39R - 3R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 00100	$((39R - 4R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 00101	$((39R - 5R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 00110	$((39R - 6R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 00111	$((39R - 7R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 01000	$((39R - 8R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 01001	$((39R - 9R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 01010	$((39R - 10R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 01011	$((39R - 11R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 01100	$((39R - 12R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 01101	$((39R - 13R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 01110	$((39R - 14R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 01111	$((39R - 15R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 10000	$((39R - 16R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 10001	$((39R - 17R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 10010	$((39R - 18R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 10011	$((39R - 19R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 10100	$((39R - 20R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 10101	$((39R - 21R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 10110	$((39R - 22R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 10111	$((39R - 23R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 11000	$((39R - 24R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 11001	$((39R - 25R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 11010	$((39R - 26R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 11011	$((39R - 27R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 11100	$((39R - 28R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 11101	$((39R - 29R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 11110	$((39R - 30R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP11 4-0 = 11111	$((39R - 31R) / 48R) * (VinP13 - VinP18) + VinP18$

Table 5.25: VinP16

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Reference voltage	Macro adjustment value	VinP13 formula
VinP17	PKP12 4-0 = 00000	$(32R / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 00001	$((32R - 1R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 00010	$((32R - 2R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 00011	$((32R - 3R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 00100	$((32R - 4R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 00101	$((32R - 5R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 00110	$((32R - 6R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 00111	$((32R - 7R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 01000	$((32R - 8R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 01001	$((32R - 9R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 01010	$((32R - 10R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 01011	$((32R - 11R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 01100	$((32R - 12R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 01101	$((32R - 13R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 01110	$((32R - 14R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 01111	$((32R - 15R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 10000	$((32R - 16R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 10001	$((32R - 17R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 10010	$((32R - 18R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 10011	$((32R - 19R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 10100	$((32R - 20R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 10101	$((32R - 21R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 10110	$((32R - 22R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 10111	$((32R - 23R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 11000	$((32R - 24R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 11001	$((32R - 25R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 11010	$((32R - 26R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 11011	$((32R - 27R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 11100	$((32R - 28R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 11101	$((32R - 29R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 11110	$((32R - 30R) / 48R) * (VinP13 - VinP18) + VinP18$
	PKP12 4-0 = 11111	$((32R - 31R) / 48R) * (VinP13 - VinP18) + VinP18$

Table 5.26: VinP17

Reference voltage	Macro adjustment value	VinP0 formula
VinN0	VRN0 5-0 = 000000	VSPR
	VRN0 5-0 = 000001	((450R - 20R) / 450R) * VSPR
	VRN0 5-0 = 000010	((450R - 22R) / 450R) * VSPR
	VRN0 5-0 = 000011	((450R - 24R) / 450R) * VSPR
	VRN0 5-0 = 000100	((450R - 26R) / 450R) * VSPR
	VRN0 5-0 = 000101	((450R - 28R) / 450R) * VSPR
	VRN0 5-0 = 000110	((450R - 30R) / 450R) * VSPR
	VRN0 5-0 = 000111	((450R - 32R) / 450R) * VSPR
	VRN0 5-0 = 001000	((450R - 34R) / 450R) * VSPR
	VRN0 5-0 = 001001	((450R - 36R) / 450R) * VSPR
	VRN0 5-0 = 001010	((450R - 38R) / 450R) * VSPR
	VRN0 5-0 = 001011	((450R - 40R) / 450R) * VSPR
	VRN0 5-0 = 001100	((450R - 42R) / 450R) * VSPR
	VRN0 5-0 = 001101	((450R - 44R) / 450R) * VSPR
	VRN0 5-0 = 001110	((450R - 46R) / 450R) * VSPR
	VRN0 5-0 = 001111	((450R - 48R) / 450R) * VSPR
	VRN0 5-0 = 010000	((450R - 50R) / 450R) * VSPR
	VRN0 5-0 = 010001	((450R - 52R) / 450R) * VSPR
	VRN0 5-0 = 010010	((450R - 54R) / 450R) * VSPR
	VRN0 5-0 = 010011	((450R - 56R) / 450R) * VSPR
	VRN0 5-0 = 010100	((450R - 58R) / 450R) * VSPR
	VRN0 5-0 = 010101	((450R - 60R) / 450R) * VSPR
	VRN0 5-0 = 010110	((450R - 62R) / 450R) * VSPR
	VRN0 5-0 = 010111	((450R - 64R) / 450R) * VSPR
	VRN0 5-0 = 011000	((450R - 66R) / 450R) * VSPR
	VRN0 5-0 = 011001	((450R - 68R) / 450R) * VSPR
	VRN0 5-0 = 011010	((450R - 70R) / 450R) * VSPR
	VRN0 5-0 = 011011	((450R - 72R) / 450R) * VSPR
	VRN0 5-0 = 011100	((450R - 74R) / 450R) * VSPR
	VRN0 5-0 = 011101	((450R - 76R) / 450R) * VSPR
	VRN0 5-0 = 011110	((450R - 78R) / 450R) * VSPR
	VRN0 5-0 = 011111	((450R - 80R) / 450R) * VSPR
	VRN0 5-0 = 100000	((450R - 82R) / 450R) * VSPR
	VRN0 5-0 = 100001	((450R - 84R) / 450R) * VSPR
	VRN0 5-0 = 100010	((450R - 86R) / 450R) * VSPR
	VRN0 5-0 = 100011	((450R - 88R) / 450R) * VSPR
	VRN0 5-0 = 100100	((450R - 90R) / 450R) * VSPR
	VRN0 5-0 = 100101	((450R - 92R) / 450R) * VSPR
	VRN0 5-0 = 100110	((450R - 94R) / 450R) * VSPR
	VRN0 5-0 = 100111	((450R - 96R) / 450R) * VSPR
	VRN0 5-0 = 101000	((450R - 98R) / 450R) * VSPR
	VRN0 5-0 = 101001	((450R - 100R) / 450R) * VSPR
	VRN0 5-0 = 101010	((450R - 102R) / 450R) * VSPR
	VRN0 5-0 = 101011	((450R - 104R) / 450R) * VSPR
	VRN0 5-0 = 101100	((450R - 106R) / 450R) * VSPR
	VRN0 5-0 = 101101	((450R - 108R) / 450R) * VSPR
	VRN0 5-0 = 101110	((450R - 110R) / 450R) * VSPR
	VRN0 5-0 = 101111	((450R - 112R) / 450R) * VSPR
	VRN0 5-0 = 110000	((450R - 114R) / 450R) * VSPR
	VRN0 5-0 = 110001	((450R - 116R) / 450R) * VSPR
	VRN0 5-0 = 110010	((450R - 118R) / 450R) * VSPR
	VRN0 5-0 = 110011	((450R - 120R) / 450R) * VSPR
	VRN0 5-0 = 110100	((450R - 122R) / 450R) * VSPR
	VRN0 5-0 = 110101	((450R - 124R) / 450R) * VSPR
	VRN0 5-0 = 110110	((450R - 126R) / 450R) * VSPR
	VRN0 5-0 = 110111	((450R - 128R) / 450R) * VSPR
	VRN0 5-0 = 111000	((450R - 130R) / 450R) * VSPR
	VRN0 5-0 = 111001	((450R - 132R) / 450R) * VSPR
	VRN0 5-0 = 111010	((450R - 134R) / 450R) * VSPR
	VRN0 5-0 = 111011	((450R - 136R) / 450R) * VSPR
	VRN0 5-0 = 111100	((450R - 138R) / 450R) * VSPR
	VRN0 5-0 = 111101	((450R - 140R) / 450R) * VSPR
	VRN0 5-0 = 111110	((450R - 142R) / 450R) * VSPR
	VRN0 5-0 = 111111	((450R - 144R) / 450R) * VSPR

Table 5.27: VinN0

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Reference voltage	Macro adjustment value	VinN1 formula
VinN1	VRN1 5-0 = 000000	((430R / 450R) * VSPR
	VRN1 5-0 = 000001	((430R - 2R ) / 450R) * VSPR
	VRN1 5-0 = 000010	((430R - 4R ) / 450R) * VSPR
	VRN1 5-0 = 000011	((430R - 6R ) / 450R) * VSPR
	VRN1 5-0 = 000100	((430R - 8R ) / 450R) * VSPR
	VRN1 5-0 = 000101	((430R - 10R ) / 450R) * VSPR
	VRN1 5-0 = 000110	((430R - 12R ) / 450R) * VSPR
	VRN1 5-0 = 000111	((430R - 14R ) / 450R) * VSPR
	VRN1 5-0 = 001000	((430R - 16R ) / 450R) * VSPR
	VRN1 5-0 = 001001	((430R - 18R ) / 450R) * VSPR
	VRN1 5-0 = 001010	((430R - 20R ) / 450R) * VSPR
	VRN1 5-0 = 001011	((430R - 22R ) / 450R) * VSPR
	VRN1 5-0 = 001100	((430R - 24R ) / 450R) * VSPR
	VRN1 5-0 = 001101	((430R - 26R ) / 450R) * VSPR
	VRN1 5-0 = 001110	((430R - 28R ) / 450R) * VSPR
	VRN1 5-0 = 001111	((430R - 30R ) / 450R) * VSPR
	VRN1 5-0 = 010000	((430R - 32R ) / 450R) * VSPR
	VRN1 5-0 = 010001	((430R - 34R ) / 450R) * VSPR
	VRN1 5-0 = 010010	((430R - 36R ) / 450R) * VSPR
	VRN1 5-0 = 010011	((430R - 38R ) / 450R) * VSPR
	VRN1 5-0 = 010100	((430R - 40R ) / 450R) * VSPR
	VRN1 5-0 = 010101	((430R - 42R ) / 450R) * VSPR
	VRN1 5-0 = 010110	((430R - 44R ) / 450R) * VSPR
	VRN1 5-0 = 010111	((430R - 46R ) / 450R) * VSPR
	VRN1 5-0 = 011000	((430R - 48R ) / 450R) * VSPR
	VRN1 5-0 = 011001	((430R - 50R ) / 450R) * VSPR
	VRN1 5-0 = 011010	((430R - 52R ) / 450R) * VSPR
	VRN1 5-0 = 011011	((430R - 54R ) / 450R) * VSPR
	VRN1 5-0 = 011100	((430R - 56R ) / 450R) * VSPR
	VRN1 5-0 = 011101	((430R - 58R ) / 450R) * VSPR
	VRN1 5-0 = 011110	((430R - 60R ) / 450R) * VSPR
	VRN1 5-0 = 011111	((430R - 62R ) / 450R) * VSPR
	VRN1 5-0 = 100000	((430R - 64R ) / 450R) * VSPR
	VRN1 5-0 = 100001	((430R - 66R ) / 450R) * VSPR
	VRN1 5-0 = 100010	((430R - 68R ) / 450R) * VSPR
	VRN1 5-0 = 100011	((430R - 70R ) / 450R) * VSPR
	VRN1 5-0 = 100100	((430R - 72R ) / 450R) * VSPR
	VRN1 5-0 = 100101	((430R - 74R ) / 450R) * VSPR
	VRN1 5-0 = 100110	((430R - 76R ) / 450R) * VSPR
	VRN1 5-0 = 100111	((430R - 78R ) / 450R) * VSPR
	VRN1 5-0 = 101000	((430R - 80R ) / 450R) * VSPR
	VRN1 5-0 = 101001	((430R - 82R ) / 450R) * VSPR
	VRN1 5-0 = 101010	((430R - 84R ) / 450R) * VSPR
	VRN1 5-0 = 101011	((430R - 86R ) / 450R) * VSPR
	VRN1 5-0 = 101100	((430R - 88R ) / 450R) * VSPR
	VRN1 5-0 = 101101	((430R - 90R ) / 450R) * VSPR
	VRN1 5-0 = 101110	((430R - 92R ) / 450R) * VSPR
	VRN1 5-0 = 101111	((430R - 94R ) / 450R) * VSPR
	VRN1 5-0 = 110000	((430R - 96R ) / 450R) * VSPR
	VRN1 5-0 = 110001	((430R - 98R ) / 450R) * VSPR
	VRN1 5-0 = 110010	((430R - 100R ) / 450R) * VSPR
	VRN1 5-0 = 110011	((430R - 102R ) / 450R) * VSPR
	VRN1 5-0 = 110100	((430R - 104R ) / 450R) * VSPR
	VRN1 5-0 = 110101	((430R - 106R ) / 450R) * VSPR
	VRN1 5-0 = 110110	((430R - 108R ) / 450R) * VSPR
	VRN1 5-0 = 110111	((430R - 110R ) / 450R) * VSPR
	VRN1 5-0 = 111000	((430R - 112R ) / 450R) * VSPR
	VRN1 5-0 = 111001	((430R - 114R ) / 450R) * VSPR
	VRN1 5-0 = 111010	((430R - 116R ) / 450R) * VSPR
	VRN1 5-0 = 111011	((430R - 118R ) / 450R) * VSPR
	VRN1 5-0 = 111100	((430R - 120R ) / 450R) * VSPR
	VRN1 5-0 = 111101	((430R - 122R ) / 450R) * VSPR
	VRN1 5-0 = 111110	((430R - 124R ) / 450R) * VSPR
	VRN1 5-0 = 111111	((430R - 126R ) / 450R) * VSPR

Table 5.28: VinN1

Reference voltage	Macro adjustment value	VinN2 formula
VinN2	VRN2 5-0 = 000000	((420R / 450R) * VSPR
	VRN2 5-0 = 000001	((420R - 2R ) / 450R) * VSPR
	VRN2 5-0 = 000010	((420R - 4R ) / 450R) * VSPR
	VRN2 5-0 = 000011	((420R - 6R ) / 450R) * VSPR
	VRN2 5-0 = 000100	((420R - 8R ) / 450R) * VSPR
	VRN2 5-0 = 000101	((420R - 10R ) / 450R) * VSPR
	VRN2 5-0 = 000110	((420R - 12R ) / 450R) * VSPR
	VRN2 5-0 = 000111	((420R - 14R ) / 450R) * VSPR
	VRN2 5-0 = 001000	((420R - 16R ) / 450R) * VSPR
	VRN2 5-0 = 001001	((420R - 18R ) / 450R) * VSPR
	VRN2 5-0 = 001010	((420R - 20R ) / 450R) * VSPR
	VRN2 5-0 = 001011	((420R - 22R ) / 450R) * VSPR
	VRN2 5-0 = 001100	((420R - 24R ) / 450R) * VSPR
	VRN2 5-0 = 001101	((420R - 26R ) / 450R) * VSPR
	VRN2 5-0 = 001110	((420R - 28R ) / 450R) * VSPR
	VRN2 5-0 = 001111	((420R - 30R ) / 450R) * VSPR
	VRN2 5-0 = 010000	((420R - 32R ) / 450R) * VSPR
	VRN2 5-0 = 010001	((420R - 34R ) / 450R) * VSPR
	VRN2 5-0 = 010010	((420R - 36R ) / 450R) * VSPR
	VRN2 5-0 = 010011	((420R - 38R ) / 450R) * VSPR
	VRN2 5-0 = 010100	((420R - 40R ) / 450R) * VSPR
	VRN2 5-0 = 010101	((420R - 42R ) / 450R) * VSPR
	VRN2 5-0 = 010110	((420R - 44R ) / 450R) * VSPR
	VRN2 5-0 = 010111	((420R - 46R ) / 450R) * VSPR
	VRN2 5-0 = 011000	((420R - 48R ) / 450R) * VSPR
	VRN2 5-0 = 011001	((420R - 50R ) / 450R) * VSPR
	VRN2 5-0 = 011010	((420R - 52R ) / 450R) * VSPR
	VRN2 5-0 = 011011	((420R - 54R ) / 450R) * VSPR
	VRN2 5-0 = 011100	((420R - 56R ) / 450R) * VSPR
	VRN2 5-0 = 011101	((420R - 58R ) / 450R) * VSPR
	VRN2 5-0 = 011110	((420R - 60R ) / 450R) * VSPR
	VRN2 5-0 = 011111	((420R - 62R ) / 450R) * VSPR
	VRN2 5-0 = 100000	((420R - 64R ) / 450R) * VSPR
	VRN2 5-0 = 100001	((420R - 66R ) / 450R) * VSPR
	VRN2 5-0 = 100010	((420R - 68R ) / 450R) * VSPR
	VRN2 5-0 = 100011	((420R - 70R ) / 450R) * VSPR
	VRN2 5-0 = 100100	((420R - 72R ) / 450R) * VSPR
	VRN2 5-0 = 100101	((420R - 74R ) / 450R) * VSPR
	VRN2 5-0 = 100110	((420R - 76R ) / 450R) * VSPR
	VRN2 5-0 = 100111	((420R - 78R ) / 450R) * VSPR
	VRN2 5-0 = 101000	((420R - 80R ) / 450R) * VSPR
	VRN2 5-0 = 101001	((420R - 82R ) / 450R) * VSPR
	VRN2 5-0 = 101010	((420R - 84R ) / 450R) * VSPR
	VRN2 5-0 = 101011	((420R - 86R ) / 450R) * VSPR
	VRN2 5-0 = 101100	((420R - 88R ) / 450R) * VSPR
	VRN2 5-0 = 101101	((420R - 90R ) / 450R) * VSPR
	VRN2 5-0 = 101110	((420R - 92R ) / 450R) * VSPR
	VRN2 5-0 = 101111	((420R - 94R ) / 450R) * VSPR
	VRN2 5-0 = 110000	((420R - 96R ) / 450R) * VSPR
	VRN2 5-0 = 110001	((420R - 98R ) / 450R) * VSPR
	VRN2 5-0 = 110010	((420R - 100R ) / 450R) * VSPR
	VRN2 5-0 = 110011	((420R - 102R ) / 450R) * VSPR
	VRN2 5-0 = 110100	((420R - 104R ) / 450R) * VSPR
	VRN2 5-0 = 110101	((420R - 106R ) / 450R) * VSPR
	VRN2 5-0 = 110110	((420R - 108R ) / 450R) * VSPR
	VRN2 5-0 = 110111	((420R - 110R ) / 450R) * VSPR
	VRN2 5-0 = 111000	((420R - 112R ) / 450R) * VSPR
	VRN2 5-0 = 111001	((420R - 114R ) / 450R) * VSPR
	VRN2 5-0 = 111010	((420R - 116R ) / 450R) * VSPR
	VRN2 5-0 = 111011	((420R - 118R ) / 450R) * VSPR
	VRN2 5-0 = 111100	((420R - 120R ) / 450R) * VSPR
	VRN2 5-0 = 111101	((420R - 122R ) / 450R) * VSPR
	VRN2 5-0 = 111110	((420R - 124R ) / 450R) * VSPR
	VRN2 5-0 = 111111	((420R - 126R ) / 450R) * VSPR

Table 5.29: VinN2

Reference voltage	Macro adjustment value	VinN18 formula
VinN18	VRN3 5-0 = 000000	(156R / 450R) * VSPR
	VRN3 5-0 = 000001	((156R - 2R ) / 450R) * VSPR
	VRN3 5-0 = 000010	((156R - 4R ) / 450R) * VSPR
	VRN3 5-0 = 000011	((156R - 6R ) / 450R) * VSPR
	VRN3 5-0 = 000100	((156R - 8R ) / 450R) * VSPR
	VRN3 5-0 = 000101	((156R - 10R ) / 450R) * VSPR
	VRN3 5-0 = 000110	((156R - 12R ) / 450R) * VSPR
	VRN3 5-0 = 000111	((156R - 14R ) / 450R) * VSPR
	VRN3 5-0 = 001000	((156R - 16R ) / 450R) * VSPR
	VRN3 5-0 = 001001	((156R - 18R ) / 450R) * VSPR
	VRN3 5-0 = 001010	((156R - 20R ) / 450R) * VSPR
	VRN3 5-0 = 001011	((156R - 22R ) / 450R) * VSPR
	VRN3 5-0 = 001100	((156R - 24R ) / 450R) * VSPR
	VRN3 5-0 = 001101	((156R - 26R ) / 450R) * VSPR
	VRN3 5-0 = 001110	((156R - 28R ) / 450R) * VSPR
	VRN3 5-0 = 001111	((156R - 30R ) / 450R) * VSPR
	VRN3 5-0 = 010000	((156R - 32R ) / 450R) * VSPR
	VRN3 5-0 = 010001	((156R - 34R ) / 450R) * VSPR
	VRN3 5-0 = 010010	((156R - 36R ) / 450R) * VSPR
	VRN3 5-0 = 010011	((156R - 38R ) / 450R) * VSPR
	VRN3 5-0 = 010100	((156R - 40R ) / 450R) * VSPR
	VRN3 5-0 = 010101	((156R - 42R ) / 450R) * VSPR
	VRN3 5-0 = 010110	((156R - 44R ) / 450R) * VSPR
	VRN3 5-0 = 010111	((156R - 46R ) / 450R) * VSPR
	VRN3 5-0 = 011000	((156R - 48R ) / 450R) * VSPR
	VRN3 5-0 = 011001	((156R - 50R ) / 450R) * VSPR
	VRN3 5-0 = 011010	((156R - 52R ) / 450R) * VSPR
	VRN3 5-0 = 011011	((156R - 54R ) / 450R) * VSPR
	VRN3 5-0 = 011100	((156R - 56R ) / 450R) * VSPR
	VRN3 5-0 = 011101	((156R - 58R ) / 450R) * VSPR
	VRN3 5-0 = 011110	((156R - 60R ) / 450R) * VSPR
	VRN3 5-0 = 011111	((156R - 62R ) / 450R) * VSPR
	VRN3 5-0 = 100000	((156R - 64R ) / 450R) * VSPR
	VRN3 5-0 = 100001	((156R - 66R ) / 450R) * VSPR
	VRN3 5-0 = 100010	((156R - 68R ) / 450R) * VSPR
	VRN3 5-0 = 100011	((156R - 70R ) / 450R) * VSPR
	VRN3 5-0 = 100100	((156R - 72R ) / 450R) * VSPR
	VRN3 5-0 = 100101	((156R - 74R ) / 450R) * VSPR
	VRN3 5-0 = 100110	((156R - 76R ) / 450R) * VSPR
	VRN3 5-0 = 100111	((156R - 78R ) / 450R) * VSPR
	VRN3 5-0 = 101000	((156R - 80R ) / 450R) * VSPR
	VRN3 5-0 = 101001	((156R - 82R ) / 450R) * VSPR
	VRN3 5-0 = 101010	((156R - 84R ) / 450R) * VSPR
	VRN3 5-0 = 101011	((156R - 86R ) / 450R) * VSPR
	VRN3 5-0 = 101100	((156R - 88R ) / 450R) * VSPR
	VRN3 5-0 = 101101	((156R - 90R ) / 450R) * VSPR
	VRN3 5-0 = 101110	((156R - 92R ) / 450R) * VSPR
	VRN3 5-0 = 101111	((156R - 94R ) / 450R) * VSPR
	VRN3 5-0 = 110000	((156R - 96R ) / 450R) * VSPR
	VRN3 5-0 = 110001	((156R - 98R ) / 450R) * VSPR
	VRN3 5-0 = 110010	((156R - 100R ) / 450R) * VSPR
	VRN3 5-0 = 110011	((156R - 102R ) / 450R) * VSPR
	VRN3 5-0 = 110100	((156R - 104R ) / 450R) * VSPR
	VRN3 5-0 = 110101	((156R - 106R ) / 450R) * VSPR
	VRN3 5-0 = 110110	((156R - 108R ) / 450R) * VSPR
	VRN3 5-0 = 110111	((156R - 110R ) / 450R) * VSPR
	VRN3 5-0 = 111000	((156R - 112R ) / 450R) * VSPR
	VRN3 5-0 = 111001	((156R - 114R ) / 450R) * VSPR
	VRN3 5-0 = 111010	((156R - 116R ) / 450R) * VSPR
	VRN3 5-0 = 111011	((156R - 118R ) / 450R) * VSPR
	VRN3 5-0 = 111100	((156R - 120R ) / 450R) * VSPR
	VRN3 5-0 = 111101	((156R - 122R ) / 450R) * VSPR
	VRN3 5-0 = 111110	((156R - 124R ) / 450R) * VSPR
	VRN3 5-0 = 111111	((156R - 126R ) / 450R) * VSPR

Table 5.30: VinN18

Reference voltage	Macro adjustment value	VinN19 formula
VinN19	VRN4 5-0 = 000000	((146R / 450R) * VSPR
	VRN4 5-0 = 000001	((146R - 2R ) / 450R) * VSPR
	VRN4 5-0 = 000010	((146R - 4R ) / 450R) * VSPR
	VRN4 5-0 = 000011	((146R - 6R ) / 450R) * VSPR
	VRN4 5-0 = 000100	((146R - 8R ) / 450R) * VSPR
	VRN4 5-0 = 000101	((146R - 10R ) / 450R) * VSPR
	VRN4 5-0 = 000110	((146R - 12R ) / 450R) * VSPR
	VRN4 5-0 = 000111	((146R - 14R ) / 450R) * VSPR
	VRN4 5-0 = 001000	((146R - 16R ) / 450R) * VSPR
	VRN4 5-0 = 001001	((146R - 18R ) / 450R) * VSPR
	VRN4 5-0 = 001010	((146R - 20R ) / 450R) * VSPR
	VRN4 5-0 = 001011	((146R - 22R ) / 450R) * VSPR
	VRN4 5-0 = 001100	((146R - 24R ) / 450R) * VSPR
	VRN4 5-0 = 001101	((146R - 26R ) / 450R) * VSPR
	VRN4 5-0 = 001110	((146R - 28R ) / 450R) * VSPR
	VRN4 5-0 = 001111	((146R - 30R ) / 450R) * VSPR
	VRN4 5-0 = 010000	((146R - 32R ) / 450R) * VSPR
	VRN4 5-0 = 010001	((146R - 34R ) / 450R) * VSPR
	VRN4 5-0 = 010010	((146R - 36R ) / 450R) * VSPR
	VRN4 5-0 = 010011	((146R - 38R ) / 450R) * VSPR
	VRN4 5-0 = 010100	((146R - 40R ) / 450R) * VSPR
	VRN4 5-0 = 010101	((146R - 42R ) / 450R) * VSPR
	VRN4 5-0 = 010110	((146R - 44R ) / 450R) * VSPR
	VRN4 5-0 = 010111	((146R - 46R ) / 450R) * VSPR
	VRN4 5-0 = 011000	((146R - 48R ) / 450R) * VSPR
	VRN4 5-0 = 011001	((146R - 50R ) / 450R) * VSPR
	VRN4 5-0 = 011010	((146R - 52R ) / 450R) * VSPR
	VRN4 5-0 = 011011	((146R - 54R ) / 450R) * VSPR
	VRN4 5-0 = 011100	((146R - 56R ) / 450R) * VSPR
	VRN4 5-0 = 011101	((146R - 58R ) / 450R) * VSPR
	VRN4 5-0 = 011110	((146R - 60R ) / 450R) * VSPR
	VRN4 5-0 = 011111	((146R - 62R ) / 450R) * VSPR
	VRN4 5-0 = 100000	((146R - 64R ) / 450R) * VSPR
	VRN4 5-0 = 100001	((146R - 66R ) / 450R) * VSPR
	VRN4 5-0 = 100010	((146R - 68R ) / 450R) * VSPR
	VRN4 5-0 = 100011	((146R - 70R ) / 450R) * VSPR
	VRN4 5-0 = 100100	((146R - 72R ) / 450R) * VSPR
	VRN4 5-0 = 100101	((146R - 74R ) / 450R) * VSPR
	VRN4 5-0 = 100110	((146R - 76R ) / 450R) * VSPR
	VRN4 5-0 = 100111	((146R - 78R ) / 450R) * VSPR
	VRN4 5-0 = 101000	((146R - 80R ) / 450R) * VSPR
	VRN4 5-0 = 101001	((146R - 82R ) / 450R) * VSPR
	VRN4 5-0 = 101010	((146R - 84R ) / 450R) * VSPR
	VRN4 5-0 = 101011	((146R - 86R ) / 450R) * VSPR
	VRN4 5-0 = 101100	((146R - 88R ) / 450R) * VSPR
	VRN4 5-0 = 101101	((146R - 90R ) / 450R) * VSPR
	VRN4 5-0 = 101110	((146R - 92R ) / 450R) * VSPR
	VRN4 5-0 = 101111	((146R - 94R ) / 450R) * VSPR
	VRN4 5-0 = 110000	((146R - 96R ) / 450R) * VSPR
	VRN4 5-0 = 110001	((146R - 98R ) / 450R) * VSPR
	VRN4 5-0 = 110010	((146R - 100R ) / 450R) * VSPR
	VRN4 5-0 = 110011	((146R - 102R ) / 450R) * VSPR
	VRN4 5-0 = 110100	((146R - 104R ) / 450R) * VSPR
	VRN4 5-0 = 110101	((146R - 106R ) / 450R) * VSPR
	VRN4 5-0 = 110110	((146R - 108R ) / 450R) * VSPR
	VRN4 5-0 = 110111	((146R - 110R ) / 450R) * VSPR
	VRN4 5-0 = 111000	((146R - 112R ) / 450R) * VSPR
	VRN4 5-0 = 111001	((146R - 114R ) / 450R) * VSPR
	VRN4 5-0 = 111010	((146R - 116R ) / 450R) * VSPR
	VRN4 5-0 = 111011	((146R - 118R ) / 450R) * VSPR
	VRN4 5-0 = 111100	((146R - 120R ) / 450R) * VSPR
	VRN4 5-0 = 111101	((146R - 122R ) / 450R) * VSPR
	VRN4 5-0 = 111110	((146R - 124R ) / 450R) * VSPR
	VRN4 5-0 = 111111	((146R - 126R ) / 450R) * VSPR

Table 5.31: VinN19

Reference voltage	Macro adjustment value	VinN20 formula
VinN20	VRN5 5-0 = 000000	((144R / 450R) * VSPR
	VRN5 5-0 = 000001	((144R - 2R ) / 450R) * VSPR
	VRN5 5-0 = 000010	((144R - 4R ) / 450R) * VSPR
	VRN5 5-0 = 000011	((144R - 6R ) / 450R) * VSPR
	VRN5 5-0 = 000100	((144R - 8R ) / 450R) * VSPR
	VRN5 5-0 = 000101	((144R - 10R ) / 450R) * VSPR
	VRN5 5-0 = 000110	((144R - 12R ) / 450R) * VSPR
	VRN5 5-0 = 000111	((144R - 14R ) / 450R) * VSPR
	VRN5 5-0 = 001000	((144R - 16R ) / 450R) * VSPR
	VRN5 5-0 = 001001	((144R - 18R ) / 450R) * VSPR
	VRN5 5-0 = 001010	((144R - 20R ) / 450R) * VSPR
	VRN5 5-0 = 001011	((144R - 22R ) / 450R) * VSPR
	VRN5 5-0 = 001100	((144R - 24R ) / 450R) * VSPR
	VRN5 5-0 = 001101	((144R - 26R ) / 450R) * VSPR
	VRN5 5-0 = 001110	((144R - 28R ) / 450R) * VSPR
	VRN5 5-0 = 001111	((144R - 30R ) / 450R) * VSPR
	VRN5 5-0 = 010000	((144R - 32R ) / 450R) * VSPR
	VRN5 5-0 = 010001	((144R - 34R ) / 450R) * VSPR
	VRN5 5-0 = 010010	((144R - 36R ) / 450R) * VSPR
	VRN5 5-0 = 010011	((144R - 38R ) / 450R) * VSPR
	VRN5 5-0 = 010100	((144R - 40R ) / 450R) * VSPR
	VRN5 5-0 = 010101	((144R - 42R ) / 450R) * VSPR
	VRN5 5-0 = 010110	((144R - 44R ) / 450R) * VSPR
	VRN5 5-0 = 010111	((144R - 46R ) / 450R) * VSPR
	VRN5 5-0 = 011000	((144R - 48R ) / 450R) * VSPR
	VRN5 5-0 = 011001	((144R - 50R ) / 450R) * VSPR
	VRN5 5-0 = 011010	((144R - 52R ) / 450R) * VSPR
	VRN5 5-0 = 011011	((144R - 54R ) / 450R) * VSPR
	VRN5 5-0 = 011100	((144R - 56R ) / 450R) * VSPR
	VRN5 5-0 = 011101	((144R - 58R ) / 450R) * VSPR
	VRN5 5-0 = 011110	((144R - 60R ) / 450R) * VSPR
	VRN5 5-0 = 011111	((144R - 62R ) / 450R) * VSPR
	VRN5 5-0 = 100000	((144R - 64R ) / 450R) * VSPR
	VRN5 5-0 = 100001	((144R - 66R ) / 450R) * VSPR
	VRN5 5-0 = 100010	((144R - 68R ) / 450R) * VSPR
	VRN5 5-0 = 100011	((144R - 70R ) / 450R) * VSPR
	VRN5 5-0 = 100100	((144R - 72R ) / 450R) * VSPR
	VRN5 5-0 = 100101	((144R - 74R ) / 450R) * VSPR
	VRN5 5-0 = 100110	((144R - 76R ) / 450R) * VSPR
	VRN5 5-0 = 100111	((144R - 78R ) / 450R) * VSPR
	VRN5 5-0 = 101000	((144R - 80R ) / 450R) * VSPR
	VRN5 5-0 = 101001	((144R - 82R ) / 450R) * VSPR
	VRN5 5-0 = 101010	((144R - 84R ) / 450R) * VSPR
	VRN5 5-0 = 101011	((144R - 86R ) / 450R) * VSPR
	VRN5 5-0 = 101100	((144R - 88R ) / 450R) * VSPR
	VRN5 5-0 = 101101	((144R - 90R ) / 450R) * VSPR
	VRN5 5-0 = 101110	((144R - 92R ) / 450R) * VSPR
	VRN5 5-0 = 101111	((144R - 94R ) / 450R) * VSPR
	VRN5 5-0 = 110000	((144R - 96R ) / 450R) * VSPR
	VRN5 5-0 = 110001	((144R - 98R ) / 450R) * VSPR
	VRN5 5-0 = 110010	((144R - 100R) / 450R) * VSPR
	VRN5 5-0 = 110011	((144R - 102R) / 450R) * VSPR
	VRN5 5-0 = 110100	((144R - 104R) / 450R) * VSPR
	VRN5 5-0 = 110101	((144R - 106R) / 450R) * VSPR
	VRN5 5-0 = 110110	((144R - 108R) / 450R) * VSPR
	VRN5 5-0 = 110111	((144R - 110R) / 450R) * VSPR
	VRN5 5-0 = 111000	((144R - 112R) / 450R) * VSPR
	VRN5 5-0 = 111001	((144R - 114R) / 450R) * VSPR
	VRN5 5-0 = 111010	((144R - 116R) / 450R) * VSPR
	VRN5 5-0 = 111011	((144R - 118R) / 450R) * VSPR
	VRN5 5-0 = 111100	((144R - 120R) / 450R) * VSPR
	VRN5 5-0 = 111101	((144R - 122R) / 450R) * VSPR
	VRN5 5-0 = 111110	((144R - 124R) / 450R) * VSPR
	VRN5 5-0 = 111111	VGSP

Table 5.32: VinN20

Reference voltage	Macro adjustment value	VinN7 formula
VinN7	PRN0 6-0 = 0000000	(350R / 450R) * VSPR
	PRN0 6-0 = 0000001	((350R - 2R) / 450R) * VSPR
	PRN0 6-0 = 0000010	((350R - 4R) / 450R) * VSPR
	PRN0 6-0 = 0000011	((350R - 6R) / 450R) * VSPR
	PRN0 6-0 = 00000100	((350R - 8R) / 450R) * VSPR
	PRN0 6-0 = 00000101	((350R - 10R) / 450R) * VSPR
	PRN0 6-0 = 00000110	((350R - 12R) / 450R) * VSPR
	PRN0 6-0 = 00000111	((350R - 14R) / 450R) * VSPR
	PRN0 6-0 = 0001000	((350R - 16R) / 450R) * VSPR
	PRN0 6-0 = 0001001	((350R - 18R) / 450R) * VSPR
	PRN0 6-0 = 0001010	((350R - 20R) / 450R) * VSPR
	PRN0 6-0 = 0001011	((350R - 22R) / 450R) * VSPR
	PRN0 6-0 = 0001100	((350R - 24R) / 450R) * VSPR
	PRN0 6-0 = 0001101	((350R - 26R) / 450R) * VSPR
	PRN0 6-0 = 0001110	((350R - 28R) / 450R) * VSPR
	PRN0 6-0 = 0001111	((350R - 30R) / 450R) * VSPR
	PRN0 6-0 = 0010000	((350R - 32R) / 450R) * VSPR
	PRN0 6-0 = 0010001	((350R - 34R) / 450R) * VSPR
	PRN0 6-0 = 0010010	((350R - 36R) / 450R) * VSPR
	PRN0 6-0 = 0010011	((350R - 38R) / 450R) * VSPR
	PRN0 6-0 = 0010100	((350R - 40R) / 450R) * VSPR
	PRN0 6-0 = 0010101	((350R - 42R) / 450R) * VSPR
	PRN0 6-0 = 0010110	((350R - 44R) / 450R) * VSPR
	PRN0 6-0 = 0010111	((350R - 46R) / 450R) * VSPR
	PRN0 6-0 = 0011000	((350R - 48R) / 450R) * VSPR
	PRN0 6-0 = 0011001	((350R - 50R) / 450R) * VSPR
	PRN0 6-0 = 0011010	((350R - 52R) / 450R) * VSPR
	PRN0 6-0 = 0011011	((350R - 54R) / 450R) * VSPR
	PRN0 6-0 = 0011100	((350R - 56R) / 450R) * VSPR
	PRN0 6-0 = 0011101	((350R - 58R) / 450R) * VSPR
	PRN0 6-0 = 0011110	((350R - 60R) / 450R) * VSPR
	PRN0 6-0 = 0011111	((350R - 62R) / 450R) * VSPR
	PRN0 6-0 = 0100000	((350R - 64R) / 450R) * VSPR
	PRN0 6-0 = 0100001	((350R - 66R) / 450R) * VSPR
	PRN0 6-0 = 0100010	((350R - 68R) / 450R) * VSPR
	PRN0 6-0 = 0100011	((350R - 70R) / 450R) * VSPR
	PRN0 6-0 = 0100100	((350R - 72R) / 450R) * VSPR
	PRN0 6-0 = 0100101	((350R - 74R) / 450R) * VSPR
	PRN0 6-0 = 0100110	((350R - 76R) / 450R) * VSPR
	PRN0 6-0 = 0100111	((350R - 78R) / 450R) * VSPR
	PRN0 6-0 = 0101000	((350R - 80R) / 450R) * VSPR
	PRN0 6-0 = 0101001	((350R - 82R) / 450R) * VSPR
	PRN0 6-0 = 0101010	((350R - 84R) / 450R) * VSPR
	PRN0 6-0 = 0101011	((350R - 86R) / 450R) * VSPR
	PRN0 6-0 = 0101100	((350R - 88R) / 450R) * VSPR
	PRN0 6-0 = 0101101	((350R - 90R) / 450R) * VSPR
	PRN0 6-0 = 0101110	((350R - 92R) / 450R) * VSPR
	PRN0 6-0 = 0101111	((350R - 94R) / 450R) * VSPR
	PRN0 6-0 = 0110000	((350R - 96R) / 450R) * VSPR
	PRN0 6-0 = 0110001	((350R - 98R) / 450R) * VSPR
	PRN0 6-0 = 0110010	((350R - 100R) / 450R) * VSPR
	PRN0 6-0 = 0110011	((350R - 102R) / 450R) * VSPR
	PRN0 6-0 = 0110100	((350R - 104R) / 450R) * VSPR
	PRN0 6-0 = 0110101	((350R - 106R) / 450R) * VSPR
	PRN0 6-0 = 0110110	((350R - 108R) / 450R) * VSPR
	PRN0 6-0 = 0110111	((350R - 110R) / 450R) * VSPR
	PRN0 6-0 = 0111000	((350R - 112R) / 450R) * VSPR
	PRN0 6-0 = 0111001	((350R - 114R) / 450R) * VSPR
	PRN0 6-0 = 0111010	((350R - 116R) / 450R) * VSPR
	PRN0 6-0 = 0111011	((350R - 118R) / 450R) * VSPR
	PRN0 6-0 = 0111100	((350R - 120R) / 450R) * VSPR
	PRN0 6-0 = 0111101	((350R - 122R) / 450R) * VSPR
	PRN0 6-0 = 0111110	((350R - 124R) / 450R) * VSPR
	PRN0 6-0 = 0111111	((350R - 126R) / 450R) * VSPR
PRN0 6-0 = 1000000	((350R - 128R) / 450R) * VSPR	
PRN0 6-0 = 1000001	((350R - 130R) / 450R) * VSPR	
PRN0 6-0 = 1000010	((350R - 132R) / 450R) * VSPR	
PRN0 6-0 = 1000011	((350R - 134R) / 450R) * VSPR	
PRN0 6-0 = 1000100	((350R - 136R) / 450R) * VSPR	

Reference voltage	Macro adjustment value	VinN7 formula
	PRN0 6-0 = 1000101	$((350R - 138R) / 450R) * VSPR$
	PRN0 6-0 = 1000110	$((350R - 140R) / 450R) * VSPR$
	PRN0 6-0 = 1000111	$((350R - 142R) / 450R) * VSPR$
	PRN0 6-0 = 1001000	$((350R - 144R) / 450R) * VSPR$
	PRN0 6-0 = 1001001	$((350R - 146R) / 450R) * VSPR$
	PRN0 6-0 = 1001010	$((350R - 148R) / 450R) * VSPR$
	PRN0 6-0 = 1001011	$((350R - 150R) / 450R) * VSPR$
	PRN0 6-0 = 1001100	$((350R - 152R) / 450R) * VSPR$
	PRN0 6-0 = 1001101	$((350R - 154R) / 450R) * VSPR$
	PRN0 6-0 = 1001110	$((350R - 156R) / 450R) * VSPR$
	PRN0 6-0 = 1001111	$((350R - 158R) / 450R) * VSPR$
	PRN0 6-0 = 1010000	$((350R - 160R) / 450R) * VSPR$
	PRN0 6-0 = 1010001	$((350R - 162R) / 450R) * VSPR$
	PRN0 6-0 = 1010010	$((350R - 164R) / 450R) * VSPR$
	PRN0 6-0 = 1010011	$((350R - 166R) / 450R) * VSPR$
	PRN0 6-0 = 1010100	$((350R - 168R) / 450R) * VSPR$
	PRN0 6-0 = 1010101	$((350R - 170R) / 450R) * VSPR$
	PRN0 6-0 = 1010110	$((350R - 172R) / 450R) * VSPR$
	PRN0 6-0 = 1010111	$((350R - 174R) / 450R) * VSPR$
	PRN0 6-0 = 1011000	inhibit
	PRN0 6-0 = 1011001	inhibit
	PRN0 6-0 = 1011010	inhibit
	PRN0 6-0 = 1011011	inhibit
	PRN0 6-0 = 1011100	inhibit
	PRN0 6-0 = 1011101	inhibit
	PRN0 6-0 = 1011110	inhibit
	PRN0 6-0 = 1011111	inhibit
	PRN0 6-0 = 1100000	inhibit
	PRN0 6-0 = 1100001	inhibit
	PRN0 6-0 = 1100010	inhibit
	PRN0 6-0 = 1100011	inhibit
	PRN0 6-0 = 1100100	inhibit
	PRN0 6-0 = 1100101	inhibit
	PRN0 6-0 = 1100110	inhibit
	PRN0 6-0 = 1100111	inhibit
	PRN0 6-0 = 1101000	inhibit
	PRN0 6-0 = 1101001	inhibit
	PRN0 6-0 = 1101010	inhibit
	PRN0 6-0 = 1101011	inhibit
	PRN0 6-0 = 1101100	inhibit
	PRN0 6-0 = 1101101	inhibit
	PRN0 6-0 = 1101110	inhibit
	PRN0 6-0 = 1101111	inhibit
	PRN0 6-0 = 1110000	inhibit
	PRN0 6-0 = 1110001	inhibit
	PRN0 6-0 = 1110010	inhibit
	PRN0 6-0 = 1110011	inhibit
	PRN0 6-0 = 1110100	inhibit
	PRN0 6-0 = 1110101	inhibit
	PRN0 6-0 = 1110110	inhibit
	PRN0 6-0 = 1110111	inhibit
	PRN0 6-0 = 1111000	inhibit
	PRN0 6-0 = 1111001	inhibit
	PRN0 6-0 = 1111010	inhibit
	PRN0 6-0 = 1111011	inhibit
	PRN0 6-0 = 1111100	inhibit
	PRN0 6-0 = 1111101	inhibit
	PRN0 6-0 = 1111110	inhibit
	PRN0 6-0 = 1111111	inhibit

Table 5.33: VinN7

Reference voltage	Macro adjustment value	VinN13 formula
VinN13	PRN1 6-0 = 0000000	((274R / 450R) * VSPR)
	PRN1 6-0 = 0000001	((274R - 2R) / 450R) * VSPR
	PRN1 6-0 = 0000010	((274R - 4R) / 450R) * VSPR
	PRN1 6-0 = 0000011	((274R - 6R) / 450R) * VSPR
	PRN1 6-0 = 00000100	((274R - 8R) / 450R) * VSPR
	PRN1 6-0 = 00000101	((274R - 10R) / 450R) * VSPR
	PRN1 6-0 = 00000110	((274R - 12R) / 450R) * VSPR
	PRN1 6-0 = 00000111	((274R - 14R) / 450R) * VSPR
	PRN1 6-0 = 0001000	((274R - 16R) / 450R) * VSPR
	PRN1 6-0 = 0001001	((274R - 18R) / 450R) * VSPR
	PRN1 6-0 = 0001010	((274R - 20R) / 450R) * VSPR
	PRN1 6-0 = 0001011	((274R - 22R) / 450R) * VSPR
	PRN1 6-0 = 0001100	((274R - 24R) / 450R) * VSPR
	PRN1 6-0 = 0001101	((274R - 26R) / 450R) * VSPR
	PRN1 6-0 = 0001110	((274R - 28R) / 450R) * VSPR
	PRN1 6-0 = 0001111	((274R - 30R) / 450R) * VSPR
	PRN1 6-0 = 0010000	((274R - 32R) / 450R) * VSPR
	PRN1 6-0 = 0010001	((274R - 34R) / 450R) * VSPR
	PRN1 6-0 = 0010010	((274R - 36R) / 450R) * VSPR
	PRN1 6-0 = 0010011	((274R - 38R) / 450R) * VSPR
	PRN1 6-0 = 0010100	((274R - 40R) / 450R) * VSPR
	PRN1 6-0 = 0010101	((274R - 42R) / 450R) * VSPR
	PRN1 6-0 = 0010110	((274R - 44R) / 450R) * VSPR
	PRN1 6-0 = 0010111	((274R - 46R) / 450R) * VSPR
	PRN1 6-0 = 0011000	((274R - 48R) / 450R) * VSPR
	PRN1 6-0 = 0011001	((274R - 50R) / 450R) * VSPR
	PRN1 6-0 = 0011010	((274R - 52R) / 450R) * VSPR
	PRN1 6-0 = 0011011	((274R - 54R) / 450R) * VSPR
	PRN1 6-0 = 0011100	((274R - 56R) / 450R) * VSPR
	PRN1 6-0 = 0011101	((274R - 58R) / 450R) * VSPR
	PRN1 6-0 = 0011110	((274R - 60R) / 450R) * VSPR
	PRN1 6-0 = 0011111	((274R - 62R) / 450R) * VSPR
	PRN1 6-0 = 0100000	((274R - 64R) / 450R) * VSPR
	PRN1 6-0 = 0100001	((274R - 66R) / 450R) * VSPR
	PRN1 6-0 = 0100010	((274R - 68R) / 450R) * VSPR
	PRN1 6-0 = 0100011	((274R - 70R) / 450R) * VSPR
	PRN1 6-0 = 0100100	((274R - 72R) / 450R) * VSPR
	PRN1 6-0 = 0100101	((274R - 74R) / 450R) * VSPR
	PRN1 6-0 = 0100110	((274R - 76R) / 450R) * VSPR
	PRN1 6-0 = 0100111	((274R - 78R) / 450R) * VSPR
	PRN1 6-0 = 0101000	((274R - 80R) / 450R) * VSPR
	PRN1 6-0 = 0101001	((274R - 82R) / 450R) * VSPR
	PRN1 6-0 = 0101010	((274R - 84R) / 450R) * VSPR
	PRN1 6-0 = 0101011	((274R - 86R) / 450R) * VSPR
	PRN1 6-0 = 0101100	((274R - 88R) / 450R) * VSPR
	PRN1 6-0 = 0101101	((274R - 90R) / 450R) * VSPR
	PRN1 6-0 = 0101110	((274R - 92R) / 450R) * VSPR
	PRN1 6-0 = 0101111	((274R - 94R) / 450R) * VSPR
	PRN1 6-0 = 0110000	((274R - 96R) / 450R) * VSPR
	PRN1 6-0 = 0110001	((274R - 98R) / 450R) * VSPR
	PRN1 6-0 = 0110010	((274R - 100R) / 450R) * VSPR
	PRN1 6-0 = 0110011	((274R - 102R) / 450R) * VSPR
	PRN1 6-0 = 0110100	((274R - 104R) / 450R) * VSPR
	PRN1 6-0 = 0110101	((274R - 106R) / 450R) * VSPR
	PRN1 6-0 = 0110110	((274R - 108R) / 450R) * VSPR
	PRN1 6-0 = 0110111	((274R - 110R) / 450R) * VSPR
	PRN1 6-0 = 0111000	((274R - 112R) / 450R) * VSPR
	PRN1 6-0 = 0111001	((274R - 114R) / 450R) * VSPR
	PRN1 6-0 = 0111010	((274R - 116R) / 450R) * VSPR
	PRN1 6-0 = 0111011	((274R - 118R) / 450R) * VSPR
	PRN1 6-0 = 0111100	((274R - 120R) / 450R) * VSPR
	PRN1 6-0 = 0111101	((274R - 122R) / 450R) * VSPR
	PRN1 6-0 = 0111110	((274R - 124R) / 450R) * VSPR
	PRN1 6-0 = 0111111	((274R - 126R) / 450R) * VSPR
	PRN1 6-0 = 1000000	((274R - 128R) / 450R) * VSPR
	PRN1 6-0 = 1000001	((274R - 130R) / 450R) * VSPR
	PRN1 6-0 = 1000010	((274R - 132R) / 450R) * VSPR
	PRN1 6-0 = 1000011	((274R - 134R) / 450R) * VSPR
	PRN1 6-0 = 1000100	((274R - 136R) / 450R) * VSPR

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Reference voltage	Macro adjustment value	VinN13 formula
	PRN1 6-0 = 1000101	$((274R - 138R) / 450R) * VSPR$
	PRN1 6-0 = 1000110	$((274R - 140R) / 450R) * VSPR$
	PRN1 6-0 = 1000111	$((274R - 142R) / 450R) * VSPR$
	PRN1 6-0 = 1001000	$((274R - 144R) / 450R) * VSPR$
	PRN1 6-0 = 1001001	$((274R - 146R) / 450R) * VSPR$
	PRN1 6-0 = 1001010	$((274R - 148R) / 450R) * VSPR$
	PRN1 6-0 = 1001011	$((274R - 150R) / 450R) * VSPR$
	PRN1 6-0 = 1001100	$((274R - 152R) / 450R) * VSPR$
	PRN1 6-0 = 1001101	$((274R - 154R) / 450R) * VSPR$
	PRN1 6-0 = 1001110	$((274R - 156R) / 450R) * VSPR$
	PRN1 6-0 = 1001111	$((274R - 158R) / 450R) * VSPR$
	PRN1 6-0 = 1010000	$((274R - 160R) / 450R) * VSPR$
	PRN1 6-0 = 1010001	$((274R - 162R) / 450R) * VSPR$
	PRN1 6-0 = 1010010	$((274R - 164R) / 450R) * VSPR$
	PRN1 6-0 = 1010011	$((274R - 166R) / 450R) * VSPR$
	PRN1 6-0 = 1010100	$((274R - 168R) / 450R) * VSPR$
	PRN1 6-0 = 1010101	$((274R - 170R) / 450R) * VSPR$
	PRN1 6-0 = 1010110	$((274R - 172R) / 450R) * VSPR$
	PRN1 6-0 = 1010111	$((274R - 174R) / 450R) * VSPR$
	PRN1 6-0 = 1011000	inhibit
	PRN1 6-0 = 1011001	inhibit
	PRN1 6-0 = 1011010	inhibit
	PRN1 6-0 = 1011011	inhibit
	PRN1 6-0 = 1011100	inhibit
	PRN1 6-0 = 1011101	inhibit
	PRN1 6-0 = 1011110	inhibit
	PRN1 6-0 = 1011111	inhibit
	PRN1 6-0 = 1100000	inhibit
	PRN1 6-0 = 1100001	inhibit
	PRN1 6-0 = 1100010	inhibit
	PRN1 6-0 = 1100011	inhibit
	PRN1 6-0 = 1100100	inhibit
	PRN1 6-0 = 1100101	inhibit
	PRN1 6-0 = 1100110	inhibit
	PRN1 6-0 = 1100111	inhibit
	PRN1 6-0 = 1101000	inhibit
	PRN1 6-0 = 1101001	inhibit
	PRN1 6-0 = 1101010	inhibit
	PRN1 6-0 = 1101011	inhibit
	PRN1 6-0 = 1101100	inhibit
	PRN1 6-0 = 1101101	inhibit
	PRN1 6-0 = 1101110	inhibit
	PRN1 6-0 = 1101111	inhibit
	PRN1 6-0 = 1110000	inhibit
	PRN1 6-0 = 1110001	inhibit
	PRN1 6-0 = 1110010	inhibit
	PRN1 6-0 = 1110011	inhibit
	PRN1 6-0 = 1110100	inhibit
	PRN1 6-0 = 1110101	inhibit
	PRN1 6-0 = 1110110	inhibit
	PRN1 6-0 = 1110111	inhibit
	PRN1 6-0 = 1111000	inhibit
	PRN1 6-0 = 1111001	inhibit
	PRN1 6-0 = 1111010	inhibit
	PRN1 6-0 = 1111011	inhibit
	PRN1 6-0 = 1111100	inhibit
	PRN1 6-0 = 1111101	inhibit
	PRN1 6-0 = 1111110	inhibit
	PRN1 6-0 = 1111111	inhibit

Table 5.34: VinN13

Reference voltage	Macro adjustment value	VinN3 formula
VinN3	PKN0 4-0 = 00000	$(47R / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 00001	$((47R - 1R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 00010	$((47R - 2R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 00011	$((47R - 3R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 00100	$((47R - 4R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 00101	$((47R - 5R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 00110	$((47R - 6R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 00111	$((47R - 7R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 01000	$((47R - 8R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 01001	$((47R - 9R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 01010	$((47R - 10R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 01011	$((47R - 11R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 01100	$((47R - 12R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 01101	$((47R - 13R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 01110	$((47R - 14R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 01111	$((47R - 15R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 10000	$((47R - 16R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 10001	$((47R - 17R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 10010	$((47R - 18R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 10011	$((47R - 19R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 10100	$((47R - 20R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 10101	$((47R - 21R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 10110	$((47R - 22R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 10111	$((47R - 23R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 11000	$((47R - 24R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 11001	$((47R - 25R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 11010	$((47R - 26R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 11011	$((47R - 27R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 11100	$((47R - 28R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 11101	$((47R - 29R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 11110	$((47R - 30R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN0 4-0 = 11111	$((47R - 31R) / 48R) * (VinN2 - VinN7) + VinN7$

Table 5.35: VinN3

Reference voltage	Macro adjustment value	VinN4 formula
VinN4	PKN1 4-0 = 00000	$(39R / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 00001	$((39R - 1R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 00010	$((39R - 2R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 00011	$((39R - 3R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 00100	$((39R - 4R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 00101	$((39R - 5R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 00110	$((39R - 6R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 00111	$((39R - 7R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 01000	$((39R - 8R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 01001	$((39R - 9R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 01010	$((39R - 10R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 01011	$((39R - 11R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 01100	$((39R - 12R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 01101	$((39R - 13R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 01110	$((39R - 14R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 01111	$((39R - 15R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 10000	$((39R - 16R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 10001	$((39R - 17R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 10010	$((39R - 18R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 10011	$((39R - 19R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 10100	$((39R - 20R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 10101	$((39R - 21R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 10110	$((39R - 22R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 10111	$((39R - 23R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 11000	$((39R - 24R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 11001	$((39R - 25R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 11010	$((39R - 26R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 11011	$((39R - 27R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 11100	$((39R - 28R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 11101	$((39R - 29R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 11110	$((39R - 30R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN1 4-0 = 11111	$((39R - 31R) / 48R) * (VinN2 - VinN7) + VinN7$

Table 5.36: VinN4

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Reference voltage	Macro adjustment value	VinN5 formula
VinN5	PKN2 4-0 = 00000	$(32R / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 00001	$((32R - 1R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 00010	$((32R - 2R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 00011	$((32R - 3R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 00100	$((32R - 4R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 00101	$((32R - 5R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 00110	$((32R - 6R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 00111	$((32R - 7R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 01000	$((32R - 8R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 01001	$((32R - 9R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 01010	$((32R - 10R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 01011	$((32R - 11R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 01100	$((32R - 12R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 01101	$((32R - 13R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 01110	$((32R - 14R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 01111	$((32R - 15R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 10000	$((32R - 16R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 10001	$((32R - 17R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 10010	$((32R - 18R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 10011	$((32R - 19R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 10100	$((32R - 20R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 10101	$((32R - 21R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 10110	$((32R - 22R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 10111	$((32R - 23R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 11000	$((32R - 24R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 11001	$((32R - 25R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 11010	$((32R - 26R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 11011	$((32R - 27R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 11100	$((32R - 28R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 11101	$((32R - 29R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 11110	$((32R - 30R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN2 4-0 = 11111	$((32R - 31R) / 48R) * (VinN2 - VinN7) + VinN7$

Table 5.37: VinN5

Reference voltage	Macro adjustment value	VinN6 formula
VinN6	PKN3 4-0 = 00000	$(32R / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 00001	$((32R - 1R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 00010	$((32R - 2R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 00011	$((32R - 3R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 00100	$((32R - 4R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 00101	$((32R - 5R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 00110	$((32R - 6R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 00111	$((32R - 7R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 01000	$((32R - 8R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 01001	$((32R - 9R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 01010	$((32R - 10R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 01011	$((32R - 11R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 01100	$((32R - 12R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 01101	$((32R - 13R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 01110	$((32R - 14R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 01111	$((32R - 15R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 10000	$((32R - 16R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 10001	$((32R - 17R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 10010	$((32R - 18R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 10011	$((32R - 19R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 10100	$((32R - 20R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 10101	$((32R - 21R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 10110	$((32R - 22R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 10111	$((32R - 23R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 11000	$((32R - 24R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 11001	$((32R - 25R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 11010	$((32R - 26R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 11011	$((32R - 27R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 11100	$((32R - 28R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 11101	$((32R - 29R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 11110	$((32R - 30R) / 48R) * (VinN2 - VinN7) + VinN7$
	PKN3 4-0 = 11111	$((32R - 31R) / 48R) * (VinN2 - VinN7) + VinN7$

Table 5.38: VinN6

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Reference voltage	Macro adjustment value	VinN8 formula
VinN8	PKN4 4-0 = 00000	$(220R / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 00001	$((220R - 3R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 00010	$((220R - 6R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 00011	$((220R - 9R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 00100	$((220R - 12R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 00101	$((220R - 15R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 00110	$((220R - 18R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 00111	$((220R - 21R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 01000	$((220R - 24R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 01001	$((220R - 27R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 01010	$((220R - 30R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 01011	$((220R - 33R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 01100	$((220R - 36R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 01101	$((220R - 39R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 01110	$((220R - 42R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 01111	$((220R - 45R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 10000	$((220R - 48R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 10001	$((220R - 51R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 10010	$((220R - 54R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 10011	$((220R - 57R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 10100	$((220R - 60R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 10101	$((220R - 63R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 10110	$((220R - 66R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 10111	$((220R - 69R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 11000	$((220R - 72R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 11001	$((220R - 75R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 11010	$((220R - 78R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 11011	$((220R - 81R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 11100	$((220R - 84R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 11101	$((220R - 87R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 11110	$((220R - 90R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN4 4-0 = 11111	$((220R - 93R) / 223R) * (VinN7 - VinN13) + VinN13$

Table 5.39: VinN8

Reference voltage	Macro adjustment value	VinN9 formula
VinN9	PKN5 4-0 = 00000	$(193R / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 00001	$((193R - 3R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 00010	$((193R - 6R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 00011	$((193R - 9R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 00100	$((193R - 12R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 00101	$((193R - 15R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 00110	$((193R - 18R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 00111	$((193R - 21R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 01000	$((193R - 24R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 01001	$((193R - 27R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 01010	$((193R - 30R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 01011	$((193R - 33R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 01100	$((193R - 36R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 01101	$((193R - 39R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 01110	$((193R - 42R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 01111	$((193R - 45R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 10000	$((193R - 48R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 10001	$((193R - 51R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 10010	$((193R - 54R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 10011	$((193R - 57R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 10100	$((193R - 60R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 10101	$((193R - 63R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 10110	$((193R - 66R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 10111	$((193R - 69R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 11000	$((193R - 72R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 11001	$((193R - 75R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 11010	$((193R - 78R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 11011	$((193R - 81R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 11100	$((193R - 84R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 11101	$((193R - 87R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 11110	$((193R - 90R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN5 4-0 = 11111	$((193R - 93R) / 223R) * (VinN7 - VinN13) + VinN13$

Table 5.40: VinN9

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Reference voltage	Macro adjustment value	VinN10 formula
VinN10	PKN6 4-0 = 00000	$(158R / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 00001	$((158R - 3R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 00010	$((158R - 6R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 00011	$((158R - 9R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 00100	$((158R - 12R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 00101	$((158R - 15R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 00110	$((158R - 18R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 00111	$((158R - 21R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 01000	$((158R - 24R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 01001	$((158R - 27R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 01010	$((158R - 30R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 01011	$((158R - 33R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 01100	$((158R - 36R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 01101	$((158R - 39R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 01110	$((158R - 42R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 01111	$((158R - 45R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 10000	$((158R - 48R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 10001	$((158R - 51R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 10010	$((158R - 54R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 10011	$((158R - 57R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 10100	$((158R - 60R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 10101	$((158R - 63R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 10110	$((158R - 66R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 10111	$((158R - 69R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 11000	$((158R - 72R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 11001	$((158R - 75R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 11010	$((158R - 78R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 11011	$((158R - 81R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 11100	$((158R - 84R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 11101	$((158R - 87R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 11110	$((158R - 90R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN6 4-0 = 11111	$((158R - 93R) / 223R) * (VinN7 - VinN13) + VinN13$

Table 5.41: VinN10

Reference voltage	Macro adjustment value	VinN11 formula
VinN11	PKN7 4-0 = 00000	$(123R / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 00001	$((123R - 3R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 00010	$((123R - 6R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 00011	$((123R - 9R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 00100	$((123R - 12R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 00101	$((123R - 15R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 00110	$((123R - 18R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 00111	$((123R - 21R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 01000	$((123R - 24R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 01001	$((123R - 27R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 01010	$((123R - 30R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 01011	$((123R - 33R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 01100	$((123R - 36R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 01101	$((123R - 39R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 01110	$((123R - 42R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 01111	$((123R - 45R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 10000	$((123R - 48R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 10001	$((123R - 51R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 10010	$((123R - 54R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 10011	$((123R - 57R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 10100	$((123R - 60R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 10101	$((123R - 63R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 10110	$((123R - 66R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 10111	$((123R - 69R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 11000	$((123R - 72R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 11001	$((123R - 75R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 11010	$((123R - 78R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 11011	$((123R - 81R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 11100	$((123R - 84R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 11101	$((123R - 87R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 11110	$((123R - 90R) / 223R) * (VinN7 - VinN13) + VinN13$
	PKN7 4-0 = 11111	$((123R - 93R) / 223R) * (VinN7 - VinN13) + VinN13$

Table 5.42: VinN11

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- P.90-  
October 2013

Reference voltage	Macro adjustment value	VinN12 formula
VinN12	PKN8 4-0 = 00000	(96R / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00001	((96R - 3R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00010	((96R - 6R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00011	((96R - 9R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00100	((96R - 12R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00101	((96R - 15R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00110	((96R - 18R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 00111	((96R - 21R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01000	((96R - 24R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01001	((96R - 27R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01010	((96R - 30R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01011	((96R - 33R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01100	((96R - 36R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01101	((96R - 39R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01110	((96R - 42R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 01111	((96R - 45R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10000	((96R - 48R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10001	((96R - 51R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10010	((96R - 54R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10011	((96R - 57R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10100	((96R - 60R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10101	((96R - 63R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10110	((96R - 66R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 10111	((96R - 69R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11000	((96R - 72R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11001	((96R - 75R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11010	((96R - 78R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11011	((96R - 81R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11100	((96R - 84R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11101	((96R - 87R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11110	((96R - 90R) / 223R) * (VinN7 - VinN13) + VinN13
	PKN8 4-0 = 11111	((96R - 93R) / 223R) * (VinN7 - VinN13) + VinN13

Table 5.43: VinN12

Reference voltage	Macro adjustment value	VinN14 formula
VinN14	PKN9 4-0 = 00000	(47R / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00001	((47R - 1R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00010	((47R - 2R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00011	((47R - 3R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00100	((47R - 4R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00101	((47R - 5R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00110	((47R - 6R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 00111	((47R - 7R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01000	((47R - 8R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01001	((47R - 9R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01010	((47R - 10R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01011	((47R - 11R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01100	((47R - 12R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01101	((47R - 13R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01110	((47R - 14R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 01111	((47R - 15R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10000	((47R - 16R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10001	((47R - 17R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10010	((47R - 18R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10011	((47R - 19R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10100	((47R - 20R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10101	((47R - 21R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10110	((47R - 22R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 10111	((47R - 23R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11000	((47R - 24R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11001	((47R - 25R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11010	((47R - 26R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11011	((47R - 27R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11100	((47R - 28R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11101	((47R - 29R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11110	((47R - 30R) / 48R) * (VinN13 - VinN18) + VinN18
	PKN9 4-0 = 11111	((47R - 31R) / 48R) * (VinN13 - VinN18) + VinN18

Table 5.44: VinN14

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Reference voltage	Macro adjustment value	VinN15 formula
VinN15	PKN10 4-0 = 00000	$(47R / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 00001	$((47R - 1R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 00010	$((47R - 2R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 00011	$((47R - 3R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 00100	$((47R - 4R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 00101	$((47R - 5R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 00110	$((47R - 6R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 00111	$((47R - 7R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 01000	$((47R - 8R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 01001	$((47R - 9R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 01010	$((47R - 10R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 01011	$((47R - 11R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 01100	$((47R - 12R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 01101	$((47R - 13R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 01110	$((47R - 14R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 01111	$((47R - 15R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 10000	$((47R - 16R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 10001	$((47R - 17R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 10010	$((47R - 18R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 10011	$((47R - 19R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 10100	$((47R - 20R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 10101	$((47R - 21R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 10110	$((47R - 22R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 10111	$((47R - 23R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 11000	$((47R - 24R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 11001	$((47R - 25R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 11010	$((47R - 26R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 11011	$((47R - 27R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 11100	$((47R - 28R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 11101	$((47R - 29R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 11110	$((47R - 30R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN10 4-0 = 11111	$((47R - 31R) / 48R) * (VinN13 - VinN18) + VinN18$

Table 5.45: VinN15

Reference voltage	Macro adjustment value	VinN16 formula
VinN16	PKN11 4-0 = 00000	$(39R / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 00001	$((39R - 1R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 00010	$((39R - 2R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 00011	$((39R - 3R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 00100	$((39R - 4R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 00101	$((39R - 5R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 00110	$((39R - 6R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 00111	$((39R - 7R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 01000	$((39R - 8R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 01001	$((39R - 9R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 01010	$((39R - 10R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 01011	$((39R - 11R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 01100	$((39R - 12R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 01101	$((39R - 13R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 01110	$((39R - 14R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 01111	$((39R - 15R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 10000	$((39R - 16R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 10001	$((39R - 17R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 10010	$((39R - 18R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 10011	$((39R - 19R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 10100	$((39R - 20R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 10101	$((39R - 21R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 10110	$((39R - 22R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 10111	$((39R - 23R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 11000	$((39R - 24R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 11001	$((39R - 25R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 11010	$((39R - 26R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 11011	$((39R - 27R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 11100	$((39R - 28R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 11101	$((39R - 29R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 11110	$((39R - 30R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN11 4-0 = 11111	$((39R - 31R) / 48R) * (VinN13 - VinN18) + VinN18$

Table 5.46: VinN16

Reference voltage	Macro adjustment value	VinN13 formula
VinN17	PKN12 4-0 = 00000	$(32R / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 00001	$((32R - 1R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 00010	$((32R - 2R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 00011	$((32R - 3R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 00100	$((32R - 4R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 00101	$((32R - 5R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 00110	$((32R - 6R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 00111	$((32R - 7R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 01000	$((32R - 8R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 01001	$((32R - 9R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 01010	$((32R - 10R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 01011	$((32R - 11R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 01100	$((32R - 12R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 01101	$((32R - 13R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 01110	$((32R - 14R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 01111	$((32R - 15R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 10000	$((32R - 16R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 10001	$((32R - 17R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 10010	$((32R - 18R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 10011	$((32R - 19R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 10100	$((32R - 20R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 10101	$((32R - 21R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 10110	$((32R - 22R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 10111	$((32R - 23R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 11000	$((32R - 24R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 11001	$((32R - 25R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 11010	$((32R - 26R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 11011	$((32R - 27R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 11100	$((32R - 28R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 11101	$((32R - 29R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 11110	$((32R - 30R) / 48R) * (VinN13 - VinN18) + VinN18$
	PKN12 4-0 = 11111	$((32R - 31R) / 48R) * (VinN13 - VinN18) + VinN18$

Table 5.47: VinN17

Grayscale voltage	Formula
V0	$\text{VinP/N0}$
V1	$\text{VinP/N0} - (\text{VinP/N0} - \text{VinP/N1}) * (4\text{R}/16\text{R})$
V2	$\text{VinP/N0} - (\text{VinP/N0} - \text{VinP/N1}) * (8\text{R}/16\text{R})$
V3	$\text{VinP/N0} - (\text{VinP/N0} - \text{VinP/N1}) * (12\text{R}/16\text{R})$
V4	$\text{VinP/N1}$
V5	$\text{VinP/N1} - (\text{VinP/N1} - \text{VinP/N2}) * (4\text{R}/16\text{R})$
V6	$\text{VinP/N1} - (\text{VinP/N1} - \text{VinP/N2}) * (8\text{R}/16\text{R})$
V7	$\text{VinP/N1} - (\text{VinP/N1} - \text{VinP/N2}) * (12\text{R}/16\text{R})$
V8	$\text{VinP/N2}$
V9	$\text{VinP/N2} - (\text{VinP/N2} - \text{VinP/N3}) * (4\text{R}/16\text{R})$
V10	$\text{VinP/N2} - (\text{VinP/N2} - \text{VinP/N3}) * (8\text{R}/16\text{R})$
V11	$\text{VinP/N2} - (\text{VinP/N2} - \text{VinP/N3}) * (12\text{R}/16\text{R})$
V12	$\text{VinP/N3}$
V13	$\text{VinP/N3} - (\text{VinP/N3} - \text{VinP/N4}) * (1.5\text{R}/12\text{R})$
V14	$\text{VinP/N3} - (\text{VinP/N3} - \text{VinP/N4}) * (3\text{R}/12\text{R})$
V15	$\text{VinP/N3} - (\text{VinP/N3} - \text{VinP/N4}) * (4.5\text{R}/12\text{R})$
V16	$\text{VinP/N3} - (\text{VinP/N3} - \text{VinP/N4}) * (6\text{R}/12\text{R})$
V17	$\text{VinP/N3} - (\text{VinP/N3} - \text{VinP/N4}) * (7.5\text{R}/12\text{R})$
V18	$\text{VinP/N3} - (\text{VinP/N3} - \text{VinP/N4}) * (9\text{R}/12\text{R})$
V19	$\text{VinP/N3} - (\text{VinP/N3} - \text{VinP/N4}) * (10.5\text{R}/12\text{R})$
V20	$\text{VinP/N4}$
V21	$\text{VinP/N4} - (\text{VinP/N4} - \text{VinP/N5}) * (1.5\text{R}/12\text{R})$
V22	$\text{VinP/N4} - (\text{VinP/N4} - \text{VinP/N5}) * (3\text{R}/12\text{R})$
V23	$\text{VinP/N4} - (\text{VinP/N4} - \text{VinP/N5}) * (4.5\text{R}/12\text{R})$
V24	$\text{VinP/N4} - (\text{VinP/N4} - \text{VinP/N5}) * (6\text{R}/12\text{R})$
V25	$\text{VinP/N4} - (\text{VinP/N4} - \text{VinP/N5}) * (7.5\text{R}/12\text{R})$
V26	$\text{VinP/N4} - (\text{VinP/N4} - \text{VinP/N5}) * (9\text{R}/12\text{R})$
V27	$\text{VinP/N4} - (\text{VinP/N4} - \text{VinP/N5}) * (10.5\text{R}/12\text{R})$
V28	$\text{VinP/N5}$
V29	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (1.5\text{R}/18\text{R})$
V30	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (3\text{R}/18\text{R})$
V31	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (4.5\text{R}/18\text{R})$
V32	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (6\text{R}/18\text{R})$
V33	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (7.5\text{R}/18\text{R})$
V34	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (9\text{R}/18\text{R})$
V35	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (10.5\text{R}/18\text{R})$
V36	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (12\text{R}/18\text{R})$
V37	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (13.5\text{R}/18\text{R})$
V38	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (15\text{R}/18\text{R})$
V39	$\text{VinP/N5} - (\text{VinP/N5} - \text{VinP/N6}) * (16.5\text{R}/18\text{R})$
V40	$\text{VinP/N6}$
V41	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (1.5\text{R}/18\text{R})$
V42	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (3\text{R}/18\text{R})$
V43	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (4.5\text{R}/18\text{R})$

Grayscale voltage	Formula
V44	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (6\text{R}/18\text{R})$
V45	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (7.5\text{R}/18\text{R})$
V46	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (9\text{R}/18\text{R})$
V47	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (10.5\text{R}/18\text{R})$
V48	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (12\text{R}/18\text{R})$
V49	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (13.5\text{R}/18\text{R})$
V50	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (15\text{R}/18\text{R})$
V51	$\text{VinP/N6} - (\text{VinP/N6} - \text{VinP/N7}) * (16.5\text{R}/18\text{R})$
V52	$\text{VinP/N7}$
V53	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (1.6\text{R}/38.4\text{R})$
V54	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (3.2\text{R}/38.4\text{R})$
V55	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (4.8\text{R}/38.4\text{R})$
V56	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (6.4\text{R}/38.4\text{R})$
V57	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (8\text{R}/38.4\text{R})$
V58	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (9.6\text{R}/38.4\text{R})$
V59	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (11.2\text{R}/38.4\text{R})$
V60	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (12.8\text{R}/38.4\text{R})$
V61	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (14.4\text{R}/38.4\text{R})$
V62	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (16\text{R}/38.4\text{R})$
V63	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (17.6\text{R}/38.4\text{R})$
V64	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (19.2\text{R}/38.4\text{R})$
V65	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (20.8\text{R}/38.4\text{R})$
V66	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (22.4\text{R}/38.4\text{R})$
V67	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (24\text{R}/38.4\text{R})$
V68	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (25.6\text{R}/38.4\text{R})$
V69	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (27.2\text{R}/38.4\text{R})$
V70	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (28.8\text{R}/38.4\text{R})$
V71	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (30.4\text{R}/38.4\text{R})$
V72	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (32\text{R}/38.4\text{R})$
V73	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (33.6\text{R}/38.4\text{R})$
V74	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (35.2\text{R}/38.4\text{R})$
V75	$\text{VinP/N7} - (\text{VinP/N7} - \text{VinP/N8}) * (36.8\text{R}/38.4\text{R})$
V76	$\text{VinP/N8}$
V77	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (1.6\text{R}/38.4\text{R})$
V78	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (3.2\text{R}/38.4\text{R})$
V79	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (4.8\text{R}/38.4\text{R})$
V80	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (6.4\text{R}/38.4\text{R})$
V81	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (8\text{R}/38.4\text{R})$
V82	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (9.6\text{R}/38.4\text{R})$
V83	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (11.2\text{R}/38.4\text{R})$
V84	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (12.8\text{R}/38.4\text{R})$
V85	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (14.4\text{R}/38.4\text{R})$
V86	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (16\text{R}/38.4\text{R})$
V87	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (17.6\text{R}/38.4\text{R})$

Grayscale voltage	Formula
V88	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (19.2\text{R}/38.4\text{R})$
V89	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (20.8\text{R}/38.4\text{R})$
V90	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (22.4\text{R}/38.4\text{R})$
V91	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (24\text{R}/38.4\text{R})$
V92	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (25.6\text{R}/38.4\text{R})$
V93	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (27.2\text{R}/38.4\text{R})$
V94	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (28.8\text{R}/38.4\text{R})$
V95	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (30.4\text{R}/38.4\text{R})$
V96	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (32\text{R}/38.4\text{R})$
V97	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (33.6\text{R}/38.4\text{R})$
V98	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (35.2\text{R}/38.4\text{R})$
V99	$\text{VinP/N8} - (\text{VinP/N8} - \text{VinP/N9}) * (36.8\text{R}/38.4\text{R})$
V100	$\text{VinP/N9}$
V101	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (1.6\text{R}/51.2\text{R})$
V102	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (3.2\text{R}/51.2\text{R})$
V103	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (4.8\text{R}/51.2\text{R})$
V104	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (6.4\text{R}/51.2\text{R})$
V105	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (8\text{R}/51.2\text{R})$
V106	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (9.6\text{R}/51.2\text{R})$
V107	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (11.2\text{R}/51.2\text{R})$
V108	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (12.8\text{R}/51.2\text{R})$
V109	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (14.4\text{R}/51.2\text{R})$
V110	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (16\text{R}/51.2\text{R})$
V111	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (17.6\text{R}/51.2\text{R})$
V112	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (19.2\text{R}/51.2\text{R})$
V113	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (20.8\text{R}/51.2\text{R})$
V114	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (22.4\text{R}/51.2\text{R})$
V115	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (24\text{R}/51.2\text{R})$
V116	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (25.6\text{R}/51.2\text{R})$
V117	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (27.2\text{R}/51.2\text{R})$
V118	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (28.8\text{R}/51.2\text{R})$
V119	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (30.4\text{R}/51.2\text{R})$
V120	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (32\text{R}/51.2\text{R})$
V121	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (33.6\text{R}/51.2\text{R})$
V122	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (35.2\text{R}/51.2\text{R})$
V123	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (36.8\text{R}/51.2\text{R})$
V124	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (38.4\text{R}/51.2\text{R})$
V125	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (40\text{R}/51.2\text{R})$
V126	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (41.6\text{R}/51.2\text{R})$
V127	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (43.2\text{R}/51.2\text{R})$
V128	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (44.8\text{R}/51.2\text{R})$
V129	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (46.4\text{R}/51.2\text{R})$
V130	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (48\text{R}/51.2\text{R})$
V131	$\text{VinP/N9} - (\text{VinP/N9} - \text{VinP/N10}) * (49.6\text{R}/51.2\text{R})$

Grayscale voltage	Formula
V132	$\text{VinP/N10}$
V133	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (1.6\text{R}/38.4\text{R})$
V134	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (3.2\text{R}/38.4\text{R})$
V135	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (4.8\text{R}/38.4\text{R})$
V136	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (6.4\text{R}/38.4\text{R})$
V137	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (8\text{R}/38.4\text{R})$
V138	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (9.6\text{R}/38.4\text{R})$
V139	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (11.2\text{R}/38.4\text{R})$
V140	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (12.8\text{R}/38.4\text{R})$
V141	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (14.4\text{R}/38.4\text{R})$
V142	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (16\text{R}/38.4\text{R})$
V143	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (17.6\text{R}/38.4\text{R})$
V144	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (19.2\text{R}/38.4\text{R})$
V145	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (20.8\text{R}/38.4\text{R})$
V146	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (22.4\text{R}/38.4\text{R})$
V147	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (24\text{R}/38.4\text{R})$
V148	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (25.6\text{R}/38.4\text{R})$
V149	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (27.2\text{R}/38.4\text{R})$
V150	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (28.8\text{R}/38.4\text{R})$
V151	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (30.4\text{R}/38.4\text{R})$
V152	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (32\text{R}/38.4\text{R})$
V153	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (33.6\text{R}/38.4\text{R})$
V154	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (35.2\text{R}/38.4\text{R})$
V155	$\text{VinP/N10} - (\text{VinP/N10} - \text{VinP/N11}) * (36.8\text{R}/38.4\text{R})$
V156	$\text{VinP/N11}$
V157	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (1.6\text{R}/38.4\text{R})$
V158	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (3.2\text{R}/38.4\text{R})$
V159	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (4.8\text{R}/38.4\text{R})$
V160	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (6.4\text{R}/38.4\text{R})$
V161	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (8\text{R}/38.4\text{R})$
V162	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (9.6\text{R}/38.4\text{R})$
V163	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (11.2\text{R}/38.4\text{R})$
V164	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (12.8\text{R}/38.4\text{R})$
V165	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (14.4\text{R}/38.4\text{R})$
V166	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (16\text{R}/38.4\text{R})$
V167	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (17.6\text{R}/38.4\text{R})$
V168	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (19.2\text{R}/38.4\text{R})$
V169	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (20.8\text{R}/38.4\text{R})$
V170	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (22.4\text{R}/38.4\text{R})$
V171	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (24\text{R}/38.4\text{R})$
V172	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (25.6\text{R}/38.4\text{R})$
V173	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (27.2\text{R}/38.4\text{R})$
V174	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (28.8\text{R}/38.4\text{R})$
V175	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (30.4\text{R}/38.4\text{R})$

Grayscale voltage	Formula	Grayscale voltage	Formula
V176	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (32R/38.4R)$	V216	$\text{VinP/N14}$
V177	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (33.6R/38.4R)$	V217	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (1.5R/18R)$
V178	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (35.2R/38.4R)$	V218	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (3R/18R)$
V179	$\text{VinP/N11} - (\text{VinP/N11} - \text{VinP/N12}) * (36.8R/38.4R)$	V219	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (4.5R/18R)$
V180	$\text{VinP/N12}$	V220	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (6R/18R)$
V181	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (1.6R/38.4R)$	V221	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (7.5R/18R)$
V182	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (3.2R/38.4R)$	V222	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (9R/18R)$
V183	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (4.8R/38.4R)$	V223	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (10.5R/18R)$
V184	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (6.4R/38.4R)$	V224	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (12R/18R)$
V185	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (8R/38.4R)$	V225	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (13.5R/18R)$
V186	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (9.6R/38.4R)$	V226	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (15R/18R)$
V187	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (11.2R/38.4R)$	V227	$\text{VinP/N14} - (\text{VinP/N14} - \text{VinP/N15}) * (16.5R/18R)$
V188	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (12.8R/38.4R)$	V228	$\text{VinP/N15}$
V189	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (14.4R/38.4R)$	V229	$\text{VinP/N15} - (\text{VinP/N15} - \text{VinP/N16}) * (1.5R/12R)$
V190	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (16R/38.4R)$	V230	$\text{VinP/N15} - (\text{VinP/N15} - \text{VinP/N16}) * (3R/12R)$
V191	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (17.6R/38.4R)$	V231	$\text{VinP/N15} - (\text{VinP/N15} - \text{VinP/N16}) * (4.5R/12R)$
V192	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (19.2R/38.4R)$	V232	$\text{VinP/N15} - (\text{VinP/N15} - \text{VinP/N16}) * (6R/12R)$
V193	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (20.8R/38.4R)$	V233	$\text{VinP/N15} - (\text{VinP/N15} - \text{VinP/N16}) * (7.5R/12R)$
V194	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (22.4R/38.4R)$	V234	$\text{VinP/N15} - (\text{VinP/N15} - \text{VinP/N16}) * (9R/12R)$
V195	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (24R/38.4R)$	V235	$\text{VinP/N15} - (\text{VinP/N15} - \text{VinP/N16}) * (10.5R/12R)$
V196	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (25.6R/38.4R)$	V236	$\text{VinP/N16}$
V197	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (27.2R/38.4R)$	V237	$\text{VinP/N16} - (\text{VinP/N16} - \text{VinP/N17}) * (1.5R/10.5R)$
V198	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (28.8R/38.4R)$	V238	$\text{VinP/N16} - (\text{VinP/N16} - \text{VinP/N17}) * (3R/10.5R)$
V199	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (30.4R/38.4R)$	V239	$\text{VinP/N16} - (\text{VinP/N16} - \text{VinP/N17}) * (4.5R/10.5R)$
V200	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (32R/38.4R)$	V240	$\text{VinP/N16} - (\text{VinP/N16} - \text{VinP/N17}) * (6R/10.5R)$
V201	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (33.6R/38.4R)$	V241	$\text{VinP/N16} - (\text{VinP/N16} - \text{VinP/N17}) * (7.5R/10.5R)$
V202	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (35.2R/38.4R)$	V242	$\text{VinP/N16} - (\text{VinP/N16} - \text{VinP/N17}) * (9R/10.5R)$
V203	$\text{VinP/N12} - (\text{VinP/N12} - \text{VinP/N13}) * (36.8R/38.4R)$	V243	$\text{VinP/N17}$
V204	$\text{VinP/N13}$	V244	$\text{VinP/N17} - (\text{VinP/N17} - \text{VinP/N18}) * (4R/16R)$
V205	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (1.5R/18R)$	V245	$\text{VinP/N17} - (\text{VinP/N17} - \text{VinP/N18}) * (8R/16R)$
V206	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (3R/18R)$	V246	$\text{VinP/N17} - (\text{VinP/N17} - \text{VinP/N18}) * (12R/16R)$
V207	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (4.5R/18R)$	V247	$\text{VinP/N18}$
V208	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (6R/18R)$	V248	$\text{VinP/N18} - (\text{VinP/N18} - \text{VinP/N19}) * (4R/16R)$
V209	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (7.5R/18R)$	V249	$\text{VinP/N18} - (\text{VinP/N18} - \text{VinP/N19}) * (8R/16R)$
V210	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (9R/18R)$	V250	$\text{VinP/N18} - (\text{VinP/N18} - \text{VinP/N19}) * (12R/16R)$
V211	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (10.5R/18R)$	V251	$\text{VinP/N19}$
V212	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (12R/18R)$	V252	$\text{VinP/N19} - (\text{VinP/N19} - \text{VinP/N20}) * (4R/16R)$
V213	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (13.5R/18R)$	V253	$\text{VinP/N19} - (\text{VinP/N19} - \text{VinP/N20}) * (8R/16R)$
V214	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (15R/18R)$	V254	$\text{VinP/N19} - (\text{VinP/N19} - \text{VinP/N20}) * (12R/16R)$
V215	$\text{VinP/N13} - (\text{VinP/N13} - \text{VinP/N14}) * (16.5R/18R)$	V255	$\text{VinP/N20}$

Table 5.48: Voltage calculation formula of 256-grayscale voltage (positive/negative polarity)

## 5.8 Characteristics of I/O

### 5.8.1 Output or bi-directional (I/O) pins

Output or bi-directional pins	After power on	After hardware reset	After software reset
TE	Low	Low	Low
TE1	Low	Low	Low
SDO	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
CABC_PWM_OUT	Low	Low	Low

Table 5.49: Characteristics of output or bi-directional (I/O) pins

### 5.8.2 Input pins

Input pins	During power on process	After power on	After hardware reset	After software reset	During power off process
RESX	Input invalid	Input valid	Input valid	Input valid	Input invalid
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
DCX	Input invalid	Input valid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB[23:0], SDI	Input invalid	Input valid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input valid	Input invalid
PCLK	Input invalid	Input valid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input valid	Input invalid
OSC	Input invalid	Input valid	Input valid	Input valid	Input invalid
TEST[2:0]	Low	Low	Low	Low	Low
FRM	Low	Low	Low	Low	Low
PCCS[1:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_CP/N	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_D1P/N	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_D2P/N	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_D3P/N	Input invalid	Input valid	Input valid	Input valid	Input invalid

Table 5.50: Characteristics of input pins

## 5.9 GIP control singal

HX8394-D is a single chip solution for a WXGA GIP (Gate In Panel) type TFT LCD display. There are many GIP/ASG type TFT panels that correspond to different GIP timing. Therefore, the GIP setting must be setup to the correct GIP/ASG timing for the normal display. The GIP timing adjustment is related to register 0xD5h SETGIP.

The GIP control signals (CGOUT1\_L/R ~ CGOUT22\_L/R) are for panel used. The assignment of each panel type is specified on the application note. Regarding the GIP/ASG timing, please refer to HX8394-D application note.

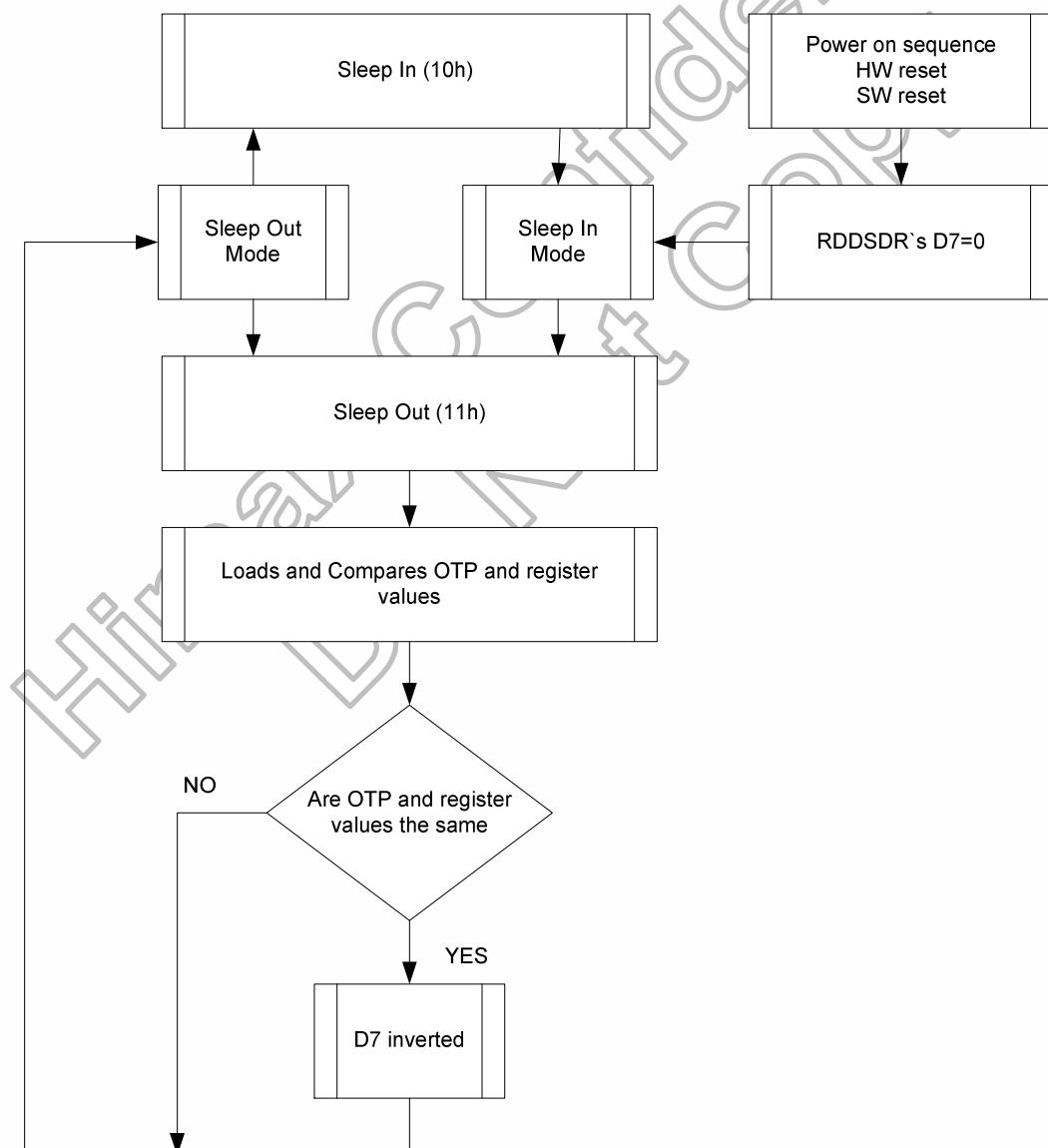
Himax Confidential  
DO NOT COPY

## 5.10 Sleep Out –command and self-diagnostic functions of the display module

### 5.10.1 Register loading detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1).

The flow chart for this internal function is following:

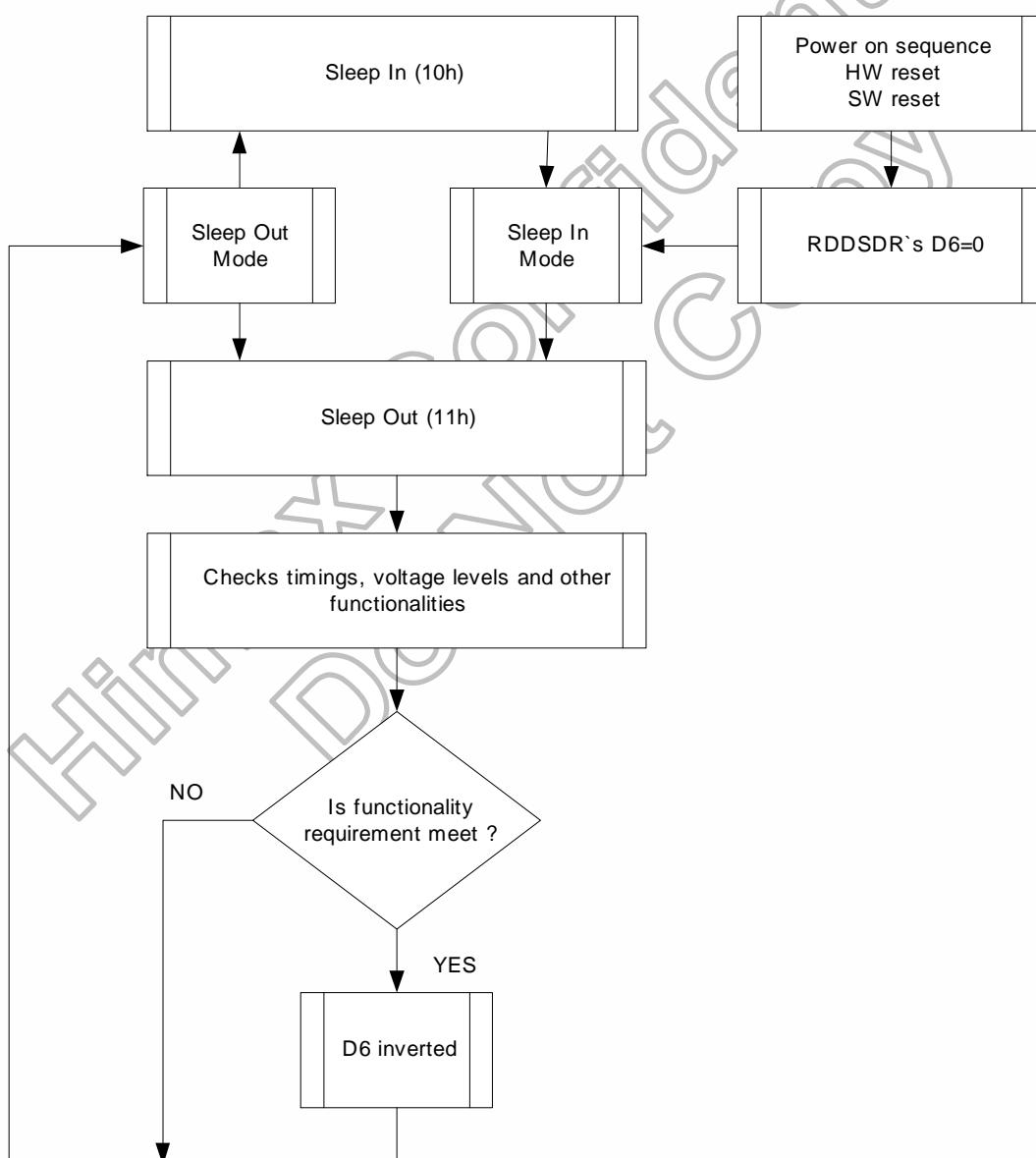


**Figure 5.17: Sleep out flow chart–command and self-diagnostic functions**

### 5.10.2 Functionality detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (=the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.



**Note:** There is needed 120m sec. after Sleep Out –command, when there is changing from Sleep In-mode to Sleep Out –mode, before there is possible to check if Customer's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out –mode.

**Figure 5.18: Sleep out flow chart internal function detection**

## 5.11 Power on/off sequence

The Power supply On/Off, Sleep In/Out and Display On/Off sequence is illustrated below.

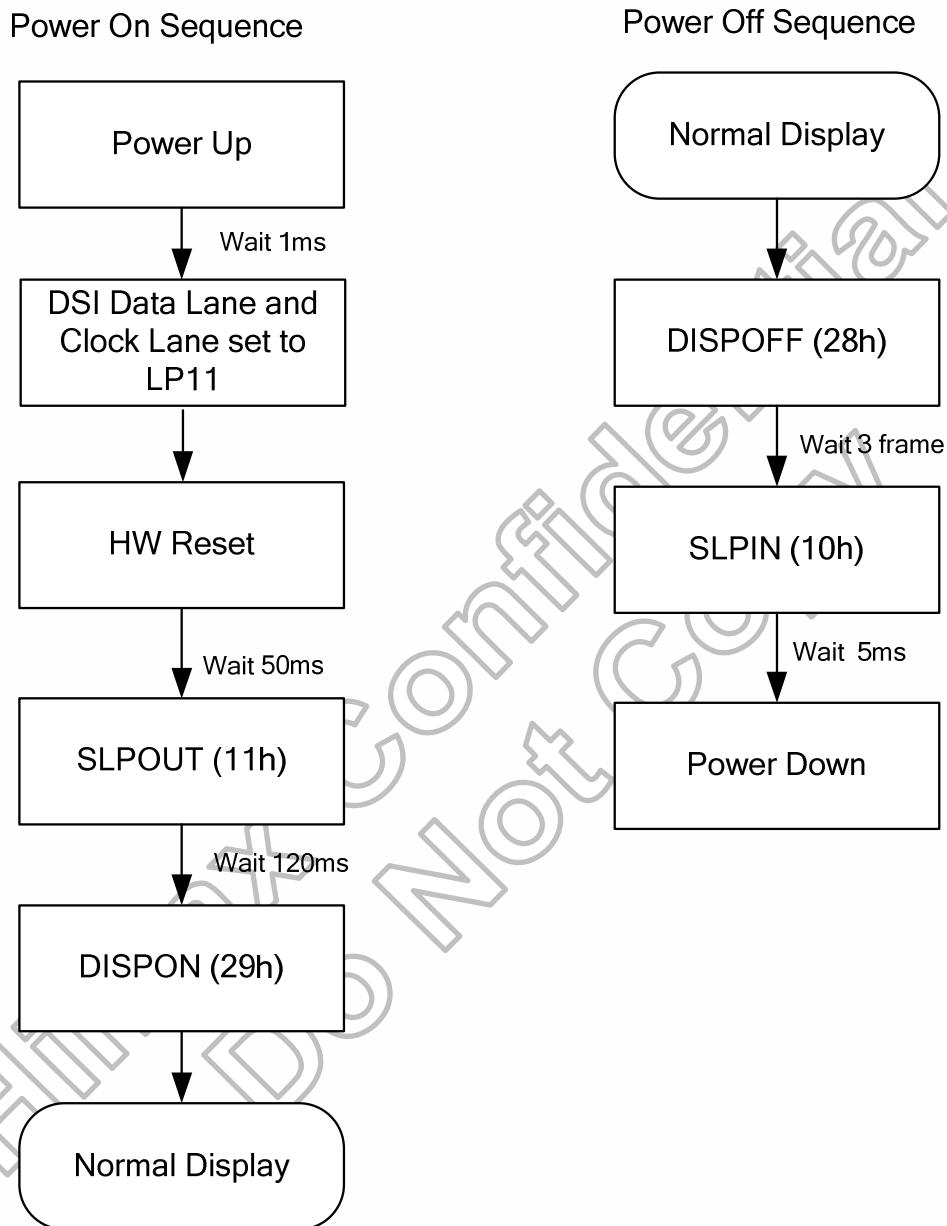
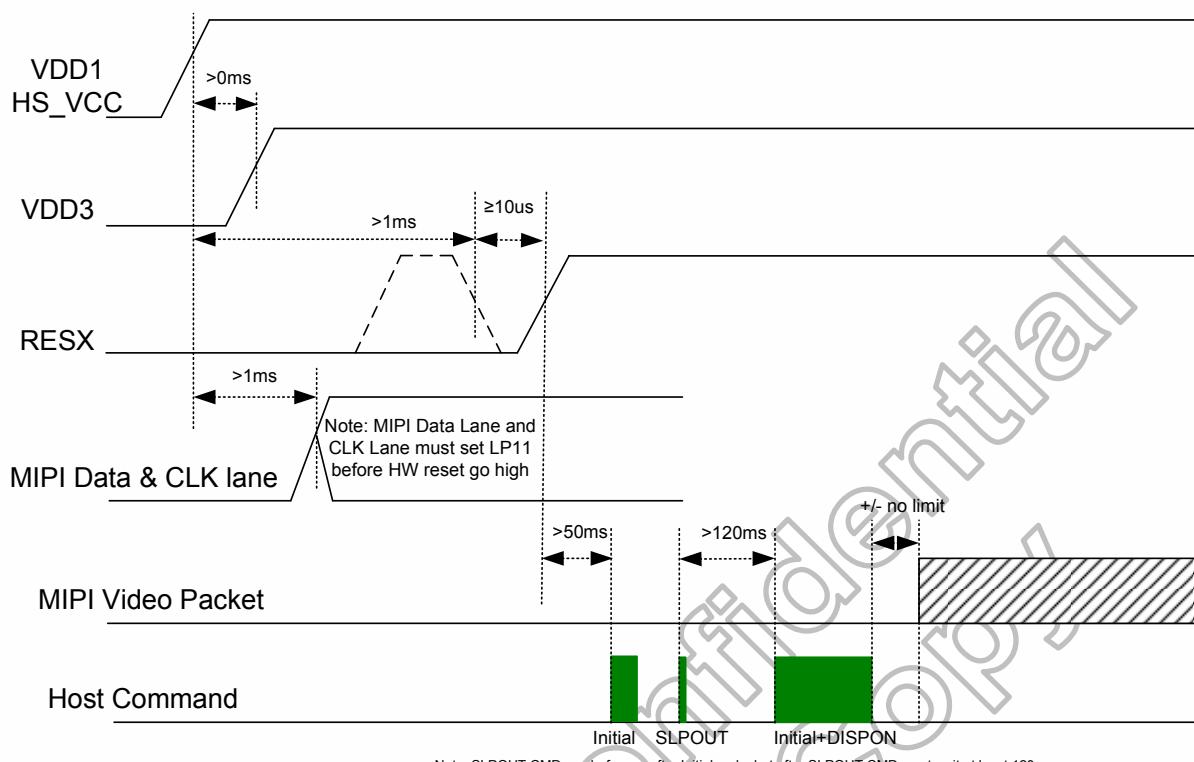
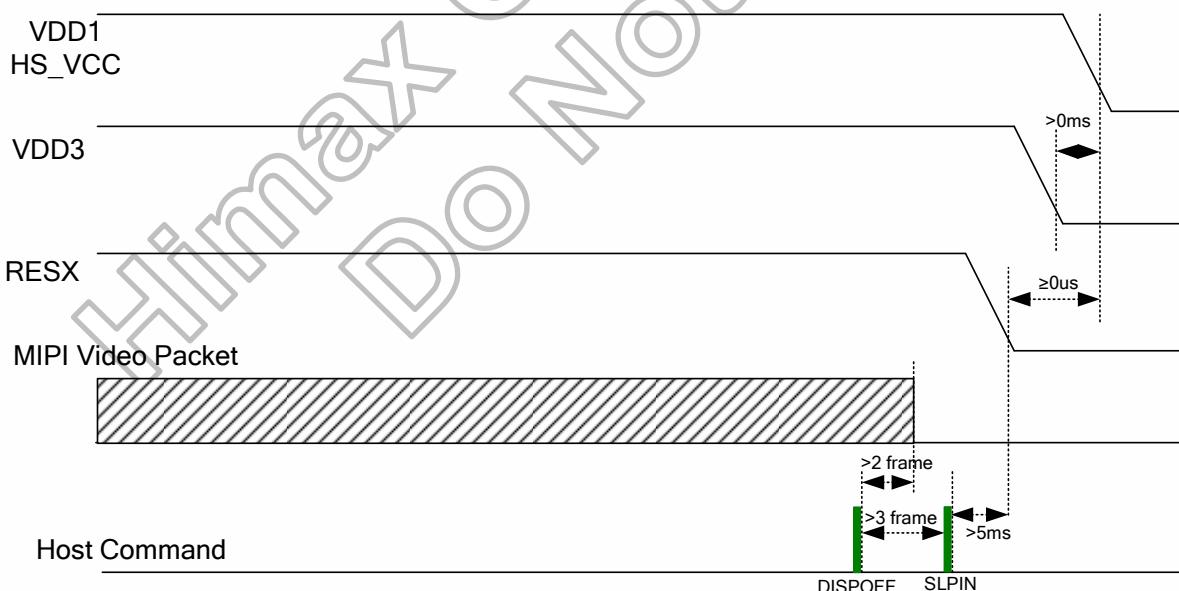


Figure 5.19: Power on/off sequence

### 5.11.1 VDD1/VDD3 input power sequence (PCCS[1:0] = "01", "10")

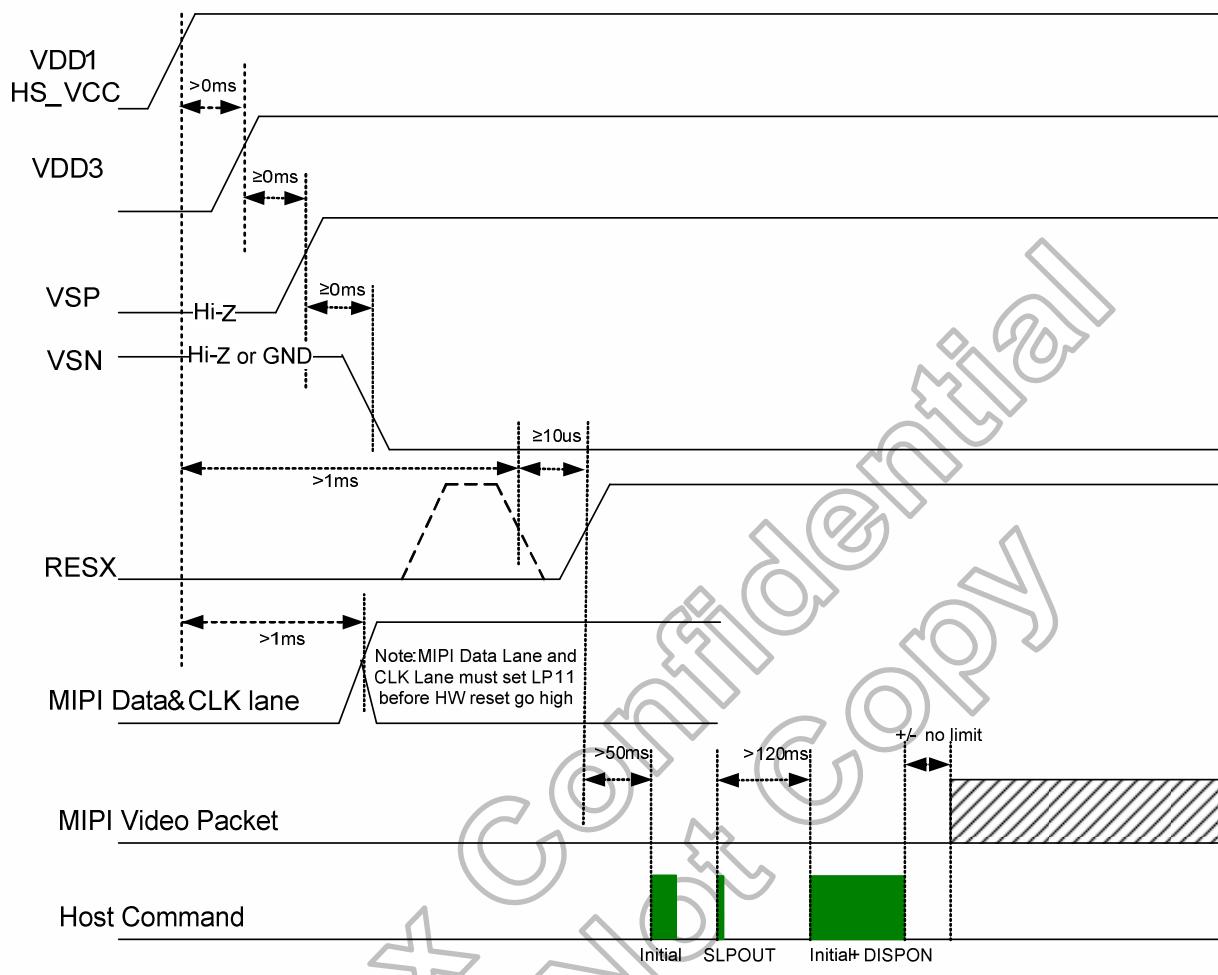


**Figure 5.20: VDD3/VDD1 input power on sequence**

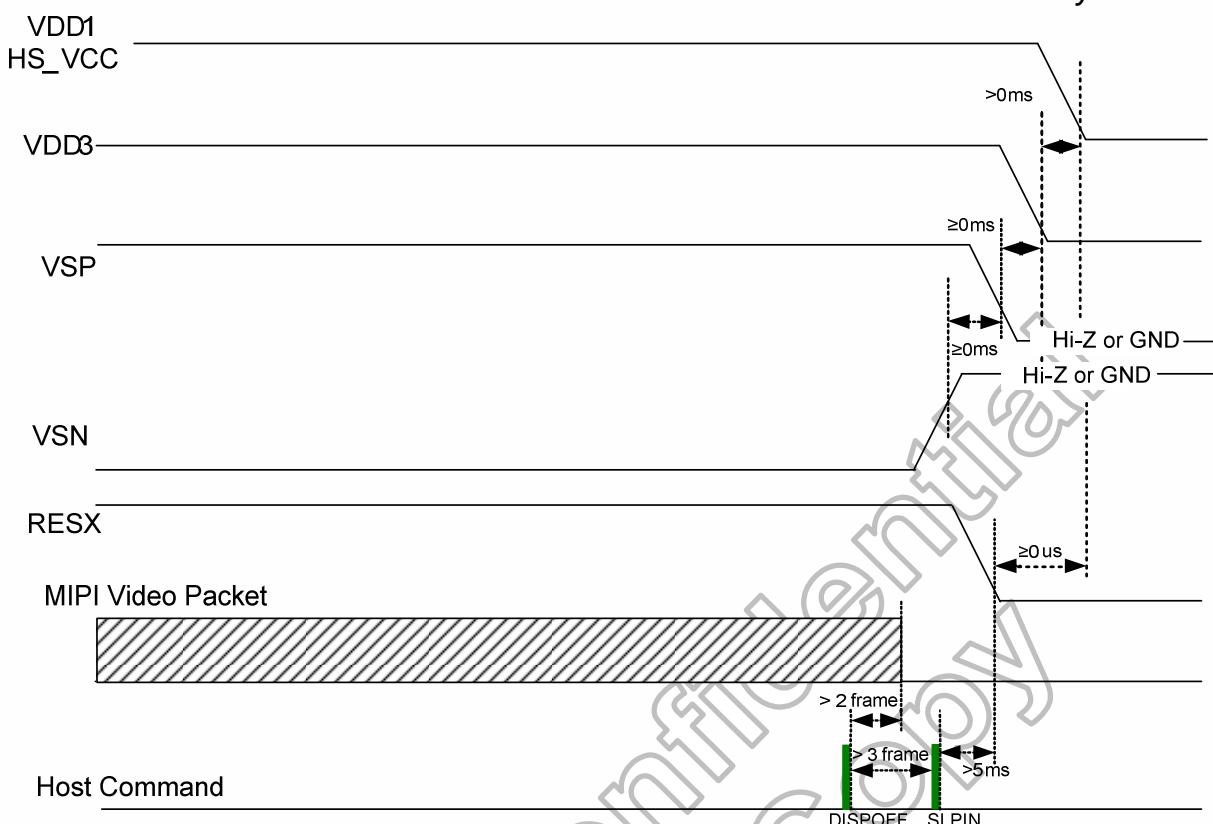


**Figure 5.21: VDD1/VDD3 input power off sequence**

### 5.11.2 VDD1/VDD3/VSP/VSN input power sequence (PCCS[1:0] = "11")



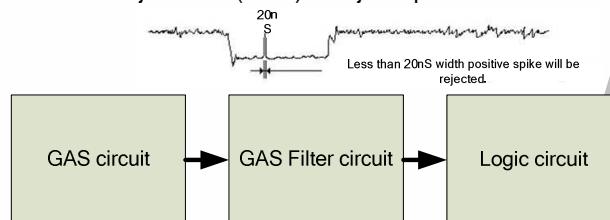
**Figure 5.22: VDD1/VDD3/VSP/VSN input power on sequence**

**Figure 5.23: VDD1/VDD3/VSP/VSN input power off sequence**

## 5.12 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

**Note:** HX8394-D is support the noise reject filter (20ns) to reject spike or noise.



### 5.13 Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

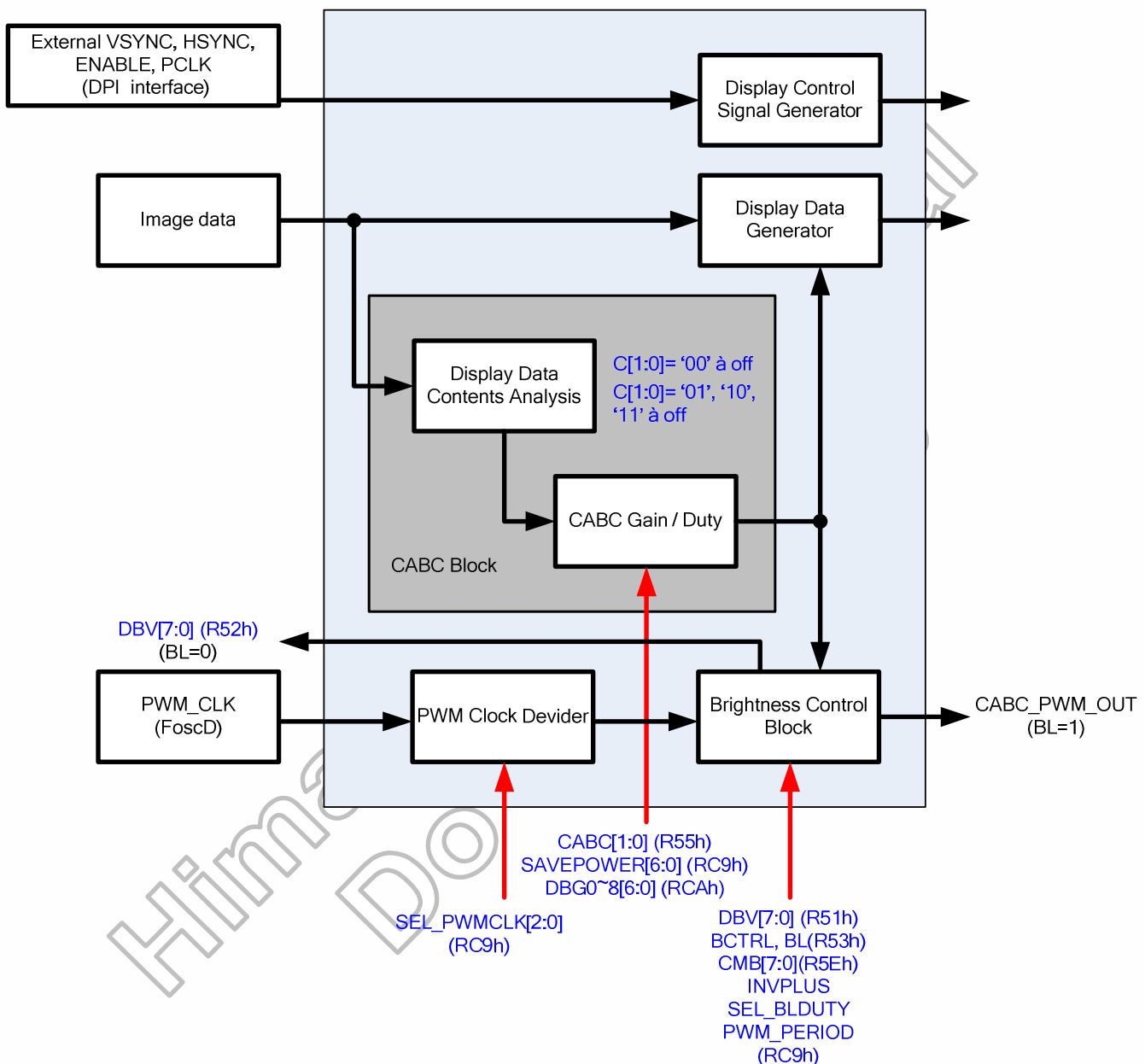
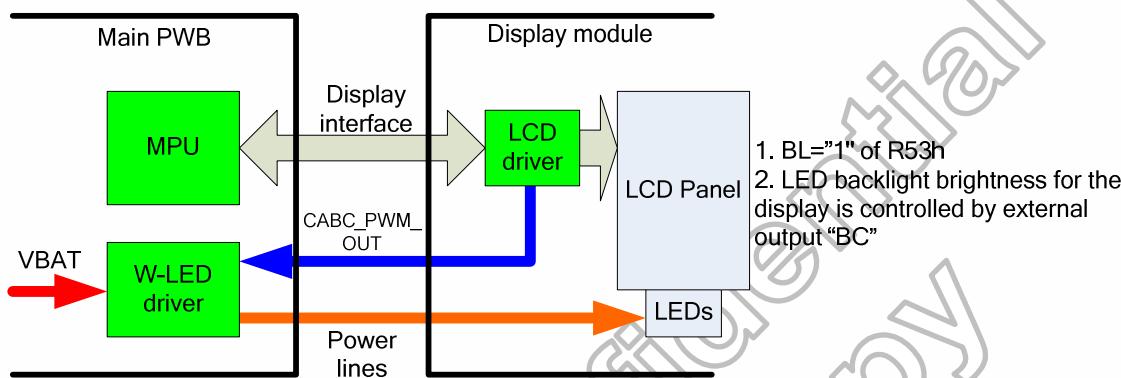


Figure 5.24: CABC block diagram

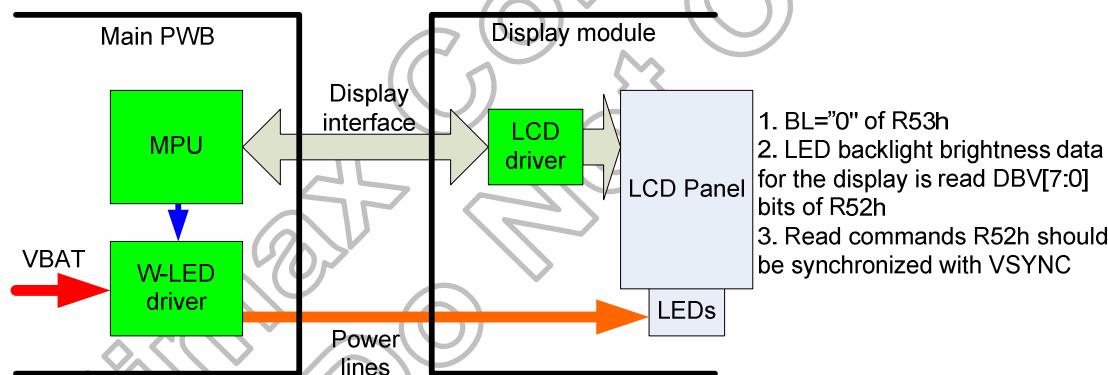
### 5.13.1 Module architectures

HX8394-D can support two module architectures for CABC operation. The BL bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I



- Architecture II



**Figure 5.25: Module architecture**

### 5.13.2 CABC block

There are DBG0~8[6:0] register bits in CABC block to define the “CABC gain”/“CABC duty” table. Every DBGx[6:0] has 33 gain/duty value setting.

After one-frame display data content analysis, LSI will generate one CABC gain / CABC duty value calculated from DBG0~8[6:0] register bits setting (by using interpolated method) for display data generating and for backlight PWM pulse generating.

Please note that the CABC gain / CABC duty value calculated by the LSI is one of the 33 gain/duty value setting in DBGxx[6:0].

Please note that : Duty ( valid level period (LED on) / one complete period)=1/ gain.

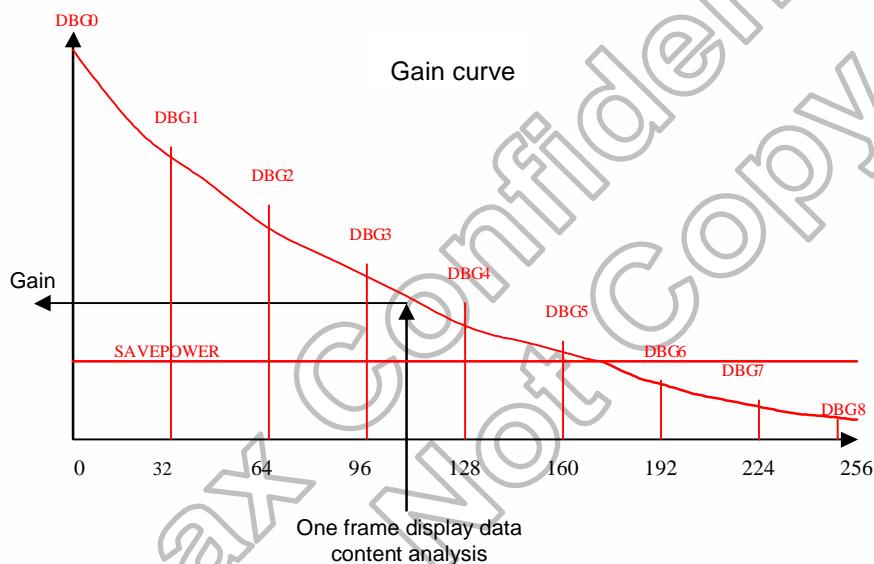


Figure 5.26: CABC gain / CABC duty generation

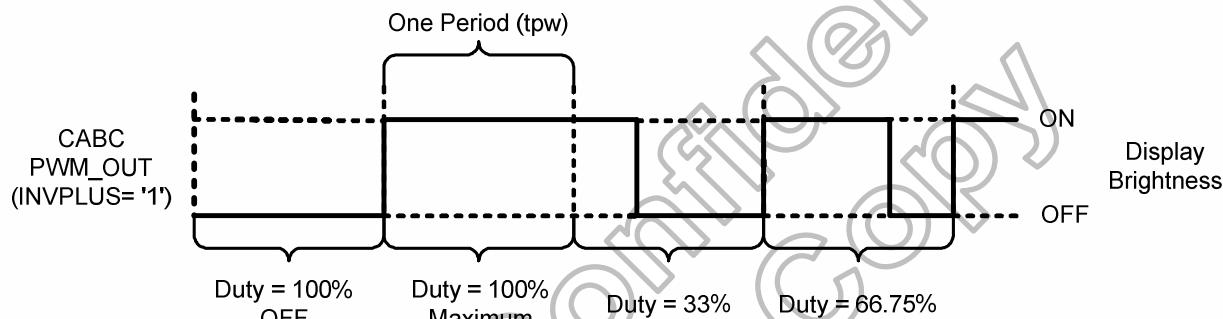
For power saving of backlight module, there are SAVEPOWER[6:0] bits to define the “minimum gain”/ “maximum duty” of CABC block output. If the CABC gain / duty after one-frame display data contents analysis is smaller(gain) / larger(duty) than SAVEPOWER[6:0] bits setting, the CABC block will output CABC gain / duty equal to SAVEPOWER[6:0] and ignore the result of display data contents analysis.

### 5.13.3 Brightness control block

There is an external output signal from brightness block, CABC\_PWM\_OUT, to control the LED driver IC in order to control display brightness.

There are register bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC\_PWM\_OUT duty is calculated as  $(DBV[7:0]) / 255 \times CABC\ duty$  (generated after one-frame display data content analysis).

For ex: CABC\_PWM\_OUT period = 2.95 ms, and DBV[7:0](R51h) = '228<sub>DEC</sub>' and CABC duty is 74%. Then CABC\_PWM\_OUT duty =  $(228) / 255 \times 74.42\% \equiv 66.54\%$ . Correspond to the CABC\_PWM\_OUT period = 2.95 ms, the high-level of CABC\_PWM\_OUT (high effective) = 1.96ms, and the low-level of CABC\_PWM\_OUT = 0.99ms.



**Figure 5.27: CABC\_PWM\_OUT output duty**

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

**Table 5.51: CABC timing table**

**Note:** (1) The signal rise and fall times ( $t_f, t_r$ ) are stipulated to be equal to or less than 15ns.  
(2) The pulse width range by setting CABC related registers is located between 0.0333ms to 8.33ms.

When Architecture II module is used ( $BL=0$ ) with the example below, the CABC\_PWM\_OUT is always output low and the DBV[7:0](R51h) will be read a value as 169<sub>DEC</sub> ( $(169) / 255 \equiv 66.27\%$ ).

#### 5.13.4 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (CMB[7:0] bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL='0' of R53h), CABC minimum brightness setting is ignored. "CMB[7:0], Read CABC minimum brightness (R5Fh)" always read the setting value of "CMB[7:0], Write CABC minimum brightness (R5Eh)"

## 5.14 OTP programming

### 5.14.1 OTP table

OTP_INDEX (HEX)	B7	B6	B5	B4	B3	B2	B1	B0
00					ID1_1[7:0]			
01					ID2_1[7:0]			
02					ID3_1[7:0]			
03					ID4_1[7:0]			
04					ID1_2[7:0]			
05					ID2_2[7:0]			
06					ID3_2[7:0]			
07					ID4_2[7:0]			
08					ID1_3[7:0]			
09					ID2_3[7:0]			
0A					ID3_3[7:0]			
0B					ID4_3[7:0]			
0C	NVALID_ID1	NVALID_ID2	NVALID_ID3	-	-	-	-	-
0D					VCMC_F1[7:0]			
0E					VCMC_B1[7:0]			
0F					VCMC_F2[7:0]			
10					VCMC_B2[7:0]			
11					VCMC_F3[7:0]			
12					VCMC_B3[7:0]			
13	-	-	VCMC_B38	VCMC_F38	VCMC_B28	VCMC_F28	VCMC_B18	VCMC_F18
14	NVALID_VC MC1	NVALID_VC MC2	NVALID_VC MC3	-	-	-	-	-
15	NVALID_PA NEL	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL

Table 5.52: OTP table

## 5.14.2 OTP programming flow

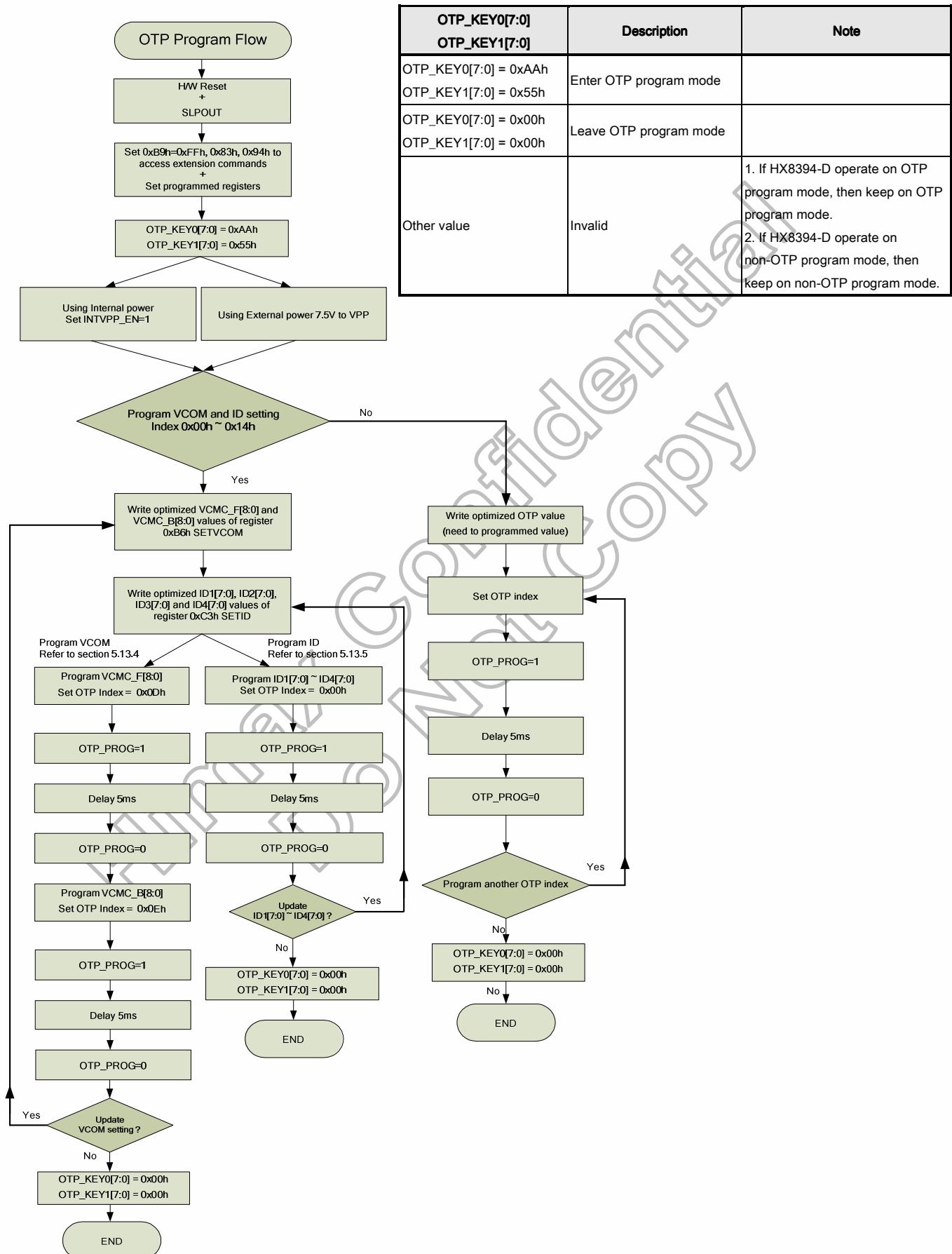


Figure 5.28: OTP programming sequence

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### 5.14.3 Programming sequence

Step	Operation
1	Power on and reset the module.
2	SLPOUT and set 0xB9h = 0xFFh, 0x83h, 0x94h to access the extension commands.
3	Set OTP_KEY0[7:0]=0xAAh and OTP_KEY1[7:0]=0x55h to enter OTP program mode.
4	Set INTVPP_EN=1 for OTP programming state for using internal power mode. Or using the external power 7.5V to VPP.
5	Write optimized values to related registers.
6	Specify OTP_index, please refer to the OTP table.
7	Set OTP_Mask=0x00h, programming the entire bit of one parameter.
8	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.
9	Wait 5 ms ( <b>Note 1</b> )
10	Set OTP_PROG=0, OTP_index programming action done.
11	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (5). Otherwise, set OTP_KEY1[7:0]=0x00h and OTP_KEY1[7:0]=0x00h to leave OTP program mode and power off the module and remove the external power on VPP pin.

**Note:** (1) When do the OTP programming process, it must be added 5ms delay time after setting OTP\_PROG=1.

Table 5.53: OTP programming sequence

### 5.14.4 OTP programming example of VCOM setting VCMC

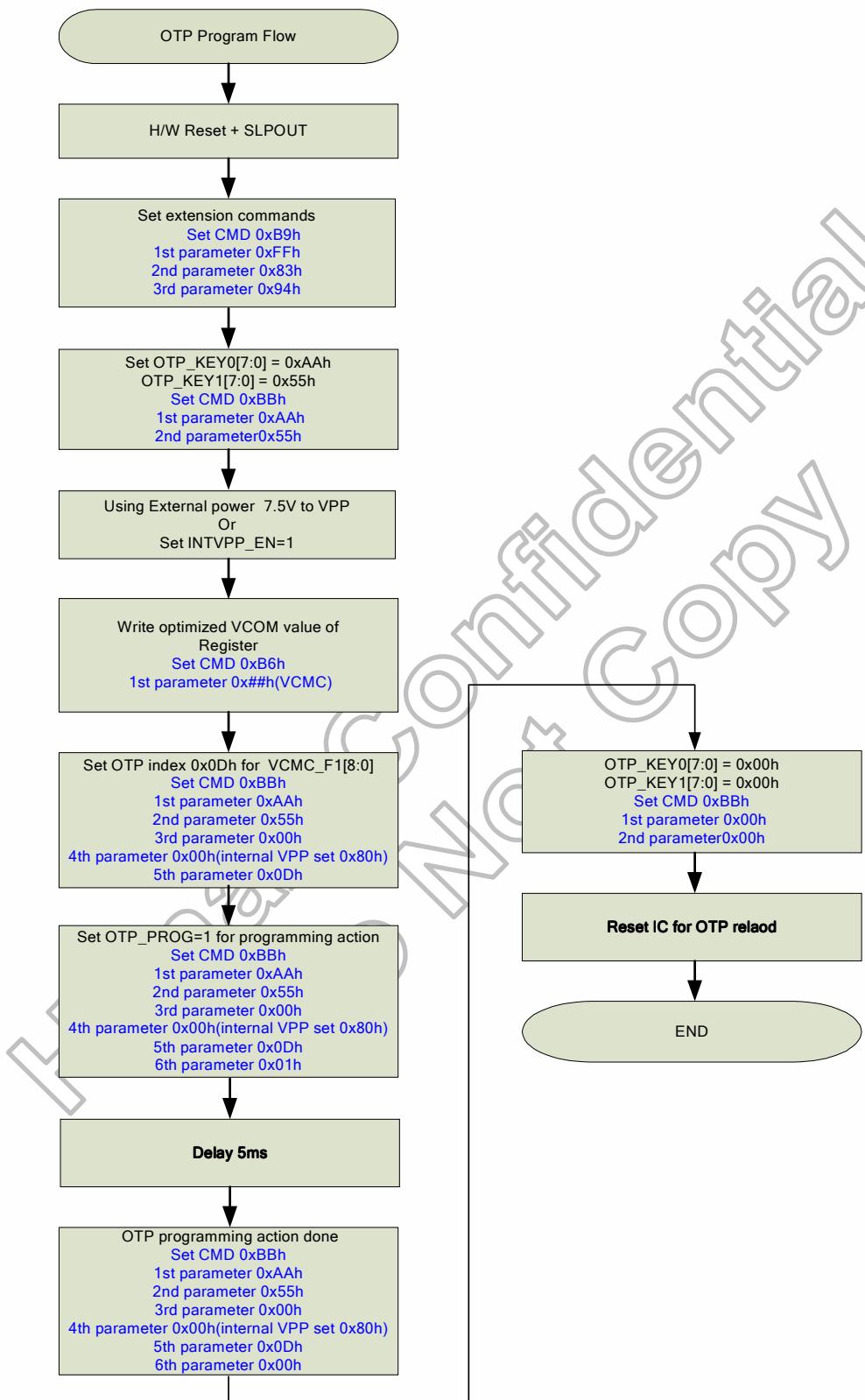


Figure 5.29: OTP programming sequence example 1

### 5.14.5 OTP programming example of ID1, ID2 and ID3

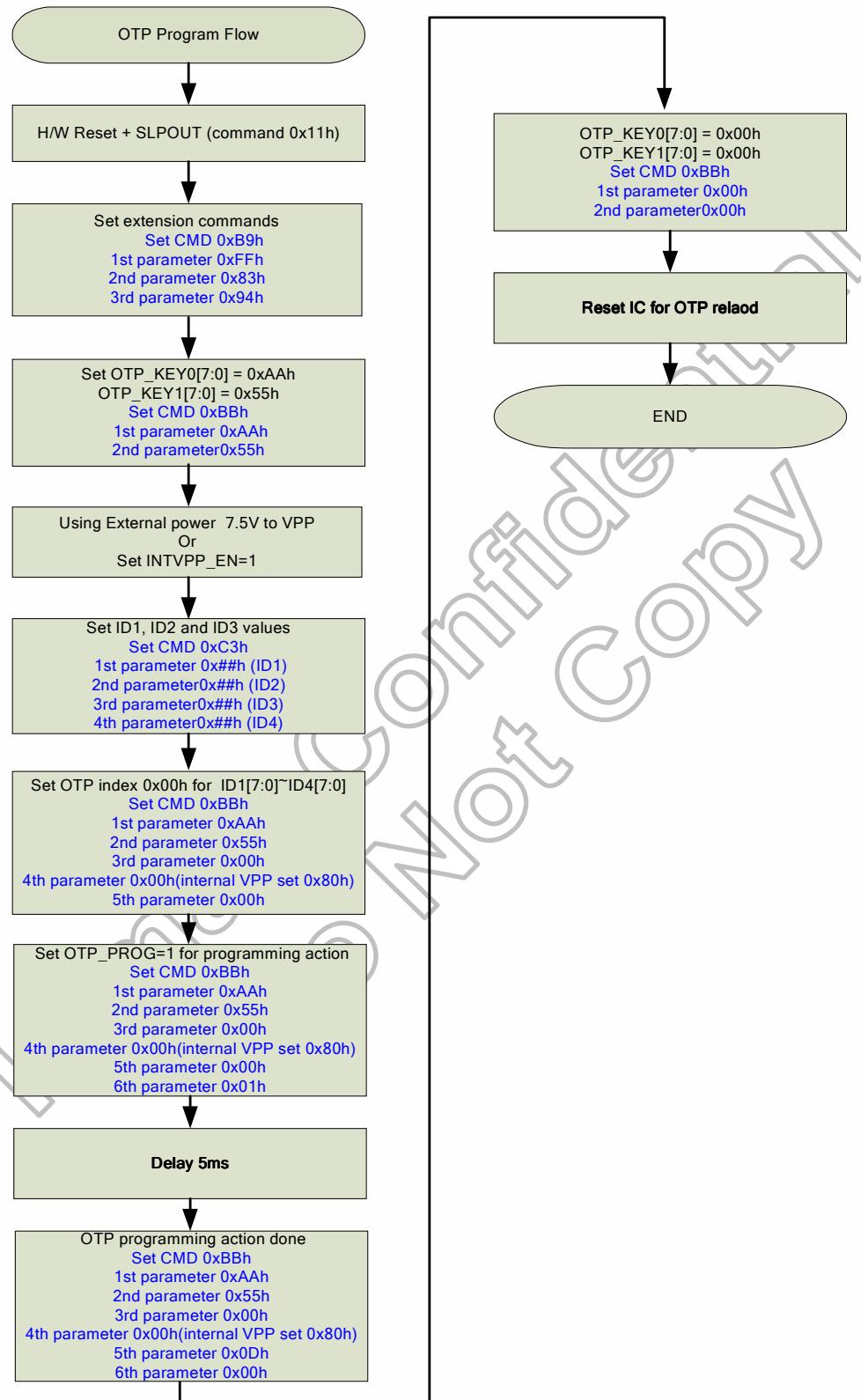


Figure 5.30: OTP programming sequence example 2

### 5.14.6 OTP read example of 0x00h (ID1)

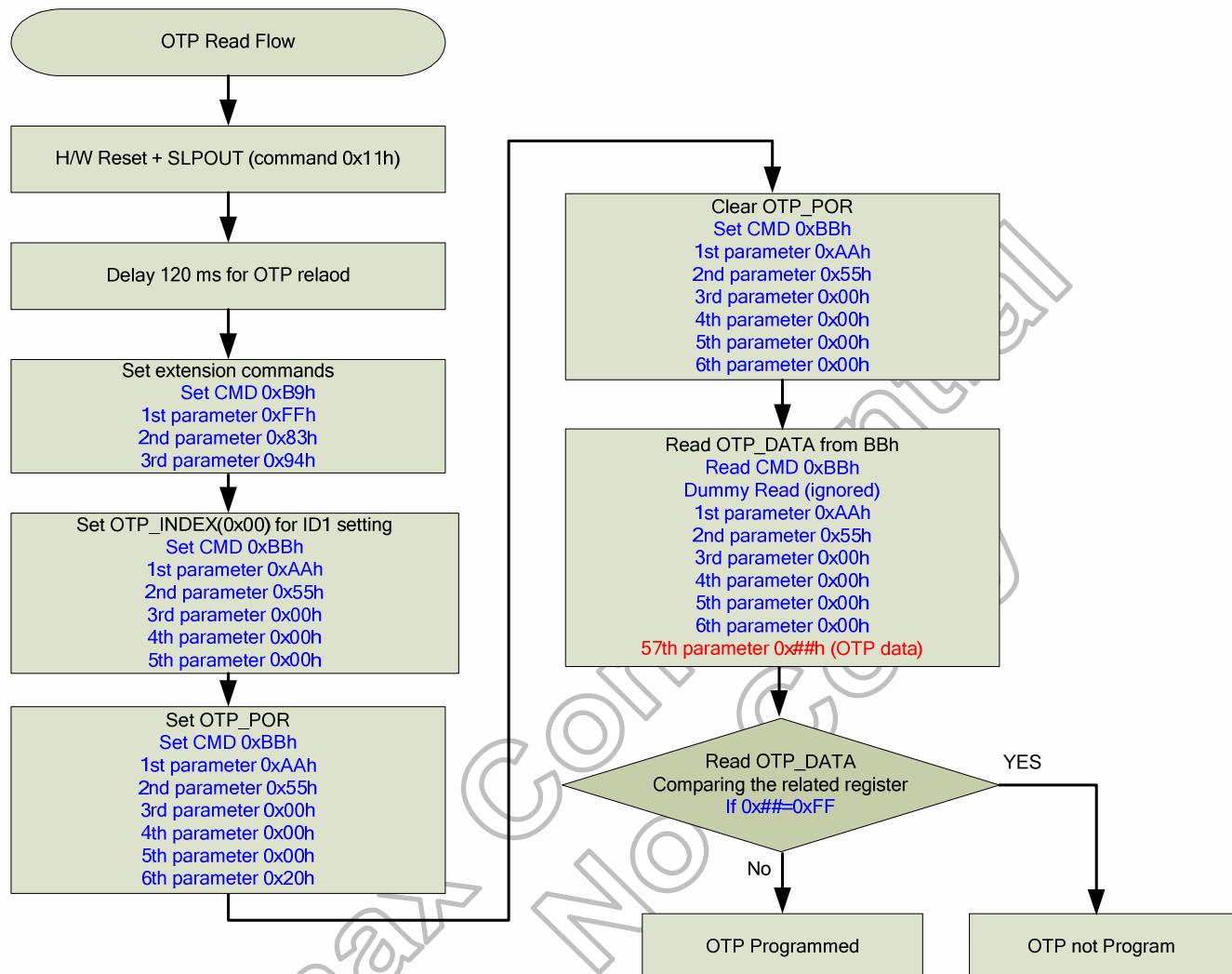
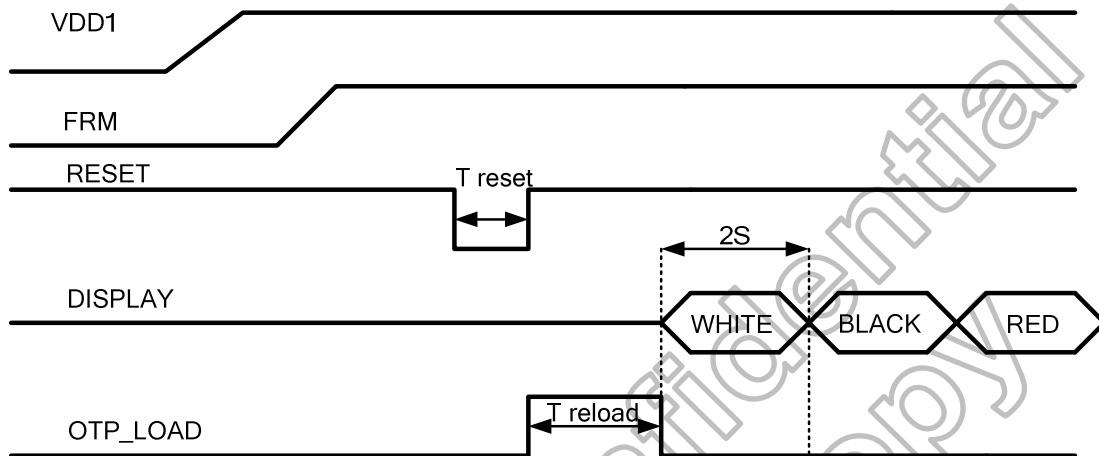


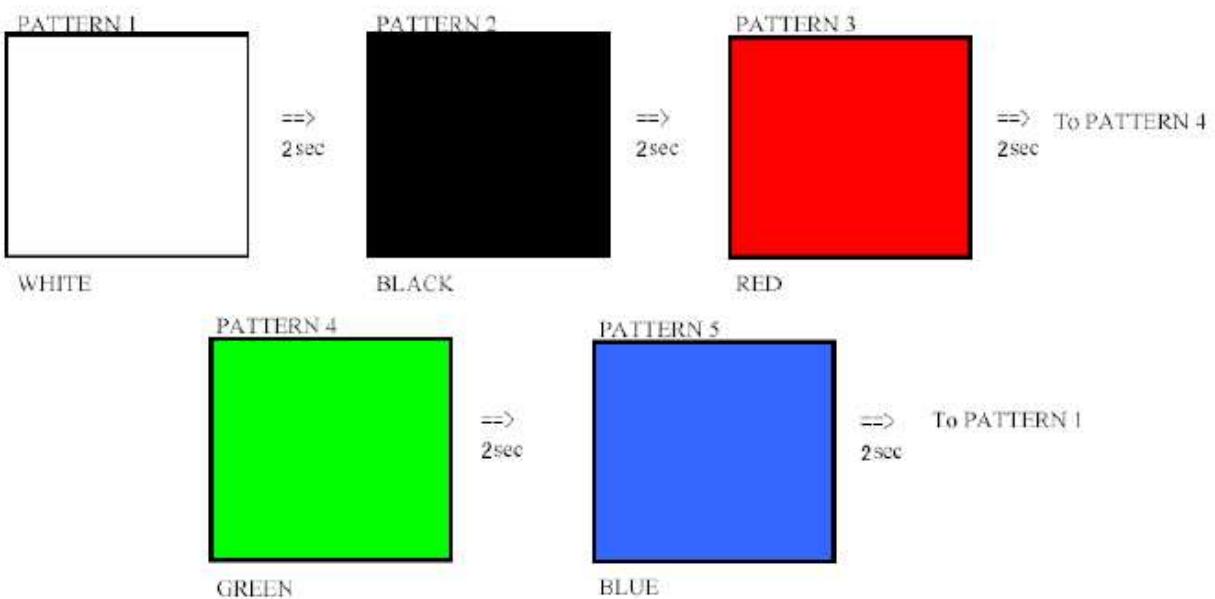
Figure 5.31: OTP read sequence flow of index 0x00h

## 5.15 FRM (Free running mode)

Burn-in of TFT displays consists of driving each module for 10hr at a temperature of 60°C. In order to drive the modules, it requires extra electronics. To reduce the burn-in cost, it is requested that the driver IC will generate the required display image without requiring extra electronics. We term this a free running mode(FRM). For burn-in, it is sufficient that the display is powered up with a plane saturated black or white pattern. The Display pattern sequence and power on sequence is as below Figure.



**Figure 5.32: FRM power on sequence**



**Figure 5.33: Display pattern sequence in FRM**

## 5.16 Temperature sensor

HX8394-D can support the temperature sensor function. This function would that the Driver to change the H\_Temp and L\_Temp mode in different environment. To achieve the low power consumption effect.

User can elasticity to define the temperture upper boundary and lower boundary. And the Driver can auto to change the other power valtage / source drvring. The Tempeture sensor can cover the panel GIP deviation in different environment, Driver can auto to change the GIP Timing.

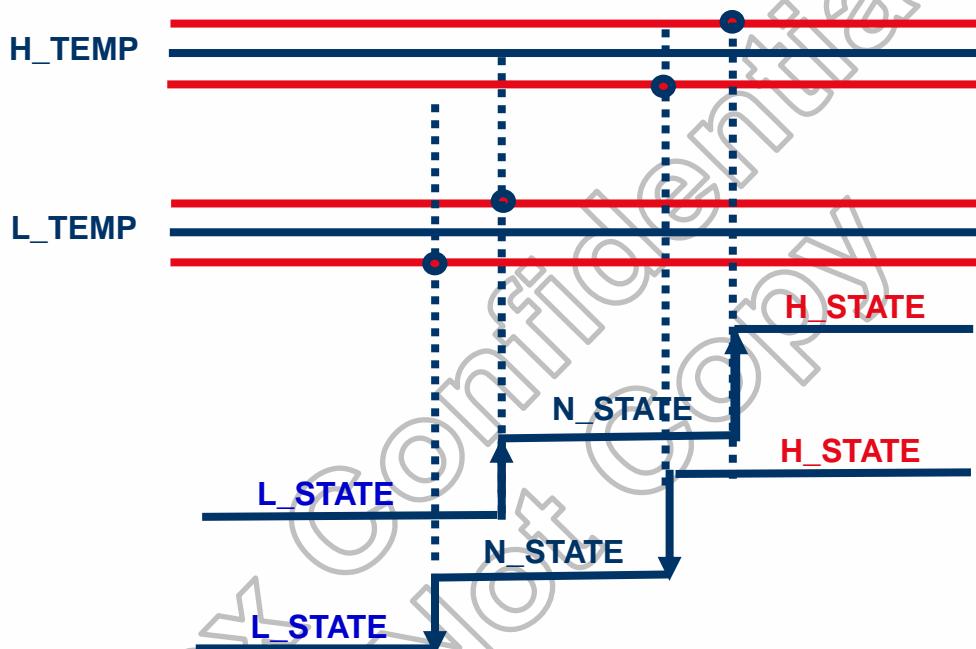


Figure 5.34: Temperture sensor diagram

## 5.17 Command list

### 5.17.1 Standard command

(Hex)	Operation code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	
00	NOP	0	0	0	0	0	0	0	0	0	No Operation	-	
01	SWRESET	0	0	0	0	0	0	0	0	1	Software Reset	-	
04	RDDIDIF	0	0	0	0	0	0	1	0	0	Read Display Identification Information	-	
		1				ID1[7:0]						-	
		1	1			ID2[6:0]						-	
		1				ID3[7:0]						-	
05	RDNUMPE	0	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error	-	
		1				P[7:0]						-	
06	RDRED	0	0	0	0	0	0	1	1	0	Read Red Colour	-	
		1	R7	R6	R5	R4	R3	R2	R1	R0		-	
07	RDGREEN	0	0	0	0	0	0	1	1	1	Read Green Colour	-	
		1	G7	G6	G5	G4	G3	G2	G1	G0		-	
08	RDBLUE	0	0	0	0	0	1	0	0	0	Read Blue Colour	-	
		1	B7	B6	B5	B4	B3	B2	B1	B0		-	
09	RDDST	0	0	0	0	0	1	0	0	1	Read display status	-	
		1				D[31:24]						-	
		1				D[23:16]						-	
		1				D[15:8]						-	
		1				D[7:0]						-	
0A	RDDPM	0	0	0	0	0	1	0	1	0	Read display power mode	-	
		1	0	D6	0	D4	D3	D2	-	-		-	
0B	RDDMADCTL	0	0	0	0	0	1	0	1	1	Read display MADCTL	-	
		1	-	-	-	-	D3	-	D1	D0		-	
0C	RDDCOLMOD	0	0	0	0	0	1	1	0	0	Read display pixel format	-	
		1	-	D6	D5	D4	-	-	-	-		-	
0D	RDDIM	0	0	0	0	0	1	1	0	1	Read display image mode	-	
		1	-	-	D5	D4	D3	D2	D1	D0		-	
0E	RDDSM	0	0	0	0	0	1	1	1	0	Read display signal mode	-	
		1	D7	D6	D5	D4	D3	D2	-	-		-	
0F	RDDSDR	0	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-	
		1	D7	D6	D5	D4	-	-	-	-		-	
10	SLPIN	0	0	0	0	1	0	0	0	0	Sleep In	-	
11	SLPOUT	0	0	0	0	1	0	0	0	1	Sleep Out	-	
13	NORON	0	0	0	0	1	0	0	1	1	Normal display mode on	-	
20	INVOFF	0	0	0	1	0	0	0	0	0	Display inversion off	-	
21	INVON	0	0	0	1	0	0	0	0	1	Display inversion on	-	
22	ALLPOFF	0	0	0	1	0	0	0	1	0	All pixel off (black)	-	
23	ALLPON	0	0	0	1	0	0	0	1	1	All pixel on (white)	-	
26	GAMSET	0	0	0	1	0	0	1	1	0	Gamma set	-	
		1				GC[7:0]						-	
28	DISPOFF	0	0	0	1	0	1	0	0	0	Display off	-	
29	DISPON	0	0	0	1	0	1	0	0	1	Display on	-	
34	TEOFF	0	0	0	1	1	0	1	0	0	Tearing Effect Line OFF	-	
35	TEON	0	0	0	1	1	0	1	0	1	Tearing Effect Line ON	-	
		1	X	X	X	X	X	X	X	M		-	
36	MADCTL	0	0	0	1	1	0	1	1	0	Memory access Control	-	
		1	X	X	X	X	B3	X	B1	B0		-	
38	IDMOFF	0	0	0	1	1	1	0	0	0	Idle mode off	-	
39	IDMON	0	0	0	1	1	1	0	0	1	Idle mode on	-	
3A	COLMOD	0	0	0	1	1	1	0	1	0	-	-	
		1	X	D6	D5	D4	X	X	X	X		-	

(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)			
44	TESL	0	0	1	0	0	0	1	0	0	Tearing Effect Scan Line number	-			
		1			TELINE[15:8](8'b0)										
		1			TELINE[7:0](8'b0)										
45	GETSCAN	0	0	1	0	0	0	1	0	1	Reture the current scanline SLN[15:0]	-			
		1			SLN[15:8]										
		1			SLN[7:0]										
51	WRDISBV	0	0	1	0	1	0	0	0	1	Write Display Brightness	-			
		1			DBV[7:0]										
52	RDDISBV	0	0	1	0	1	0	0	1	0	Read Display Brightness Value	-			
		1			DBV[7:0]										
53	WRCTRLD	0	0	1	0	1	0	0	1	1	Write CTRL Display	-			
		1	X	X	BCT RL	X	DD	BL	X	X		-			
54	RDCTRLD	0	0	1	0	1	0	0	1	1	Read Control Value Display	-			
		1	0	0	BCT RL	0	DD	BL	0	0		-			
55	WRCABC	0	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control	-			
		1	X	X	X	X	X	X	CABC[1:0]			-			
56	RDCABC	0	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content	-			
		1	0	0	0	0	0	0	C1	C0		-			
5E	WRCABCMB	0	0	1	0	1	1	1	1	0	Write CABC minimum brightness	-			
		1			CMB[7:0]										
5F	RDCABCMB	0	0	1	0	1	1	1	1	1	Read CABC minimum brightness	-			
		1			CMB[7:0]										
68	RDABCSDR	0	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	-			
		1	D[7:6]		0	0	0	0	0	0		-			
DA	RDID1	0	1	1	0	1	1	0	1	0	Read ID1	-			
		1			module's manufacturer[7:0]										
DB	RDID2	0	1	1	0	1	1	0	1	1	Read ID2	-			
		1	1		LCD module/driver version [6:0]										
DC	RDID3	0	1	1	0	1	1	1	0	0	Read ID3	-			
		1			LCD module/driver ID[7:0]										
A1	Read_DDB_start	0	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-			
		1	xx	xx	xx	xx	xx	xx	xx	xx		-			
		1	xx	xx	xx	xx	xx	xx	xx	xx		-			
		1	xx	xx	xx	xx	xx	xx	xx	xx		-			
A8	Read_DDB_continue	0	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-			
		1	xx	xx	xx	xx	xx	xx	xx	xx		-			
		1	xx	xx	xx	xx	xx	xx	xx	xx		-			
		1	xx	xx	xx	xx	xx	xx	xx	xx		-			

**Note:** (1) Undefined commands are treated as NOP (00h) command.

(2) B0h to D8h and E0h to FFh are for factory use of display supplier.

### 5.17.2 User define command list table

User define command list is available only set "SETEXC" command.( Note1: \* read only)

(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)			
B0	SETAUTO		1	0	1	1	0	0	0	0				
		1	DISP_BIS_T_EN				-				00			
		2	-	-	-	-	-	-	-	OSC_EN	00			
		3	-	VSN_EN	VSP_EN	VGL_EN	VGH_EN	VCL_EN	VDDDN_H_Z	STB	7D			
		4	-	-	-	-	GON	DTE	D[1:0]		0C			
B1	SETPOWER		1	0	1	1	0	0	0	1				
		1	DSTB	APF_EN	DD_TU	GASVCI_OPT[1:0]		AP[2:0]			64			
		2	HX5187-E_N	INT_VCI		VRHP[4:0]								
		3	-	DT[1:0]		VRHN[4:0]								
		4	FS0[3:0]			FS1[3:0]								
		5	EQ_ON	EQ_MIX	EQ_VCLEN			FS2[3:0]			24			
		6	VCL[2:0]			BTP[4:0]								
		7	CLK_OPT2	CLK_OPT1	CLK_OPT0			BTN[4:0]			F1			
		8	POWMOD[1:0]						VGHS[8]		00			
		9	VGHS[7:0]						DC					
		10	VGLS[7:0]						54					
		11	XDK[2:0]			BTP_INIT[4:0]								
		12	DCS[2]	A_DC[2]				DCDIV[3:0]			80			
		13	DCS[1:0]			DTPS[2:0]			DTNS[2:0]		C0			
		14	A_DC[1:0]			A_DTP[2:0]			A_DTN[2:0]		D2			
		15	-	VGL2_EN				VGL2S[4:0]			10			
B2	SETDISP		1	0	1	1	0	0	1	0				
		1	ZZ_LR	ZZ_EO	NW_PE[2:0]			NW[2:0]			80			
		2	NL[7:0]						64					
		3	BP [7:0]						08					
		4	FP [7:0]						08					
		5	SAP[3:0]			OSC_TUR_BO		RES_SEL[2:0]			22			
		6	RTN[7:0]						1C					
		7	BP_PE [7:0]						08					
		8	FP_PE [7:0]						08					
B3	SETRGBIF		1	0	1	1	0	0	1	1				
		1	-	-	-	DFR	DPL	HSPL	VSPL	EPL	01			
B4	SETCYC		1	0	1	1	0	1	0	0				
		1	GEN_ON[7:0]						00					
		2	GEN_OFF[7:0]						FF					
		3	SPON[7:0]						03					
		4	SPOFF[7:0]						38					
		5	CON[7:0]						05					
		6	COFF[7:0]						36					
		7	CON1[7:0]						05					
		8	COFF1[7:0]						36					
		9	EQON1[7:0]						02					
		10	EQON2[7:0]						70					
		11	SON[7:0]						10					
		12	SOFF[7:0]						70					
		13	SPON_MPU[7:0]						03					
		14	SPOFF_MPU[7:0]						38					
		15	CON_MPU[7:0]						05					
		16	COFF_MPU[7:0]						36					
		17	CON1_MPU[7:0]						05					
		18	COFF1_MPU[7:0]						36					
		19	EQON1_MPU[7:0]						02					
		20	EQON2_MPU[7:0]						70					
		21	SON_MPU[7:0]						10					
		22	SOFF_MPU[7:0]						70					
B6	SETVCOM (OTPx3)		1	0	1	1	0	1	1	0				
		1	VCMC_F[7:0]						46					
		2	VCMC_B[7:0]						46					
		3	VCOM_TIMES[2:0]*						VCMC_B[8]	VCMC_F[8]	E0			
B7	SETTE		1	0	1	1	0	1	1	1	00			
			1	-	-	TE_SEL[1:0]		TEI[3:0]						

(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)	
B9	SETEXTC	2	TEL_SEL[1:0]		TER_SEL[1:0]	-		TEP[10:8]			00	
		3				TEP[7:0]					00	
		1	1	0	1	1	1	0	0	1		
BA	SETMIPI	1			EXTC1[7:0]						00	
		2			EXTC2[7:0]						00	
		3			EXTC3[7:0]						00	
		1	1	0	1	1	1	0	1	0		
BA		1	-		DSISETUP0[6:0]						01	
		2			DSISETUP1[7:0]						83	
		3			DPHYCMD0[7:0]						A0	
		4			DPHYCMD1[7:0]						6D	
		5			DPHYCMD2[7:0]						B2	
		6			DPHYCMD3[7:0]						00	
		7			DPHYCMD4[7:0]						00	
		8			DSICMD0[7:0]						00	
		9			DSICMD1[7:0]						10	
		10			DSICMD2[7:0]						FF	
		11			DSICMD3[7:0]						0F	
		12			DPHYCMD5[7:0]						00	
		13			DSICMD4[7:0]						08	
		14			DSICMD5[7:0]						3D	
		15			DSICMD6[7:0]						06	
		16			DSICMD7[7:0]						53	
		17			DSICMD8[7:0]						0C	
		18	-	DSI_INITR DY	-	-	-	-	-	-	40	
BB	SETOTP	1	0	1	1	1	0	1	1			
		1			OTP_KEY0[7:0]						00/AA	
		2			OTP_KEY1[7:0]						00/55	
		3			OTP_MASK[7:0]						00	
		4	INT_VPPE N						OTP_INDEX[9:8]		00	
		5			OTP_INDEX[7:0]						00	
		6	OTP_LOA D_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PT[1:0]	OTP_PWR SEL	OTP_PRO G		00	
BC	SETVDC	1	0	1	1	1	0	0	0			
		1	-	-	-	-	-	VDC_SEL[2:0]			04	
BD	SET_BANK	1	1	1	1	1	1	0	1			
		1	-	-	-	-	-	-	BANK_INDEX[1:0]		00	
C1	SETDGCLUT	1	1	0	0	0	0	0	0	1		
		Bank_0_1	-	-	-	-	-	-	-	DGC_EN	00	
		Bank_0_2			R_GAMMA0[9:2]						-	
		Bank_0_3			R_GAMMA1[9:2]						-	
		Bank_0_4			R_GAMMA2[9:2]						-	
		Bank_0_5			R_GAMMA3[9:2]						-	
		Bank_0_6			R_GAMMA4[9:2]						-	
		Bank_0_7			R_GAMMA5[9:2]						-	
		Bank_0_8			R_GAMMA6[9:2]						-	
		Bank_0_9			R_GAMMA7[9:2]						-	
		Bank_0_10			R_GAMMA8[9:2]						-	
		Bank_0_11			R_GAMMA9[9:2]						-	
		Bank_0_12			R_GAMMA10[9:2]						-	
		Bank_0_13			R_GAMMA11[9:2]						-	
		Bank_0_14			R_GAMMA12[9:2]						-	
		Bank_0_15			R_GAMMA13[9:2]						-	
		Bank_0_16			R_GAMMA14[9:2]						-	

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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
	Bank_0_17					R_GAMMA15[9:2]					-
	Bank_0_18					R_GAMMA16[9:2]					-
	Bank_0_19					R_GAMMA17[9:2]					-
	Bank_0_20					R_GAMMA18[9:2]					-
	Bank_0_21					R_GAMMA19[9:2]					-
	Bank_0_22					R_GAMMA20[9:2]					-
	Bank_0_23					R_GAMMA21[9:2]					-
	Bank_0_24					R_GAMMA22[9:2]					-
	Bank_0_25					R_GAMMA23[9:2]					-
	Bank_0_26					R_GAMMA24[9:2]					-
	Bank_0_27					R_GAMMA25[9:2]					-
	Bank_0_28					R_GAMMA26[9:2]					-
	Bank_0_29					R_GAMMA27[9:2]					-
	Bank_0_30					R_GAMMA28[9:2]					-
	Bank_0_31					R_GAMMA29[9:2]					-
	Bank_0_32					R_GAMMA30[9:2]					-
	Bank_0_33					R_GAMMA31[9:2]					-
	Bank_0_34					R_GAMMA32[9:2]					-
	Bank_0_35	R_GAMMA0[1:0]		R_GAMMA1[1:0]		R_GAMMA2[1:0]		R_GAMMA3[1:0]			-
	Bank_0_36	R_GAMMA4[1:0]		R_GAMMA5[1:0]		R_GAMMA6[1:0]		R_GAMMA7[1:0]			-
	Bank_0_37	R_GAMMA8[1:0]		R_GAMMA9[1:0]		R_GAMMA10[1:0]		R_GAMMA11[1:0]			-
	Bank_0_38	R_GAMMA12[1:0]		R_GAMMA13[1:0]		R_GAMMA14[1:0]		R_GAMMA15[1:0]			-
	Bank_0_39	R_GAMMA16[1:0]		R_GAMMA17[1:0]		R_GAMMA18[1:0]		R_GAMMA19[1:0]			-
	Bank_0_40	R_GAMMA20[1:0]		R_GAMMA21[1:0]		R_GAMMA22[1:0]		R_GAMMA23[1:0]			-
	Bank_0_41	R_GAMMA24[1:0]		R_GAMMA25[1:0]		R_GAMMA26[1:0]		R_GAMMA27[1:0]			-
	Bank_0_42	R_GAMMA28[1:0]		R_GAMMA29[1:0]		R_GAMMA30[1:0]		R_GAMMA31[1:0]			-
	Bank_0_43	R_GAMMA32[1:0]	-	-	-	-	-	-	-		-
	Bank_1_1					G_GAMMA0[9:2]					-
	Bank_1_2					G_GAMMA1[9:2]					-
	Bank_1_3					G_GAMMA2[9:2]					-
	Bank_1_4					G_GAMMA3[9:2]					-
	Bank_1_5					G_GAMMA4[9:2]					-
	Bank_1_6					G_GAMMA5[9:2]					-
	Bank_1_7					G_GAMMA6[9:2]					-
	Bank_1_8					G_GAMMA7[9:2]					-
	Bank_1_9					G_GAMMA8[9:2]					-
	Bank_1_10					G_GAMMA9[9:2]					-
	Bank_1_11					G_GAMMA10[9:2]					-
	Bank_1_12					G_GAMMA11[9:2]					-
	Bank_1_13					G_GAMMA12[9:2]					-

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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
	Bank_1_14					G_GAMMA13[9:2]					-
	Bank_1_15					G_GAMMA14[9:2]					-
	Bank_1_16					G_GAMMA15[9:2]					-
	Bank_1_17					G_GAMMA16[9:2]					-
	Bank_1_18					G_GAMMA17[9:2]					-
	Bank_1_19					G_GAMMA18[9:2]					-
	Bank_1_20					G_GAMMA19[9:2]					-
	Bank_1_21					G_GAMMA20[9:2]					-
	Bank_1_22					G_GAMMA21[9:2]					-
	Bank_1_23					G_GAMMA22[9:2]					-
	Bank_1_24					G_GAMMA23[9:2]					-
	Bank_1_25					G_GAMMA24[9:2]					-
	Bank_1_26					G_GAMMA25[9:2]					-
	Bank_1_27					G_GAMMA26[9:2]					-
	Bank_1_28					G_GAMMA27[9:2]					-
	Bank_1_29					G_GAMMA28[9:2]					-
	Bank_1_30					G_GAMMA29[9:2]					-
	Bank_1_31					G_GAMMA30[9:2]					-
	Bank_1_32					G_GAMMA31[9:2]					-
	Bank_1_33					G_GAMMA32[9:2]					-
	Bank_1_34	G_GAMMA0[1:0]		G_GAMMA1[1:0]		G_GAMMA2[1:0]		G_GAMMA3[1:0]			-
	Bank_1_35	G_GAMMA4[1:0]		G_GAMMA5[1:0]		G_GAMMA6[1:0]		G_GAMMA7[1:0]			-
	Bank_1_36	G_GAMMA8[1:0]		G_GAMMA9[1:0]		G_GAMMA10[1:0]		G_GAMMA11[1:0]			-
	Bank_1_37	G_GAMMA12[1:0]		G_GAMMA13[1:0]		G_GAMMA14[1:0]		G_GAMMA15[1:0]			-
	Bank_1_38	G_GAMMA16[1:0]		G_GAMMA17[1:0]		G_GAMMA18[1:0]		G_GAMMA19[1:0]			-
	Bank_1_39	G_GAMMA20[1:0]		G_GAMMA21[1:0]		G_GAMMA22[1:0]		G_GAMMA23[1:0]			-
	Bank_1_40	G_GAMMA24[1:0]		G_GAMMA25[1:0]		G_GAMMA26[1:0]		G_GAMMA27[1:0]			-
	Bank_1_41	G_GAMMA28[1:0]		G_GAMMA29[1:0]		G_GAMMA30[1:0]		G_GAMMA31[1:0]			-
	Bank_1_42	G_GAMMA32[1:0]									-
	Bank_2_1					B_GAMMA0[9:2]					-
	Bank_2_2					B_GAMMA1[9:2]					-
	Bank_2_3					B_GAMMA2[9:2]					-
	Bank_2_4					B_GAMMA3[9:2]					-
	Bank_2_5					B_GAMMA4[9:2]					-
	Bank_2_6					B_GAMMA5[9:2]					-
	Bank_2_7					B_GAMMA6[9:2]					-
	Bank_2_8					B_GAMMA7[9:2]					-
	Bank_2_9					B_GAMMA8[9:2]					-
	Bank_2_10					B_GAMMA9[9:2]					-
	Bank_2_11					B_GAMMA10[9:2]					-

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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
	Bank_2_12					B_GAMMA11[9:2]					-
	Bank_2_13					B_GAMMA12[9:2]					-
	Bank_2_14					B_GAMMA13[9:2]					-
	Bank_2_15					B_GAMMA14[9:2]					-
	Bank_2_16					B_GAMMA15[9:2]					-
	Bank_2_17					B_GAMMA16[9:2]					-
	Bank_2_18					B_GAMMA17[9:2]					-
	Bank_2_19					B_GAMMA18[9:2]					-
	Bank_2_20					B_GAMMA19[9:2]					-
	Bank_2_21					B_GAMMA20[9:2]					-
	Bank_2_22					B_GAMMA21[9:2]					-
	Bank_2_23					B_GAMMA22[9:2]					-
	Bank_2_24					B_GAMMA23[9:2]					-
	Bank_2_25					B_GAMMA24[9:2]					-
	Bank_2_26					B_GAMMA25[9:2]					-
	Bank_2_27					B_GAMMA26[9:2]					-
	Bank_2_28					B_GAMMA27[9:2]					-
	Bank_2_29					B_GAMMA28[9:2]					-
	Bank_2_30					B_GAMMA29[9:2]					-
	Bank_2_31					B_GAMMA30[9:2]					-
	Bank_2_32					B_GAMMA31[9:2]					-
	Bank_2_33					B_GAMMA32[9:2]					-
	Bank_2_34		B_GAMMA0[1:0]		B_GAMMA1[1:0]		B_GAMMA2[1:0]		B_GAMMA3[1:0]		-
	Bank_2_35		B_GAMMA4[1:0]		B_GAMMA5[1:0]		B_GAMMA6[1:0]		B_GAMMA7[1:0]		-
	Bank_2_36		B_GAMMA8[1:0]		B_GAMMA9[1:0]		B_GAMMA10[1:0]		B_GAMMA11[1:0]		-
	Bank_2_37		B_GAMMA12[1:0]		B_GAMMA13[1:0]		B_GAMMA14[1:0]		B_GAMMA15[1:0]		-
	Bank_2_38		B_GAMMA16[1:0]		B_GAMMA17[1:0]		B_GAMMA18[1:0]		B_GAMMA19[1:0]		-
	Bank_2_39		B_GAMMA20[1:0]		B_GAMMA21[1:0]		B_GAMMA22[1:0]		B_GAMMA23[1:0]		-
	Bank_2_40		B_GAMMA24[1:0]		B_GAMMA25[1:0]		B_GAMMA26[1:0]		B_GAMMA27[1:0]		-
	Bank_2_41		B_GAMMA28[1:0]		B_GAMMA29[1:0]		B_GAMMA30[1:0]		B_GAMMA31[1:0]		-
	Bank_2_42		B_GAMMA32[1:0]								-
			1	1	0	0	0	0	1	1	
C3	SETID (OTPx3)					ID1[7:0]					83
		1				ID2[7:0]					94
		2				ID3[7:0]					0D
		3				ID4[7:0]					00
		4				ID_TIMES[2:0]*					E0
		5									
C9	SETCABC		1	1	0	0	1	0	0	1	
		1	PWM_PER_IOD[16]		SEL_PWMCLK[2:0]		SEL_GAIN[1:0]	INVPULS(1)	SEL_BLDU_TY(1)		1F
		2				PWM_PERIOD[15:8]					2E

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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
		3				PWM_PERIOD[7:0]					1E
		4	CABC_FS_YNC			DIM_FRAME[6:0]					1E
		5	CABC_DD			BC_CTRL_EN	CABC_FLM[3:0]				00
		6				CABC_STEP[7:0]					1E
		7				SAVE_POWER[6:0]					00
		8	DATAGAIN_EN			-				DATAGAIN_VALUE[9:8]	
		9				DATAGAIN_VALUE[7:0]					
CA	SETCABCGAIN		1	1	0	0	1	0	1	0	
		1	-			DBG0[6:0]					-
		2	-			DBG1[6:0]					-
		3	-			DBG2[6:0]					-
		4	-			DBG3[6:0]					-
		5	-			DBG4[6:0]					-
		6	-			DBG5[6:0]					-
		7	-			DBG6[6:0]					-
		8	-			DBG7[6:0]					-
		9	-			DBG8[6:0]					-
CC	SETPANEL		1	1	0	0	1	1	0	0	
		1	-	-	-	-	SS_PANEL	GS_PANEL	REV_PANE	BGR_PANEL	02
CE	SETCABCLUT		1	1	0	0	1	1	0	1	
		1				DATAGAIN1_00D32[7:0]					40
		2				DATAGAIN1_01D32[7:0]					40
		3				DATAGAIN1_02D32[7:0]					40
		4				DATAGAIN1_03D32[7:0]					40
		5				DATAGAIN1_04D32[7:0]					40
		6				DATAGAIN1_05D32[7:0]					40
		7				DATAGAIN1_06D32[7:0]					40
		8				DATAGAIN1_07D32[7:0]					40
		9				DATAGAIN1_08D32[7:0]					40
		10				DATAGAIN1_09D32[7:0]					41
		11				DATAGAIN1_10D32[7:0]					45
		12				DATAGAIN1_11D32[7:0]					48
		13				DATAGAIN1_12D32[7:0]					4C
		14				DATAGAIN1_13D32[7:0]					4F
		15				DATAGAIN1_14D32[7:0]					50
		16				DATAGAIN1_15D32[7:0]					53
		17				DATAGAIN1_16D32[7:0]					55
		18				DATAGAIN1_17D32[7:0]					58
		19				DATAGAIN1_18D32[7:0]					5A

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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
		20									5C
		21									5E
		22									60
		23									62
		24									64
		25									66
		26									68
		27									6A
		28									6C
		29									6E
		30									6F
		31									71
		32									73
		33									D0
		34									01
D0	SET_SLR_MODE		1	1	0	1	0	0	0	0	
		1									80
		2									40
		3									00
D1	SET_SLR		1	1	0	1	0	0	0	1	
		Bank_0_1									2D
		Bank_0_2									33
		Bank_0_3									00
		Bank_0_4									7F
		Bank_0_5									01
		Bank_0_6									FF
		Bank_0_7									F3
		Bank_0_8									33
		Bank_0_9									F3
		Bank_0_10									33
D3	SETGIP_0		1	1	0	1	0	0	1	1	
		1	-			GIP_EQ_MODE[1:0]					00
		2									00
D9	SETGPO		1	1	0	1	1	0	0	1	
		1	ESD_DET		-						00
		2	EXT_PWR_CTRL		-						01
		3	-		-						02
		4	-		-						07

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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
DE	SETSOR		1	1	0	1	1	1	1	0	
		1	TSENSOR_EN	LT_EN	HT_EN					TEMP_GAP[2:0]	01
E0	SETGAMMA (OTPx1)		1	1	1	0	0	0	0	0	
		1	-	-						VRP0[5:0]	05
		2	-	-						VRP1[5:0]	0C
		3	-	-						VRP2[5:0]	13
		4	-	-						VRP3[5:0]	20
		5	-	-						VRP4[5:0]	39
		6	-	-						VRP5[5:0]	3F
		7	-							PRP0[6:0]	24
		8	-							PRP1[6:0]	39
		9	-	-	-					PKP0[4:0]	08
		10	-	-	-					PKP1[4:0]	0A
		11	-	-	-					PKP2[4:0]	0C
		12	-	-	-					PKP3[4:0]	16
		13	-	-	-					PKP4[4:0]	10
		14	-	-	-					PKP5[4:0]	16
		15	-	-	-					PKP6[4:0]	1A
		16	-	-	-					PKP7[4:0]	17
		17	-	-	-					PKP8[4:0]	17
		18	-	-	-					PKP9[4:0]	06
		19	-	-	-					PKP10[4:0]	0D
		20	-	-	-					PKP11[4:0]	0F
		21	-	-	-					PKP12[4:0]	12
		22	-	-						VRN0[5:0]	05
		23	-	-						VRN1[5:0]	0C
		24	-	-						VRN2[5:0]	11
		25	-	-						VRN3[5:0]	27
		26	-	-						VRN4[5:0]	3B
		27	-	-						VRN5[5:0]	3F
		28	-							PRN0[6:0]	21
		29	-							PRN1[6:0]	3A
		30		-	-					PKN0[4:0]	04
		31		-	-					PKN1[4:0]	07
		32		-	-					PKN2[4:0]	0B
		33		-	-					PKN3[4:0]	16
		34		-	-					PKN4[4:0]	0F
		35	-	-	-					PKN5[4:0]	15
		36	-	-	-					PKN6[4:0]	17
		37	-	-	-					PKN7[4:0]	15

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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)					
		38	-	-	-		PKN8[4:0]				16					
		39	-	-	-		PKN9[4:0]				06					
		40	-	-	-		PKN10[4:0]				0D					
		41	-	-	-		PKN11[4:0]				11					
		42	-	-	-		PKN12[4:0]				17					
E4	SETCHEMODE		1	1	1	0	0	1	0	0						
		1	HUE_MODE[1:0]		SE_MODE[1:0]		BE_MODE[1:0]		CE_MODE[1:0]		00					
		2	-	-	-	-	-	-	-	DYN_CEH_EN	01					
E5	SETCHE		1	1	1	0	0	1	0	1						
		1	MEAN_OFFSET_CE[7:0]								-					
		2	-	-	-	SG0_F[4:0]					-					
		3	-	-	-	SG64_F[4:0]					-					
		4	-	-	-	SG128_F[4:0]					-					
		5	-	-	-	SG192_F[4:0]					-					
		6	-	-	-	SG255_F[4:0]					-					
		7	TH_SAT[7:0]								-					
		8	TH_WHITE[7:0]								-					
		9	TH_COLOR[7:0]								-					
		10	TH_GREY[7:0]								-					
		11	MEAN_OFFSET_BE[7:0]								-					
		12	-	-	-	CG0_F[4:0]					-					
		13	-	-	-	CG64_F[4:0]					-					
		14	-	-	-	CG128_F[4:0]					-					
		15	-	-	-	CG192_F[4:0]					-					
		16	-	-	-	CG255_F[4:0]					-					
		17	THC[7:0]								-					
		18	-	-	-	-	EG2_F[1:0]		EG1_F[1:0]		-					
		19	TH_RFL[7:0]								-					
		20	-	-	-	SG16_F[4:0]					-					
		21	-	-	-	SG32_F[4:0]					-					
		22	-	-	-	SG48_F[4:0]					-					
		23	-	-	-	SG80_F[4:0]					-					
		24	-	-	-	SG96_F[4:0]					-					
		25	-	-	-	SG112_F[4:0]					-					
		26	-	-	-	SG144_F[4:0]					-					
		27	-	-	-	SG160_F[4:0]					-					
		28	-	-	-	SG176_F[4:0]					-					
		29	-	-	-	SG208_F[4:0]					-					
		30	-	-	-	SG224_F[4:0]					-					
		31	-	-	-	SG240_F[4:0]					-					

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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
	32	-	-	-	-		CG16_F[4:0]				-
	33	-	-	-	-		CG32_F[4:0]				-
	34	-	-	-	-		CG48_F[4:0]				-
	35	-	-	-	-		CG80_F[4:0]				-
	36	-	-	-	-		CG96_F[4:0]				-
	37	-	-	-	-		CG112_F[4:0]				-
	38	-	-	-	-		CG144_F[4:0]				-
	39	-	-	-	-		CG160_F[4:0]				-
	40	-	-	-	-		CG176_F[4:0]				-
	41	-	-	-	-		CG208_F[4:0]				-
	42	-	-	-	-		CG224_F[4:0]				-
	43	-	-	-	-		CG240_F[4:0]				-
E6	SETCHESEL		1	1	1	0	0	1	1	0	
		1				ENCH00_SEL[6:0]				ENCH00_SAMPLE_SEL	-
		2				ENCH01_SW[4:0]	ENCH01_SE_OFF	ENCH01_BE_OFF	ENCH01_CE_OFF		-
		3				ENCH02_DS[4:0]	ENCH02_SE_DS	ENCH02_BE_DS	ENCH02_CE_DS		-
		4				ENCH03_reg[7:0]					05
		5				ENCH04_reg[7:0]					05
		6				ENCH05_reg[7:0]					-
		7				ENCH06_reg[7:0]					-
		8				ENCH07_reg[7:0]					-
		9				ENCH08_reg[7:0]					-
		10				ENCH09_reg[7:0]					-
		11				ENCH10_reg[7:0]					-
		12				ENCH11_reg[7:0]					-
		13				ENCH12_reg[7:0]					-
		14				ENCH13_reg[7:0]					-
		15				ENCH14_reg[7:0]					-
		16				ENCH15_reg[7:0]					-
		17				ENCH16_reg[7:0]					-
		18				ENCH17_reg[7:0]					-
		19				ENCH18_reg[7:0]					-
		20				ENCH19_reg[7:0]					-
		21				ENCH20_reg[7:0]					-
		22				ENCH21_reg[7:0]					-
		23				ENCH22_reg[7:0]					-
		24				ENCH23_reg[7:0]					-
		25				ENCH24_reg[7:0]					-

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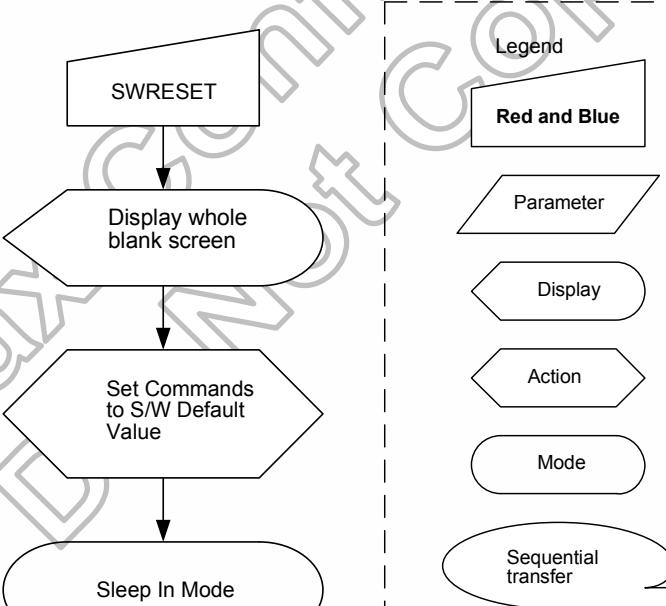
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(Hex)	Operation Code	Parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
FF	26										-
	27										-
	28										-
	29										-
	30										-
	31										-
	32										-
	33										-
	34										-
	35										10
	36										0C
	37										10
	38										-
	39										-
FE	SET READ INDEX		1	1	1	1	1	1	1	0	
		1									00
FF	GETSPIREAD		1	1	1	1	1	1	1	1	
		1									-
											-
											-

### 5.17.3 NOP (00h)

00H	NOP (No Operation)														
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX					
Command	0	0	0	0	0	0	0	0	0	00					
Parameter	NO PARAMETER														
Description	This command is an empty command; it does not have any effect on the display module.														
Restriction	-														
Register Availability	Status					Availability									
	Normal Mode On, Idle Mode Off, Sleep Out					Yes									
	Normal Mode On, Idle Mode On, Sleep Out					Yes									
	Sleep In or Booster Off					Yes									
Default	N/A														
Flow Chart	-														

### 5.17.4 Software reset (01h)

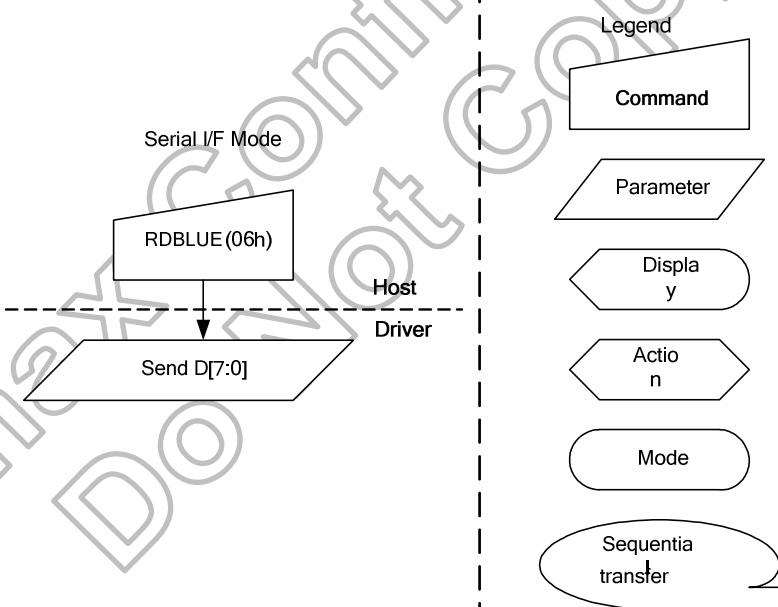
01H	SWRESET (Software Reset)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	0	0	0	0	1	01								
Parameter	NO PARAMETER																	
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)																	
Restriction	<p>It will be necessary to wait 5msec before sending new command following software reset.</p> <p>The display module loads all display supplier's factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.</p> <p>The host processor needs continuing to send PCLK, HSYNC, VSYNC and DE signals to HX8394-D for two frames after this command is sent.</p>																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	N/A																	
Flow Chart	 <pre> graph TD     SWRESET[SWRESET] --&gt; Display[Display whole blank screen]     Display --&gt; Set[Set Commands to S/W Default Value]     Set --&gt; Sleep[Sleep In Mode]   </pre> <p>Legend</p> <ul style="list-style-type: none"> <li>Red and Blue</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Sequential transfer</li> </ul>																	

### 5.17.5 Read Display Identification Information (04h)

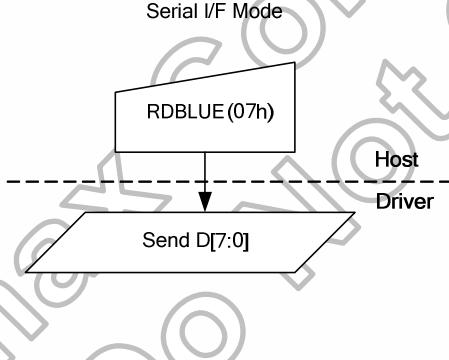
04H		RDDIDIF (Read Display Identification Information)																													
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	0	0	0	0	0	1	0	0	04																					
1 <sup>st</sup> parameter	1	ID1[7:0]								xx																					
2 <sup>nd</sup> parameter	1	1	ID2[6:0]								xx																				
3 <sup>rd</sup> parameter	1	ID3[7:0]								xx																					
Description	<p>This read byte returns 24-bit display identification information. The 1<sup>st</sup> Parameter identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX. The 2<sup>nd</sup> Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Colour). Bits 6..0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:</p> <table border="1"> <thead> <tr> <th>ID Byte Value V[7:0]</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr> <td>80h</td> <td>-</td> <td>-</td> </tr> <tr> <td>81h</td> <td>-</td> <td>-</td> </tr> <tr> <td>82h</td> <td>-</td> <td>-</td> </tr> <tr> <td>83h</td> <td>-</td> <td>-</td> </tr> <tr> <td>84h</td> <td>-</td> <td>-</td> </tr> <tr> <td>85h</td> <td>-</td> <td>-</td> </tr> </tbody> </table> <p>The 3<sup>rd</sup> parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.</p>										ID Byte Value V[7:0]	Version	Changes	80h	-	-	81h	-	-	82h	-	-	83h	-	-	84h	-	-	85h	-	-
ID Byte Value V[7:0]	Version	Changes																													
80h	-	-																													
81h	-	-																													
82h	-	-																													
83h	-	-																													
84h	-	-																													
85h	-	-																													
Restriction	-																														
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value													
Status	Default Value																														
Power On Sequence	OTP Value																														
S/W Reset	OTP Value																														
H/W Reset	OTP Value																														
Flow Chart	<pre> graph TD     Start([RDDIDIF (04h)]) --&gt; Send1[/Send ID1[7:0]/]     Send1 --&gt; Send2[/Send ID2[6:0]/]     Send2 --&gt; Send3[/Send ID3[7:0]/]   </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																														

#### 5.17.6 RDNUMPE: Read number of the parity errors (05h)

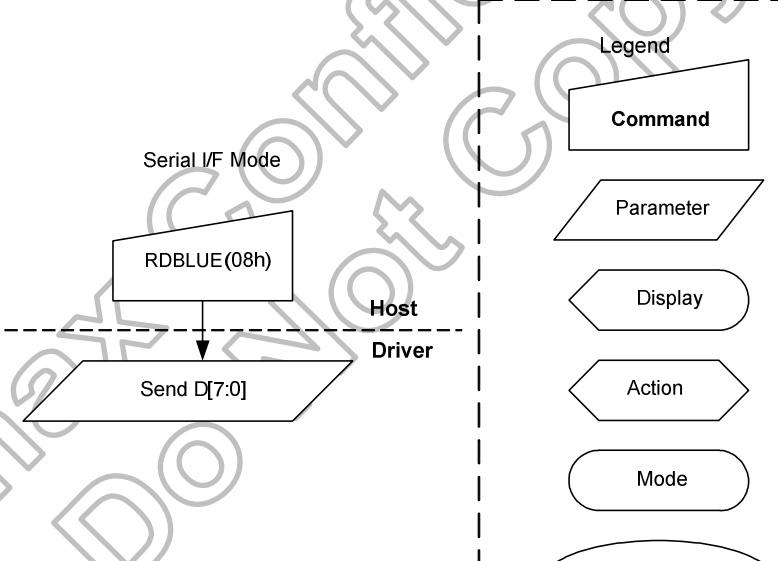
### 5.17.7 Get\_red\_channel (06h)

06H	RDRED (Read Red Colour)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	0	0	1	1	0	06								
1 <sup>st</sup> parameter	1	R7	R6	R5	R4	R3	R2	R1	R0	xx								
Description	The first parameter is telling red colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'. 24 bit format: R7 is MSB and R0 is LSB.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
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Normal Mode On, Idle Mode On, Sleep Out	Yes																	
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	 <pre> graph TD     Host[Host] -- "RDBLUE(06h)" --&gt; Driver[Driver]     Driver -- "Send D[7:0]" --&gt; Host   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

### 5.17.8 Get\_green\_channel (07h)

07H	RDGREEN (Read Green Colour)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	0	0	1	1	1	07								
1 <sup>st</sup> parameter	1	G7	G6	G5	G4	G3	G2	G1	G0	xx								
Description	The first parameter is telling green colour value of the first pixel of the frame when there is used DPI I/F. 16 and 18 bit formats: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. 24 bit format: G7 is MSB and G0 is LSB.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	 <p>The flowchart illustrates the process of reading the green channel. A box labeled "RDBLUE(07h)" is at the top. An arrow points from it down to a trapezoid labeled "Send D[7:0]". This trapezoid is positioned above a dashed horizontal line labeled "Host Driver". Above this line, the text "Serial I/F Mode" is written. To the right of the flowchart, a legend defines symbols: a rectangle for "Command", a parallelogram for "Parameter", a left-pointing triangle for "Display", an upward-pointing triangle for "Action", an oval for "Mode", and a rounded rectangle for "Sequential transfer".</p>																	

### 5.17.9 Get\_blue\_channel (08h)

08H	RDBLUE (Read Blue Colour)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	0	1	0	0	0	08								
1 <sup>st</sup> parameter	1	B7	B6	B5	B4	B3	B2	B1	B0	xx								
Description	The first parameter is telling blue colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'. 24 bit format: B7 is MSB and B0 is LSB.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	 <pre> graph TD     Host -- "RDBLUE(08h)" --&gt; Driver     Driver -- "Send D[7:0]" --&gt; Host   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

### 5.17.10 Read Display Status (09h)

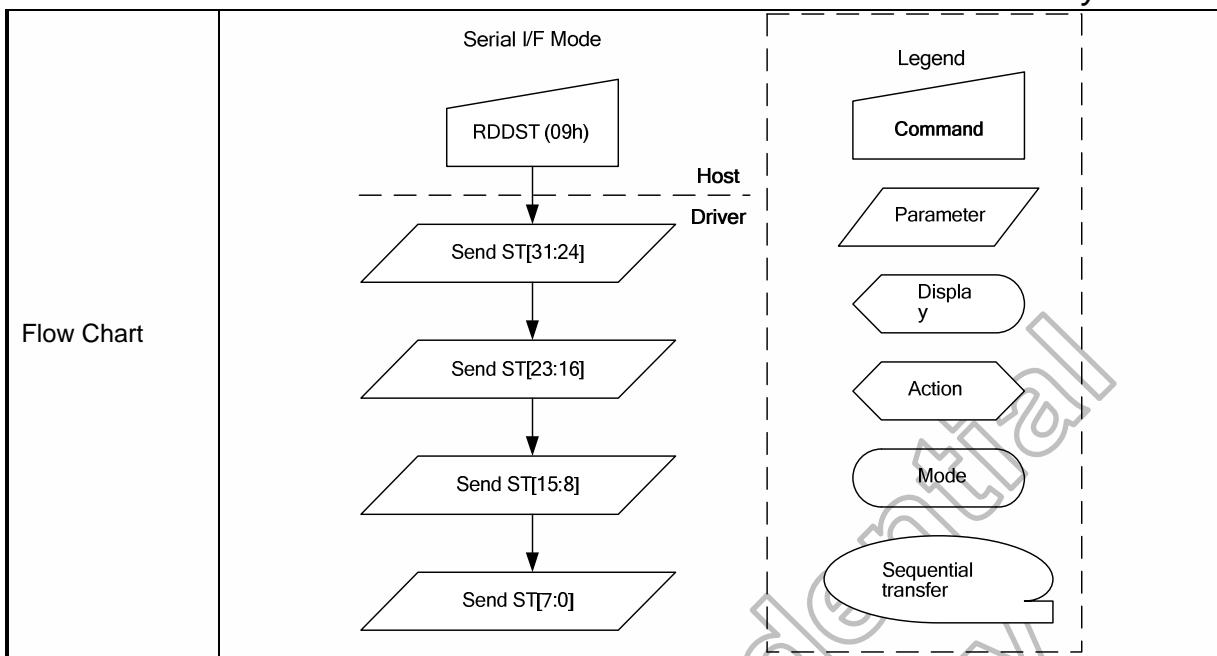
09H	RDDST (Read Display Status)																																																																																																													
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																				
Command	0	0	0	0	0	1	0	0	1	09																																																																																																				
1 <sup>st</sup> parameter	1					D[31:24]				xx																																																																																																				
2 <sup>nd</sup> parameter	1					D[23:16]				xx																																																																																																				
3 <sup>rd</sup> parameter	1					D[15:8]				xx																																																																																																				
4 <sup>th</sup> parameter	1					D[7:0]				xx																																																																																																				
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D31</td> <td>Booster Voltage Status</td> <td>-</td> </tr> <tr> <td>D30</td> <td>Page Address Order</td> <td>Set to '0'</td> </tr> <tr> <td>D29</td> <td>Column Address Order</td> <td>Set to '0'</td> </tr> <tr> <td>D28</td> <td>Page/Column Order</td> <td>Set to '0'</td> </tr> <tr> <td>D27</td> <td>Vertical Order</td> <td>Set to '0'</td> </tr> <tr> <td>D26</td> <td>RGB/BGR Order</td> <td>-</td> </tr> <tr> <td>D25</td> <td>Horizontal Order</td> <td>Set to '0'</td> </tr> <tr> <td>D24</td> <td>Source scan sequence</td> <td>-</td> </tr> <tr> <td>D23</td> <td>Gate scan sequence</td> <td>-</td> </tr> <tr> <td>D22</td> <td colspan="2" style="text-align:center;">Interface Colour Pixel Format Definition</td></tr> <tr> <td>D21</td> <td colspan="2"></td></tr> <tr> <td>D20</td> <td colspan="2"></td></tr> <tr> <td>D19</td> <td>Idle Mode On/Off</td> <td>-</td> </tr> <tr> <td>D18</td> <td>Partial Mode On/Off</td> <td>Set to '0'</td> </tr> <tr> <td>D17</td> <td>Sleep In/Out</td> <td>-</td> </tr> <tr> <td>D16</td> <td>Display Normal Mode On/Off</td> <td>-</td> </tr> <tr> <td>D15</td> <td>Vertical Scrolling Status</td> <td>Set to '0'</td> </tr> <tr> <td>D14</td> <td>Horizontal Scrolling Status</td> <td>Set to '0'</td> </tr> <tr> <td>D13</td> <td>Inversion Status</td> <td>-</td> </tr> <tr> <td>D12</td> <td>All Pixels On</td> <td>-</td> </tr> <tr> <td>D11</td> <td>All Pixels Off</td> <td>-</td> </tr> <tr> <td>D10</td> <td>Display On/Off</td> <td>-</td> </tr> <tr> <td>D9</td> <td>Tearing Effect Line On/Off</td> <td>-</td> </tr> <tr> <td>D8</td> <td colspan="2" style="text-align:center;">Gamma Curve Selection</td></tr> <tr> <td>D7</td> <td colspan="2"></td></tr> <tr> <td>D6</td> <td colspan="2"></td></tr> <tr> <td>D5</td> <td>Tearing Effect Output Line Mode</td> <td>-</td> </tr> <tr> <td>D4</td> <td>Horizontal Sync. (HSYNC, DPI I/F)</td> <td>-</td> </tr> <tr> <td>D3</td> <td>Vertical Sync. (VSYNC, DPI I/F)</td> <td>-</td> </tr> <tr> <td>D2</td> <td>Pixel Clock (DCK, DPI I/F)</td> <td>-</td> </tr> <tr> <td>D1</td> <td>Data Enable (ENABLE, DPI I/F)</td> <td>-</td> </tr> <tr> <td>D0</td> <td>For Future Use</td> <td>Set to '0'</td> </tr> </tbody> </table> Bit Values are explained overleaf. Bit D31 – Booster Voltage Status '0' = Booster Off. '1' = Booster On. Bit D30 – Page Address Order '0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1'). This bit is not applicable for this project, so it is set to '0' Bit D29 – Column Address Order '0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1'). This bit is not applicable for this project, so it is set to '0' Bit D28 – Page/Column Order '0' = Normal (When MADCTL B5='0').	Bit	Description	Comment	D31	Booster Voltage Status	-	D30	Page Address Order	Set to '0'	D29	Column Address Order	Set to '0'	D28	Page/Column Order	Set to '0'	D27	Vertical Order	Set to '0'	D26	RGB/BGR Order	-	D25	Horizontal Order	Set to '0'	D24	Source scan sequence	-	D23	Gate scan sequence	-	D22	Interface Colour Pixel Format Definition		D21			D20			D19	Idle Mode On/Off	-	D18	Partial Mode On/Off	Set to '0'	D17	Sleep In/Out	-	D16	Display Normal Mode On/Off	-	D15	Vertical Scrolling Status	Set to '0'	D14	Horizontal Scrolling Status	Set to '0'	D13	Inversion Status	-	D12	All Pixels On	-	D11	All Pixels Off	-	D10	Display On/Off	-	D9	Tearing Effect Line On/Off	-	D8	Gamma Curve Selection		D7			D6			D5	Tearing Effect Output Line Mode	-	D4	Horizontal Sync. (HSYNC, DPI I/F)	-	D3	Vertical Sync. (VSYNC, DPI I/F)	-	D2	Pixel Clock (DCK, DPI I/F)	-	D1	Data Enable (ENABLE, DPI I/F)	-	D0	For Future Use	Set to '0'										
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D1	Data Enable (ENABLE, DPI I/F)	-																																																																																																												
D0	For Future Use	Set to '0'																																																																																																												

'1' = Rotation (When MADCTL B5='1').  
 This bit is not applicable for this project, so it is set to '0'  
 Bit D27 – Line Address Order  
 '0' = LCD Refresh Top to Bottom (When MADCTL B4='0').  
 '1' = LCD Refresh Bottom to Top (When MADCTL B4='1').  
 This bit is not applicable for this project, so it is set to '0'  
 Bit D26 – RGB/BGR Order  
 '0' = RGB (When MADCTL B3='0').  
 '1' = BGR (When MADCTL B3='1').  
 This bit is not applicable for this project, so it is set to '0'  
 Bit D24 – Source scan sequence  
 '0' = Normal (When MADCTL B1='0').  
 '1' = Flipped (When MADCTL B1='1').  
 Bit D23 – Gate scan sequence  
 '0' = Normal (When MADCTL B0='0').  
 '1' = Flipped (When MADCTL B0='1').  
 Bits D22, D21, D20 – Interface Colour Pixel Format Definition

Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

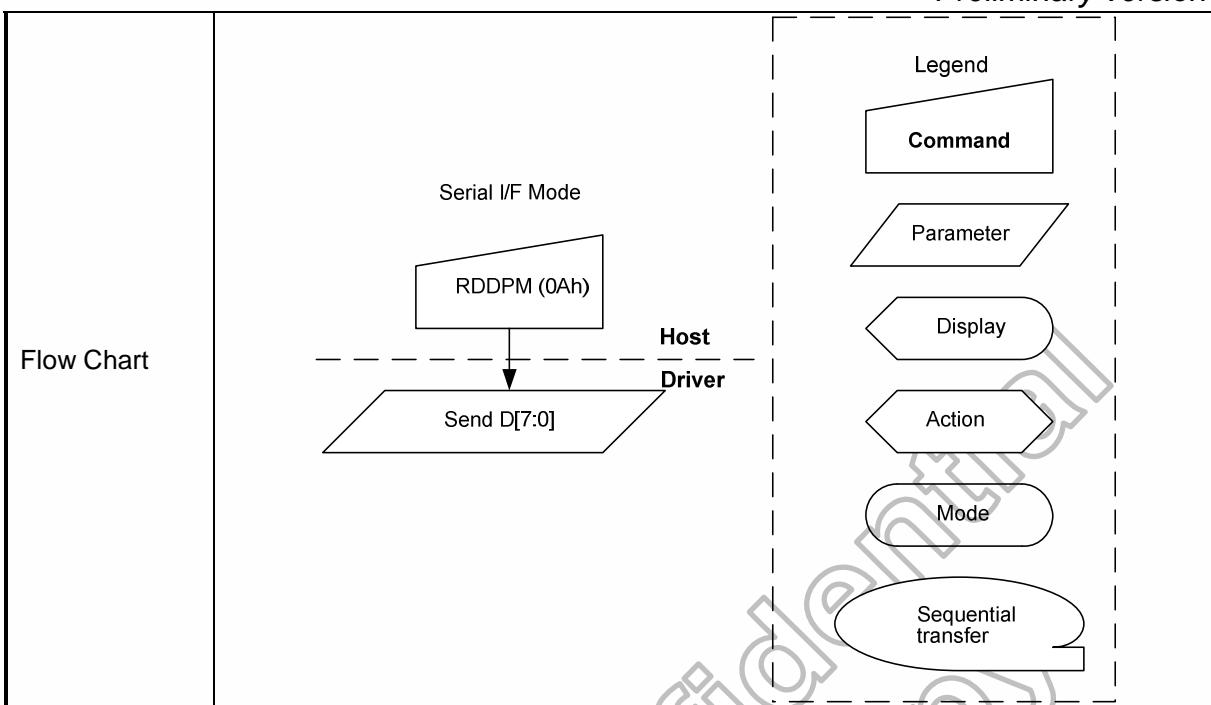
Bit D19 – Idle Mode On/Off  
 '0' = Idle Mode Off.  
 '1' = Idle Mode On.  
 Bit D18 – Partial Mode On/Off  
 '0' = Partial Mode Off.  
 '1' = Partial Mode On.  
 This bit is not applicable for this project, so it is set to '0'  
 Bit D17 – Sleep In/Out  
 '0' = Sleep In Mode.  
 '1' = Sleep Out Mode.  
 Bit D16 – Display Normal Mode On/Off  
 '0' = Partial or Scrolling Mode.  
 '1' = Normal Mode.  
 Bit D15 – Vertical Scrolling On/Off  
 '0' = Vertical Scrolling is Off.  
 '1' = Vertical Scrolling is On.  
 This bit is not applicable for this project, so it is set to '0'  
 Bit D14 – Horizontal Scrolling Status  
 This bit is not applicable for this project, so it is set to '0'  
 Bit D13 – Inversion On/Off  
 '0' = Inversion is Off.  
 '1' = Inversion is On.  
 Bit D12 – All Pixels On.  
 '0' = Nornal mode.  
 '1' = All Pixels On.  
 Bit D11 – All Pixels Off.  
 '0' = Nornal mode.  
 '1' = All Pixels Off.  
 Bit D10 – Display On/Off  
 '0' = Display is Off.  
 '1' = Display is On.  
 Bit D9 – Tearing Effect Line On/Off  
 '0' =Tearing Effect Line Off.  
 '1' = Tearing Effect On.  
 Bits D8, D7, D6 – Gamma Curve Selection

	Gamma Curve Selected	B8	B7	B6	Gamma Set (26h) Parameter
	Gamma Curve 1	0	0	0	GC0
	Gamma Curve 2	0	0	1	Setting Inhibit
	Gamma Curve 3	0	1	0	Setting Inhibit
	Gamma Curve 4	0	1	1	Setting Inhibit
	Not Defined	1	0	0	Not Defined
	Not Defined	1	0	1	Not Defined
	Not Defined	1	1	0	Not Defined
	Not Defined	1	1	1	Not Defined
Bit D5 – Tearing Effect Line Output Mode. '0' = Mode 1, V-Blanking only. '1' = Mode 2, both H-Blanking and V-Blanking.					
Bit D4 – Horizontal Sync. (HSYNC) On/Off, Note '0' = Horizontal Sync. Line is Off ("Low"). '1' = Horizontal Sync. Line is On ("High").					
Bit D3 – Vertical Sync. (VSYNC) On/Off, Note '0' = Vertical Sync. Line is Off ("Low"). '1' = Vertical Sync. Line is On ("High").					
Bit D2 – Pixel Clock (PCLK) On/Off, Note '0' = Pixel Clock line is Off ("Low"). '1' = Pixel Clock line is On ("High").					
Bit D1 – Data Enable (DE) On/Off, Note '0' = Data Enable line is Off ("Low"). '1' = Data Enable line is On ("High").					
Bit D0 – Parity Error check This bit is not applicable for this project, so it is set to '0'					
Note: This bit indicates current status of the line when this command has been sent.					
Restriction					
Register Availability	Status	Availability			
	Normal Mode On, Idle Mode Off, Sleep Out	Yes			
	Normal Mode On, Idle Mode On, Sleep Out	Yes			
	Sleep In or Booster Off	Yes			
Default	Status	Default Value			
	Power On Sequence	Refer to Description			
	S/W Reset	Refer to Description			
	H/W Reset	Refer to Description			



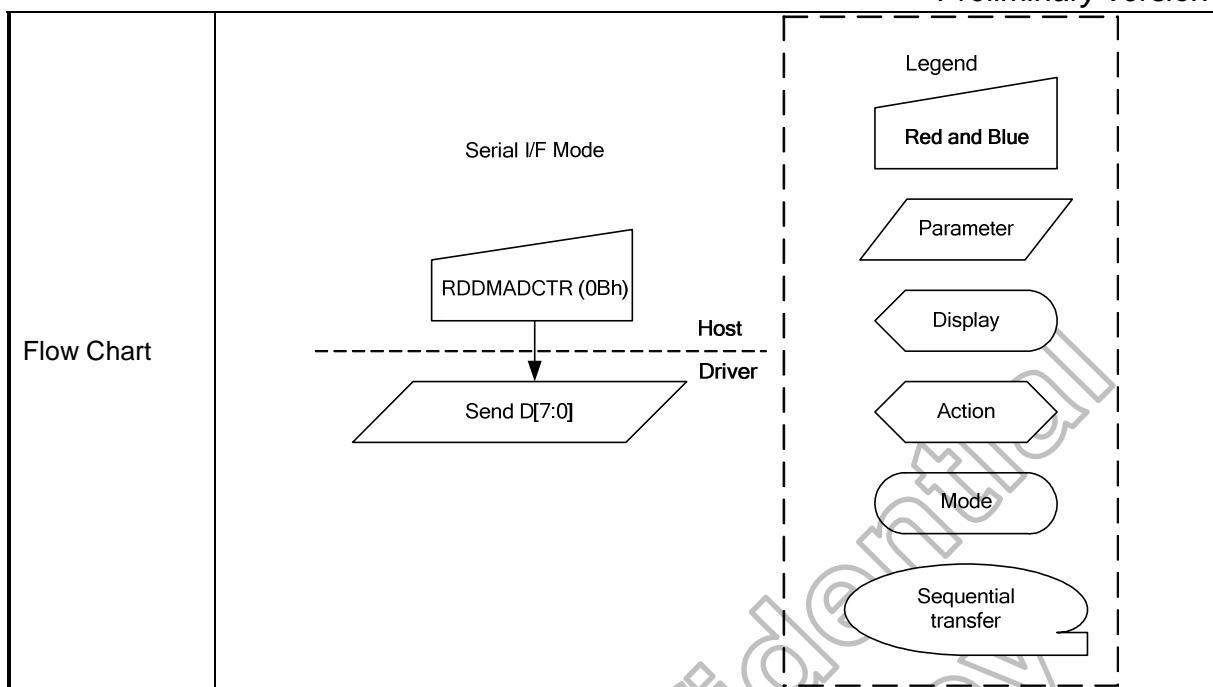
### 5.17.11 Get\_power\_mode (0Ah)

0AH		RDDPM (Read Display Power Mode)																																				
		DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command		0	0	0	0	0	1	0	1	0	0A																											
1 <sup>st</sup> parameter		1	0	D6	0	D4	D3	D2	0	0	xx																											
		This command indicates the current status of the display as described in the table below:																																				
		<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Not Defined</td><td>Set to '0'</td></tr> <tr> <td>D6</td><td>Idle Mode On/Off</td><td>-</td></tr> <tr> <td>D5</td><td>Partial Mode On/Off</td><td>Set to '0'</td></tr> <tr> <td>D4</td><td>Sleep In/Out</td><td>-</td></tr> <tr> <td>D3</td><td>Display Normal Mode On/Off</td><td>-</td></tr> <tr> <td>D2</td><td>Display On/Off</td><td>-</td></tr> <tr> <td>D1</td><td>Not Defined</td><td>Set to '0'</td></tr> <tr> <td>D0</td><td>Not Defined</td><td>Set to '0'</td></tr> </tbody> </table>										Bit	Description	Comment	D7	Not Defined	Set to '0'	D6	Idle Mode On/Off	-	D5	Partial Mode On/Off	Set to '0'	D4	Sleep In/Out	-	D3	Display Normal Mode On/Off	-	D2	Display On/Off	-	D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
Bit	Description	Comment																																				
D7	Not Defined	Set to '0'																																				
D6	Idle Mode On/Off	-																																				
D5	Partial Mode On/Off	Set to '0'																																				
D4	Sleep In/Out	-																																				
D3	Display Normal Mode On/Off	-																																				
D2	Display On/Off	-																																				
D1	Not Defined	Set to '0'																																				
D0	Not Defined	Set to '0'																																				
Description		<p>Bit D7 is for future use and set to '0'.</p> <p>Bit D6 – Idle Mode On/Off        '0' = Idle Mode Off.        '1' = Idle Mode On.</p> <p>Bit D5 – Partial Mode On/Off        '0' = Partial Mode Off.        '1' = Partial Mode On.</p> <p>This bit is not applicable for this project, so it is set to '0'</p> <p>Bit D4 – Sleep In/Out        '0' = Sleep In Mode.        '1' = Sleep Out Mode.</p> <p>Bit D3 – Display Normal Mode On/Off        '0' = Display Normal Mode Off.        '1' = Display Normal Mode On.</p> <p>Bit D2 – Display On/Off        '0' = Display is Off.        '1' = Display is On.</p>																																				
Restrictions		-																																				
Register Availability		<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																			
Status	Availability																																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																					
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Sleep In or Booster Off	Yes																																					
Default		<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>08h</td></tr> <tr> <td>S/W Reset</td><td>08h</td></tr> <tr> <td>H/W Reset</td><td>08h</td></tr> </tbody> </table>										Status	Default Value	Power On Sequence	08h	S/W Reset	08h	H/W Reset	08h																			
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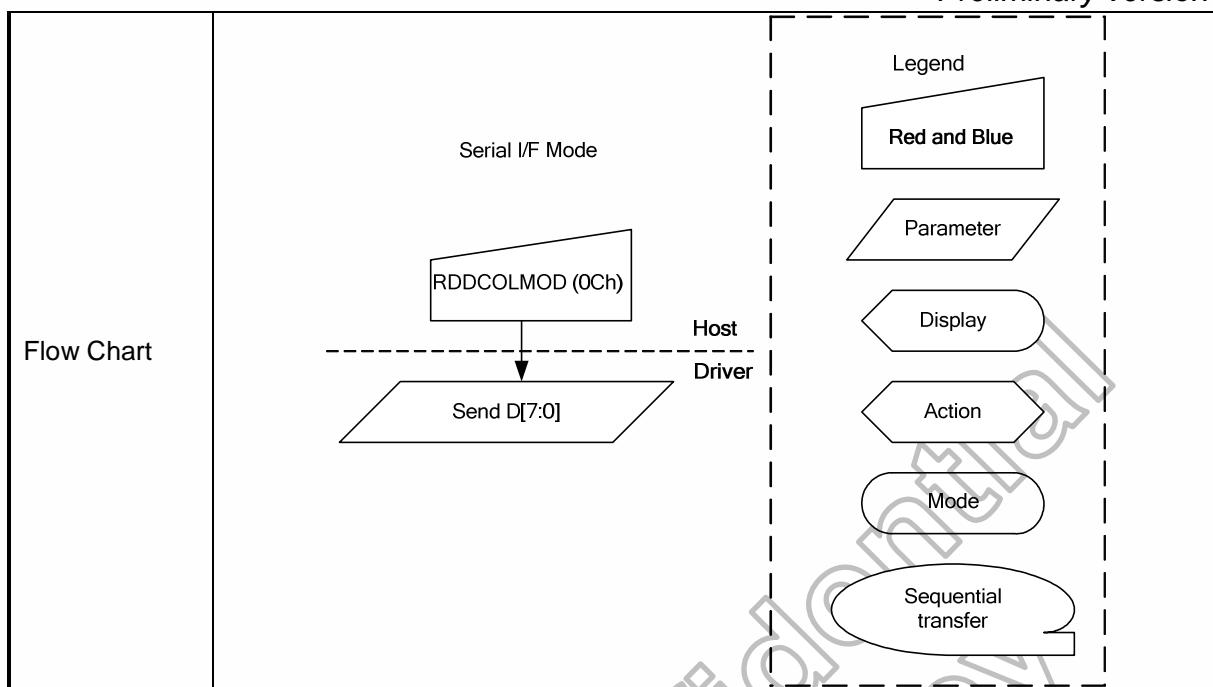
### 5.17.12 Read display MADCTL (0Bh)

0BH		RDDMADCTL (Read Display MADCTL)																		
		DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command		0	0	0	0	0	1	0	1	1	0B									
1 <sup>st</sup> parameter		1	0	0	0	0	D3	0	D1	D0	xx									
Description		This command indicates the current status of the display as described in the table below:																		
		Bit	Description				Comment													
		D7	Page Address Order				Set to '0'													
		D6	Column Address Order				Set to '0'													
		D5	Page/Column Order				Set to '0'													
		D4	Line Address Order				Set to '0'													
		D3	RGB/BGR Order				-													
		D2	Display Data Latch Order				Set to '0'													
		D1	Source scan sequence				-													
		D0	Gate scan sequence				-													
Restrictions		Bit D7 – Page Address Order This bit is not applicable for this project, so it is set to "0".																		
		Bit D6 – Column Address Order This bit is not applicable for this project, so it is set to "0".																		
		Bit D5 – Page/Column Order This bit is not applicable for this project, so it is set to "0".																		
		Bit D4 – Line Address Order This bit is not applicable for this project, so it is set to "0".																		
		Bit D3 – RGB/BGR Order '0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1').																		
		Bit D2 – Display Data Latch Data Order This bit is not applicable for this project, so it is set to "0".																		
		Bit D1 – Source scan sequence '0' = Normal (When MADCTL B1='0'). '1' = Flipped (When MADCTL B1='1').																		
		Bit D0 – Gate scan sequence '0' = Normal (When MADCTL B0='0').																		
Register Availability		-																		
		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In or Booster Off	Yes																			
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h	
Status	Default Value																			
Power On Sequence	00h																			
S/W Reset	00h																			
H/W Reset	00h																			



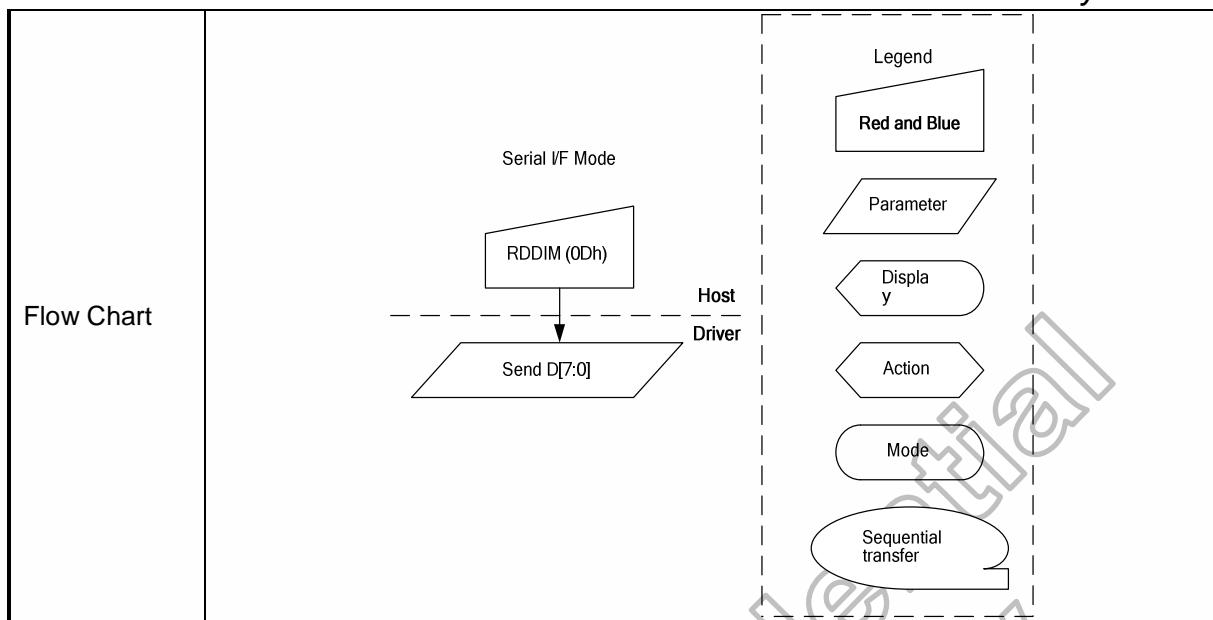
### 5.17.13 Get\_pixel\_format (0Ch)

0CH		RDDCOLMOD (Read Display COLMOD)																																												
		DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command		0	0	0	0	0	1	1	0	0	0C																																			
1 <sup>st</sup> parameter		1	0	D6	D5	D4	0	0	0	0	xx																																			
Description	This command indicates the current status of the display as described in the table below:																																													
	Bit	Description						Comment																																						
	D7	Reserved						Set to '0'																																						
	D6							-																																						
	D5	DPI Interface Pixel format						-																																						
	D4							-																																						
	D3	Reserved						Set to '0'																																						
	D2	Reserved						Set to '0'																																						
	D1	Reserved						Set to '0'																																						
	D0	Reserved						Set to '0'																																						
Description	Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition Bits D2, D1, D0 – DBI Interface Colour Pixel Format Definition. This bit is not applicable for this project, so it is set to "0".																																													
	<table border="1"> <thead> <tr> <th>Interface Colour Format</th> <th>D6</th> <th>D5</th> <th>D4</th> </tr> </thead> <tbody> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 bit/pixel</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 bit/pixel</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>24 bit/pixel</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>										Interface Colour Format	D6	D5	D4	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	Not Defined	0	1	1	Not Defined	1	0	0	16 bit/pixel	1	0	1	18 bit/pixel	1	1	0	24 bit/pixel	1	1	1
Interface Colour Format	D6	D5	D4																																											
Not Defined	0	0	0																																											
Not Defined	0	0	1																																											
Not Defined	0	1	0																																											
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Not Defined	1	0	0																																											
16 bit/pixel	1	0	1																																											
18 bit/pixel	1	1	0																																											
24 bit/pixel	1	1	1																																											
If the setting is not used then the corresponding bits in the parameter returned from																																														
Restrictions										-																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																												
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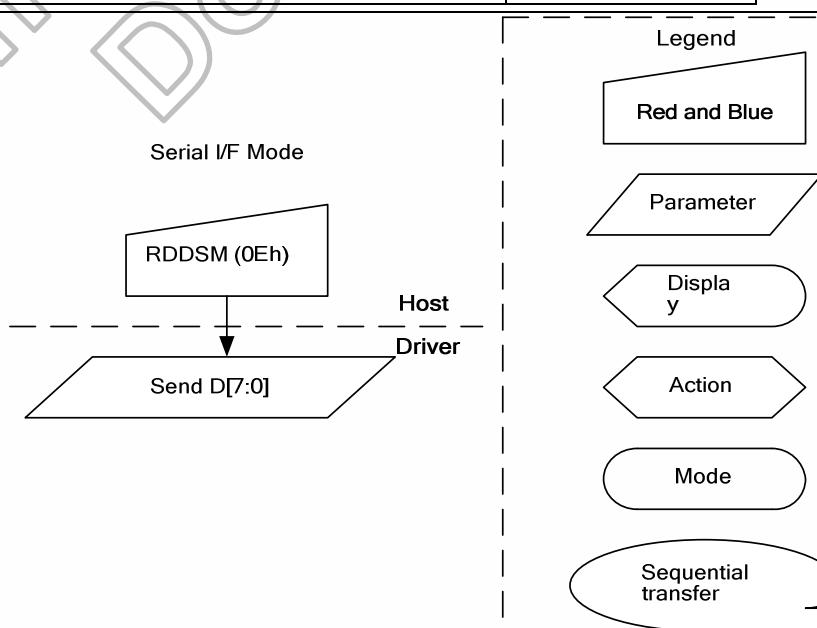


### 5.17.14 Get\_display\_mode (0Dh)

0DH	RDDIM (Read Display Image Mode)																																																							
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																														
Command	0	0	0	0	0	1	1	0	1	0D																																														
1 <sup>st</sup> parameter	1	0	0	D5	D4	D3	D2	D1	D0	xx																																														
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Vertical Scrolling On/Off This bit is not applicable for this project, so it is set to '0' Bit D6 – Horizontal Scrolling Status This bit is not applicable for this project, so it is set to '0' Bit D5 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On. Bit D4 – All Pixels On '0' = Normal Display '1' = White Display Bit D3 – All Pixels Off '0' = Normal Display '1' = Black Display Bits D2, D1, D0 – Gamma Curve Selection <table border="1" style="margin-left: 20px;"> <tr> <th>Gamma Curve Selected</th> <th>D2</th> <th>D1</th> <th>D0</th> <th>Gamma Set (26h) Parameter</th> </tr> <tr> <td>Gamma Curve1</td> <td>0</td> <td>0</td> <td>0</td> <td>GC0</td> </tr> <tr> <td>Gamma Curve2</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting Inhibit</td> </tr> <tr> <td>Gamma Curve3</td> <td>0</td> <td>1</td> <td>0</td> <td>Setting Inhibit</td> </tr> <tr> <td>Gamma Curve4</td> <td>0</td> <td>1</td> <td>1</td> <td>Setting Inhibit</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>1</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>1</td> <td>Not Defined</td> </tr> </table>											Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter	Gamma Curve1	0	0	0	GC0	Gamma Curve2	0	0	1	Setting Inhibit	Gamma Curve3	0	1	0	Setting Inhibit	Gamma Curve4	0	1	1	Setting Inhibit	Not Defined	1	0	0	Not Defined	Not Defined	1	0	1	Not Defined	Not Defined	1	1	0	Not Defined	Not Defined	1	1	1	Not Defined
Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter																																																				
Gamma Curve1	0	0	0	GC0																																																				
Gamma Curve2	0	0	1	Setting Inhibit																																																				
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Default	Status			Default Value																																																				
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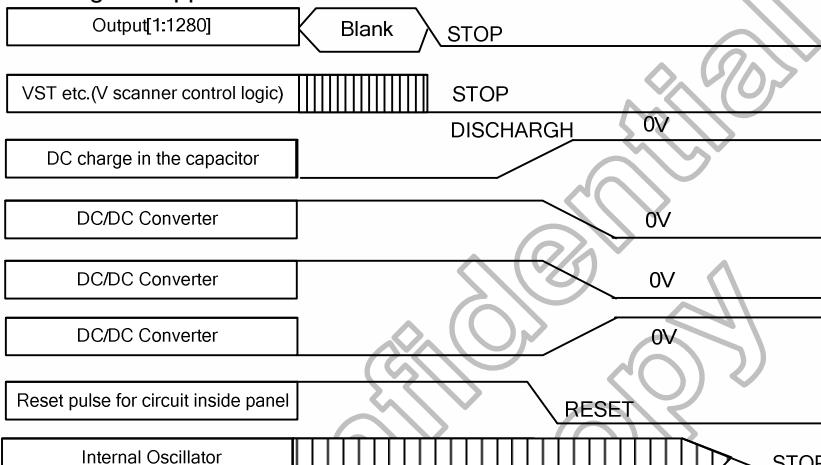
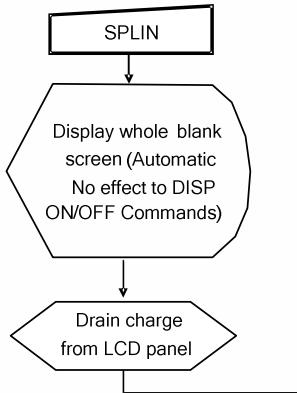
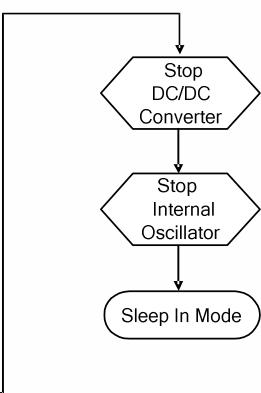
### 5.17.15 Get\_signal\_mode (0Eh)

0EH		RDDSM (Read Display Signal Mode)																	
		DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command		0	0	0	0	0	1	1	1	0	0E								
1 <sup>st</sup> parameter		1	D7	D6	D5	D4	D3	D2	0	0	xx								
Description	<p>This command indicates the current status of the display described in the table as below:</p> <p>Bit D7 – Tearing Effect Line On/Off          '0' = Tearing Effect Line Off.          '1' = Tearing Effect On.</p> <p>Bit D6 – Tearing Effect Line Output Mode, see section 5.1 for mode definitions.          '0' = Mode 1.          '1' = Mode 2.</p> <p>Bit D5 – Horizontal Sync. (DPI I/F) On/Off.          '0' = Horizontal Sync. Line is Off ("Low").          '1' = Horizontal Sync. Line is On ("High").</p> <p>Bit D4 – Vertical Sync. (DPI I/F) On/Off.          '0' = Vertical Sync. Line is Off ("Low").          '1' = Vertical Sync. Line is On ("High").</p> <p>Bit D3 – Pixel Clock (PCLK, DPI I/F) On/Off.          '0' = PCLK line is Off ("Low").          '1' = PCLK line is On ("High").</p> <p>Bit D2 – Data Enable (DE, DPI I/F) On/Off.          '0' = DE line is Off ("Low").          '1' = DE line is On ("High").</p> <p>Bits D[1:0] – Reserved.</p>																		
Restrictions	-																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																		
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Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> <li>Red and Blue</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																		

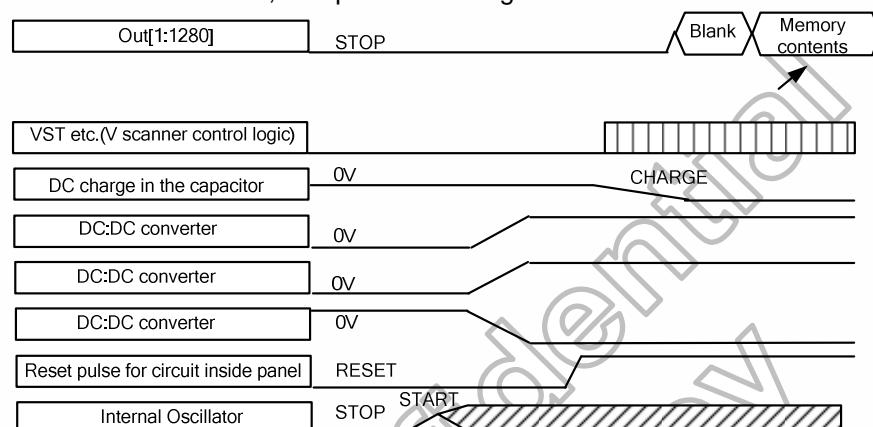
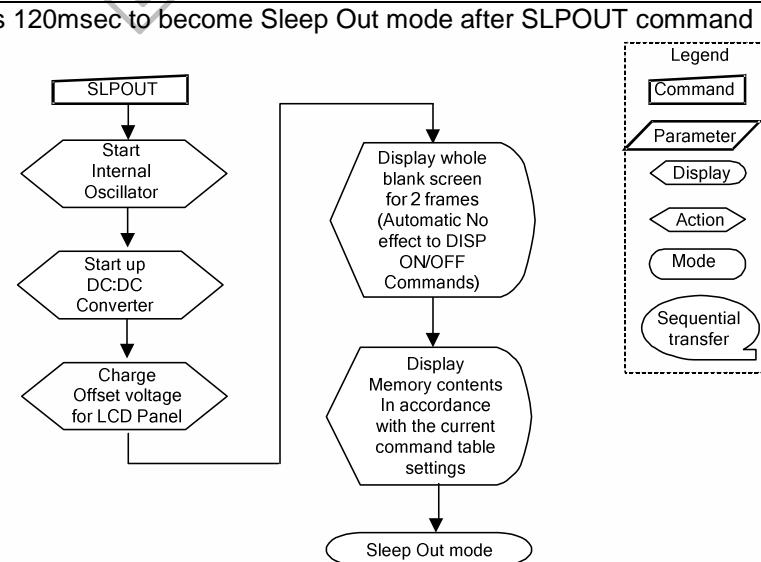
### 5.17.16 Get\_diagnostic\_result (0Fh)

0FH	RDDSDR (Read Display Self-Diagnostic Result)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	0	1	1	1	1	0F								
1 <sup>st</sup> parameter	1	D7	D6	D5	D4	0	0	0	0	xx								
Description	<p>The display module returns the self-diagnostic results following a Sleep Out command. See section 5.10 for a description of the status results.</p> <p>Bit D7 – Register Loading Detection</p> <p>Bit D6 – Functionality Detection</p> <p>Bit D5 – Chip Attachment Detection</p> <p>Set to '0' if feature unimplemented.</p> <p>Bit D4 – Display Glass Break Detection</p> <p>Set to '0' if feature unimplemented.</p> <p>Bits D[3:0] – Reserved.</p>																	
Restrictions	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	<pre> graph TD     Host[Host] -- "Serial I/F Mode" --&gt; RDDSDR[RDDSDR (0Fh)]     RDDSDR --&gt; SendD[Send D[7:0]]     SendD --&gt; Driver[Driver]   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Red and Blue: Parameter</li> <li>Parameter: Sequential transfer</li> <li>Display: Action</li> <li>Action: Mode</li> <li>Mode: Legend</li> </ul>																	

### 5.17.17 Enter\_sleep\_mode (10h)

10H	SLPIN (Sleep In)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	1	0	0	0	0	10								
Parameter	NO PARAMETER																	
Description	<p>This command causes the LCD module to enter the minimum power consumption mode.</p> <p>In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p> 																	
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p> <p>The host processor continues to send PCLK, HSYNC, and VSYNC and DE signals to HX8394-D for two frames after this command is sent.</p>																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	N/A																	
Flow Chart	  <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

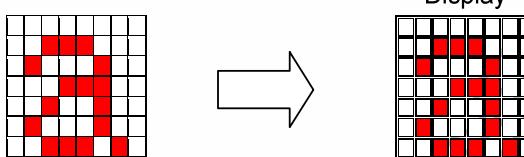
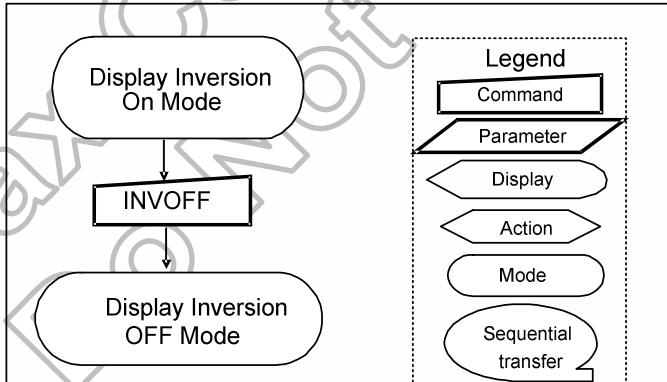
### 5.17.18 Exit\_sleep\_omde (11h)

11H		SLPOUT (Sleep Out)																	
		DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command		0	0	0	0	1	0	0	0	1	11								
Parameter	NO PARAMETER																		
Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p> 																		
Restriction	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out -mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p> <p>The host processor continues to send PCLK, HSYNC, and VSYNC and DE signals to HX8394-D for two frames after this command is sent.</p>																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		
Default	N/A																		
Flow Chart	<p>It takes 120msec to become Sleep Out mode after SLPOUT command issued.</p> 																		

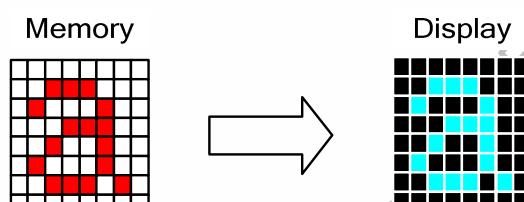
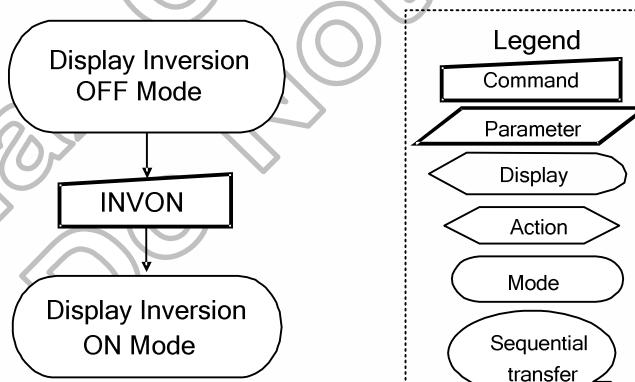
### 5.17.19 Enter\_normal\_mode (13h)

13H	NORON (Normal Display Mode On)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER									
Description	This command returns the display to normal mode.									
Restriction	This command has no effect when Normal Display mode is active.									
Register Availability	Status		Availability							
	Normal Mode On, Idle Mode Off, Sleep Out		Yes							
	Normal Mode On, Idle Mode On, Sleep Out		Yes							
	Sleep In or Booster Off		Yes							
Default	Status		Default Value							
	Power On Sequence		Normal display mode							
	S/W Reset		Normal display mode							
	H/W Reset		Normal display mode							
Flow Chart	-									

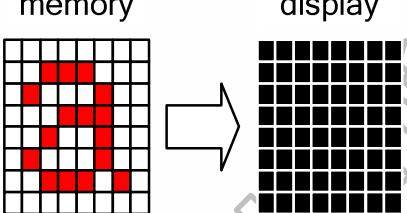
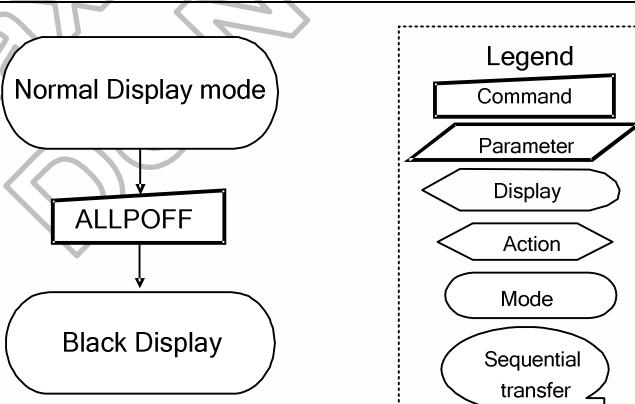
### 5.17.20 Exit\_inversion\_mode (20h)

20H		INVOFF (Display Inversion Off)																
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	0	0	0	0	20								
Parameter	NO PARAMETER																	
Description	<p>This command is used to recover from display inversion mode. This command does not change any other status.</p> <p style="text-align: center;">(Example)</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;">Memory</div> <div style="text-align: center;">Display</div> </div> 																	
Restriction	This command has no effect when module is already in inversion off mode.																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In or Booster Off</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Normal display mode</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Normal display mode</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Normal display mode</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Normal display mode	S/W Reset	Normal display mode	H/W Reset	Normal display mode
Status	Default Value																	
Power On Sequence	Normal display mode																	
S/W Reset	Normal display mode																	
H/W Reset	Normal display mode																	
Flow Chart	 <pre> graph TD     A([Display Inversion On Mode]) --&gt; B[INVOFF]     B --&gt; C([Display Inversion OFF Mode])     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

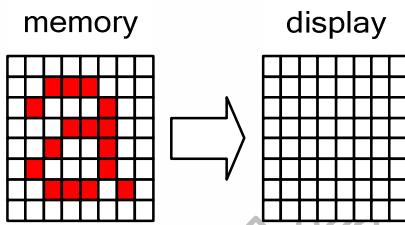
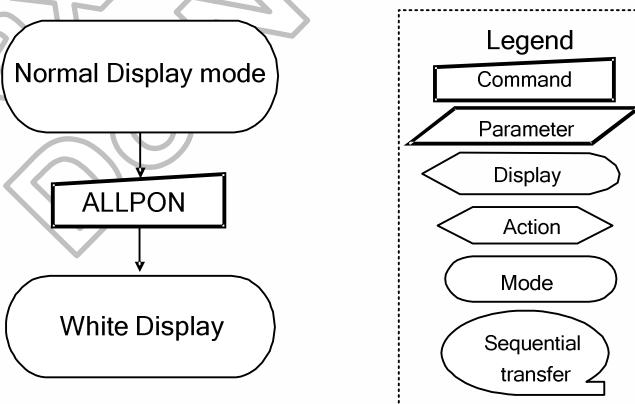
### 5.17.21 Enter\_inversion\_mode (21h)

21H	INVON (Display Inversion On)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	0	0	0	1	21								
Parameter	NO PARAMETER																	
Description	<p>This command is used to enter into display inversion mode. This command does not change any other status.</p> <p>(Example)</p> 																	
Restriction	This command has no effect when module is already in inversion on mode.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal display mode</td> </tr> <tr> <td>S/W Reset</td> <td>Normal display mode</td> </tr> <tr> <td>H/W Reset</td> <td>Normal display mode</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Normal display mode	S/W Reset	Normal display mode	H/W Reset	Normal display mode
Status	Default Value																	
Power On Sequence	Normal display mode																	
S/W Reset	Normal display mode																	
H/W Reset	Normal display mode																	
Flow Chart	 <pre> graph TD     A([Display Inversion OFF Mode]) --&gt; B[INVON]     B --&gt; C([Display Inversion ON Mode])     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

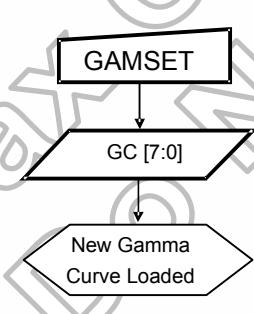
### 5.17.22 All\_Pixel\_Off (22h)

22H	ALLPOFF (All Pixel Off)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	0	0	1	0	22								
Parameter	NO PARAMETER																	
Description	<p>This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command does not change any other status.</p> <p style="text-align: center;">(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <span>memory</span>  <span>display</span> </div> <p>'All Pixels On' or 'Normal Display Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' command.</p>																	
Restriction	This command has no effect when module is already in inversion on mode.																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In or Booster Off</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
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Sleep In or Booster Off	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Normal display mode</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Normal display mode</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Normal display mode</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Normal display mode	S/W Reset	Normal display mode	H/W Reset	Normal display mode
Status	Default Value																	
Power On Sequence	Normal display mode																	
S/W Reset	Normal display mode																	
H/W Reset	Normal display mode																	
Flow Chart	 <pre> graph TD     ND([Normal Display mode]) --&gt; ALLPOFF[ALLPOFF]     ALLPOFF --&gt; BD([Black Display])     </pre> <p><b>Legend</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

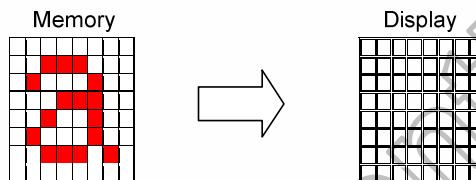
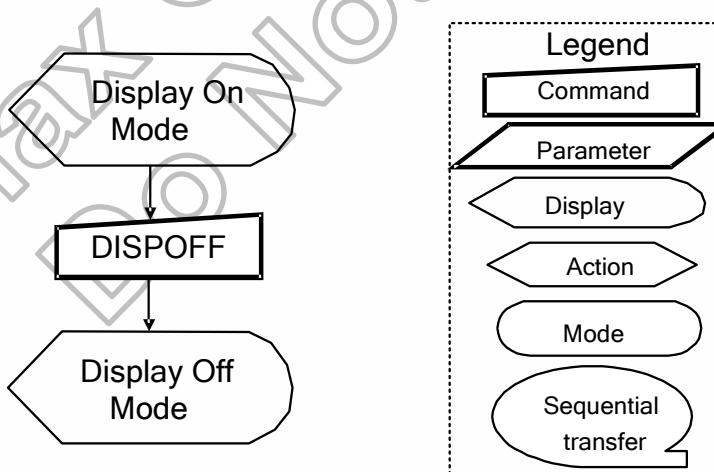
### 5.17.23 All\_Pixel\_On (23h)

23H	ALLPON(All Pixel On)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	0	0	1	1	23								
Parameter	NO PARAMETER																	
Description	<p>This command turns the display panel white in 'Sleep out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command does not change any other status.</p> <p>(Example)</p>  <p>'All Pixels Off' or 'Normal Display Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' command.</p>																	
Restriction	This command has no effect when module is already in inversion on mode.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal display mode</td> </tr> <tr> <td>S/W Reset</td> <td>Normal display mode</td> </tr> <tr> <td>H/W Reset</td> <td>Normal display mode</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Normal display mode	S/W Reset	Normal display mode	H/W Reset	Normal display mode
Status	Default Value																	
Power On Sequence	Normal display mode																	
S/W Reset	Normal display mode																	
H/W Reset	Normal display mode																	
Flow Chart	 <pre> graph TD     ND([Normal Display mode]) --&gt; AP[ALLPON]     AP --&gt; WD([White Display])     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

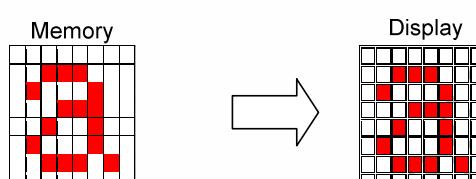
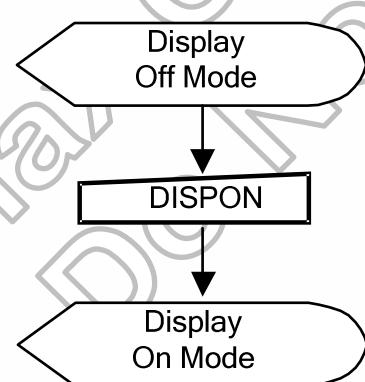
### 5.17.24 Set\_gamma\_curve (26h)

26H	GAMSET (Gamma Set)																								
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	0	0	1	0	0	1	1	0	26															
Parameter	1	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	1..08															
Description	<p>This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:</p> <table border="1"> <thead> <tr> <th>GC[7:0]</th> <th>Parameter</th> <th>Curve selected</th> </tr> </thead> <tbody> <tr> <td>01h</td> <td>GC0</td> <td>Gamma Curve 1</td> </tr> <tr> <td>02h</td> <td>GC1</td> <td>Setting Inhibit</td> </tr> <tr> <td>04h</td> <td>GC2</td> <td>Setting Inhibit</td> </tr> <tr> <td>08h</td> <td>GC3</td> <td>Setting Inhibit</td> </tr> </tbody> </table> <p><b>Note:</b> All other values are undefined.</p>										GC[7:0]	Parameter	Curve selected	01h	GC0	Gamma Curve 1	02h	GC1	Setting Inhibit	04h	GC2	Setting Inhibit	08h	GC3	Setting Inhibit
GC[7:0]	Parameter	Curve selected																							
01h	GC0	Gamma Curve 1																							
02h	GC1	Setting Inhibit																							
04h	GC2	Setting Inhibit																							
08h	GC3	Setting Inhibit																							
Restriction	<p>Values of GC[7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes							
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
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Status	Default Value																								
Power On Sequence	01h																								
S/W Reset	01h																								
H/W Reset	01h																								
Flow Chart	 <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <b>Legend</b> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> </div>																								

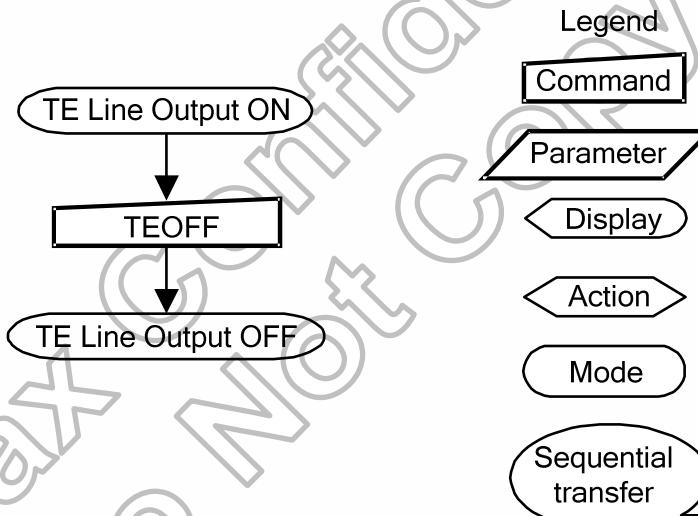
### 5.17.25 Set\_display\_off (28h)

28H	DISPOFF (Display Off)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	1	0	0	0	28								
Parameter	NO PARAMETER																	
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from DPI I/F is disabled and blank page inserted.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p> <p style="text-align: center;">Example</p> 																	
Restriction	This command has no effect when module is already in display off mode.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																	
Power On Sequence	Display off																	
S/W Reset	Display off																	
H/W Reset	Display off																	
Flow Chart	 <pre> graph TD     A([Display On Mode]) --&gt; B[DISPOFF]     B --&gt; C([Display Off Mode])     </pre> <p><b>Legend</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

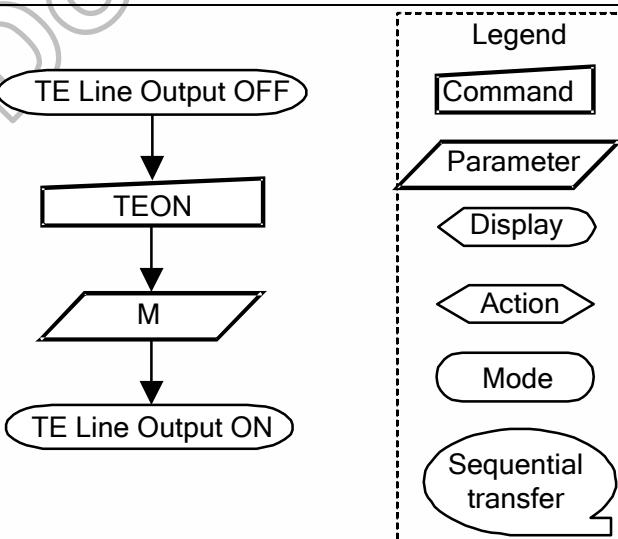
### 5.17.26 Set\_display\_on (29h)

29H	DISPON (Display On)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	1	0	0	1	29								
Parameter	NO PARAMETER																	
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from DPI I/F is enabled.</p> <p>This command does not change any other status.</p> <p>(Example)</p> 																	
Restriction	This command has no effect when module is already in display on mode.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display on</td> </tr> <tr> <td>S/W Reset</td> <td>Display on</td> </tr> <tr> <td>H/W Reset</td> <td>Display on</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display on	S/W Reset	Display on	H/W Reset	Display on
Status	Default Value																	
Power On Sequence	Display on																	
S/W Reset	Display on																	
H/W Reset	Display on																	
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

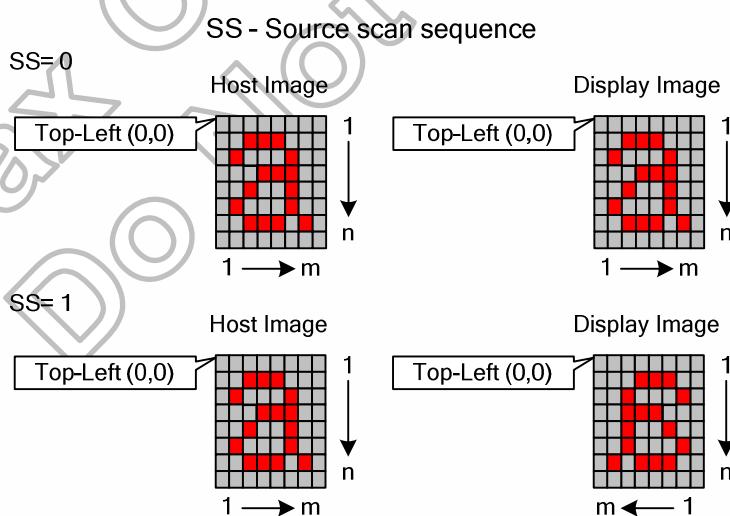
### 5.17.27 Tearing effect line off (34h)

34H	TEOFF (Tearing Effect Line OFF)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	1	0	1	0	0	34								
Parameter	NO PARAMETER																	
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.																	
Restriction	This command has no effect when Tearing Effect output is already OFF.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off
Status	Default Value																	
Power On Sequence	Off																	
S/W Reset	Off																	
H/W Reset	Off																	
Flow Chart	 <pre> graph TD     A([TE Line Output ON]) --&gt; B[TEOFF]     B --&gt; C([TE Line Output OFF]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

### 5.17.28 Set\_tear\_on (35h)

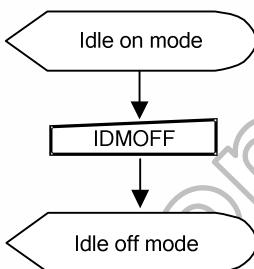
35H	TEON (Tearing Effect Line ON)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	1	0	1	0	1	35								
Parameter	1	X	X	X	X	X	X	X	M	xx								
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).</p> <p>When M=0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p>  <p>Vertical Time Scale</p> <p>When M=1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p>  <p>Vertical Time Scale</p> <p><b>Note:</b> M=1 is not applicable for this project, so it is set to "0".</p>																	
Restriction	This command has no effect when Tearing Effect output is already ON.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off
Status	Default Value																	
Power On Sequence	Off																	
S/W Reset	Off																	
H/W Reset	Off																	
Flow Chart	 <pre> graph TD     A([TE Line Output OFF]) --&gt; B[TEON]     B --&gt; C[M]     C --&gt; D([TE Line Output ON])     </pre> <p><b>Legend</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

### 5.17.29 Set\_address\_mode (36h)

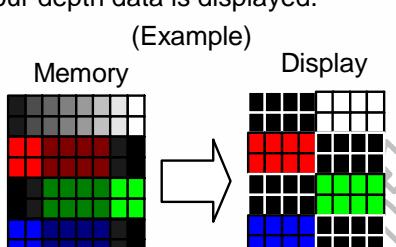
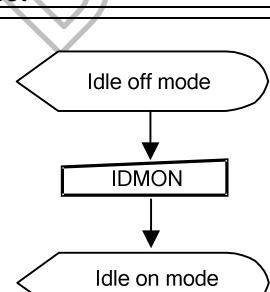
36H	MADCTL (Memory Access Control)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	1	0	1	1	0	36
1 <sup>st</sup> parameter	1	X	X	X	X	B3	X	B1	B0	xx
This command defines the display scanning direction of LCD. This command makes no change on the other driver status.										
Description	Bit Assignment									
	Bit	Name			Description					
	B7	Page Address Order			This bit is not applicable for this project, so it is set to "0".					
	B6	Column Address Order			This bit is not applicable for this project, so it is set to "0".					
	B5	Page/Column Selection			This bit is not applicable for this project, so it is set to "0".					
	B4	Display Device Line Refresh Order			This bit is not applicable for this project, so it is set to "0".					
	B3	RGB-BGR Order (BGR)			Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)					
	B2	Display Data Latch Data Order			This bit is not applicable for this project, so it is set to "0".					
	B1	Flip Horizontal (Source scan sequence)			Select the Source driver scan direction on panel module					
	B0	Flip Vertical (Gate scan sequence)			Select the Gate driver scan direction on panel module					
<p style="text-align: center;">SS - Source scan sequence</p> 										

GS - Gate scan sequence		
GS= 0	Host Image	Display Image
	 Top-Left (0,0)	 Top-Left (0,0)
1 → m      n		
GS= 1	Host Image	Display Image
	 Top-Left (0,0)	 Top-Left (0,0)
1 → m      n      1		
RGB-BGR Order		
B3= 0	Driver IC	Driver IC
	SIG1 SIG2 ..... SIG800	SIG1 SIG2 ..... SIG800
	LCD panel	
Restriction	D7, D6, D5, D4, and D2 of the 1 <sup>st</sup> parameter are set to '0' internally.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	No Change
	H/W Reset	00h
Flow Chart		

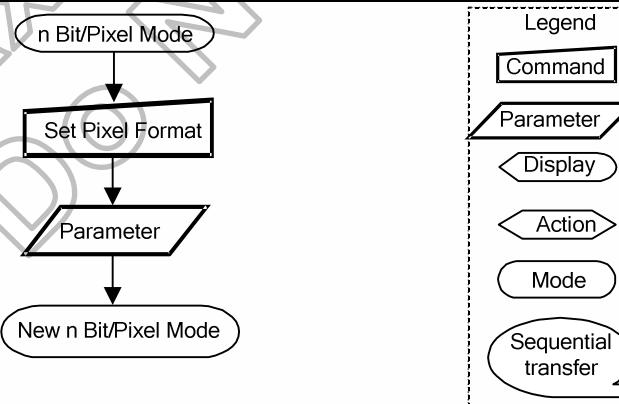
### 5.17.30 Idle mode off (38h)

38H	IDMOFF (Idle mode off)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	1	1	0	0	0	38								
Parameter	NO PARAMETER																	
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colours.																	
Restriction	This command has no effect when module is already in idle off mode.																	
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes								
Status	Availability																	
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Sleep In or Booster Off	Yes																	
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </table>		Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off								
Status	Default Value																	
Power On Sequence	Off																	
S/W Reset	Off																	
H/W Reset	Off																	
Flow Chart	 <pre> graph TD     A([Idle on mode]) --&gt; B[IDMOFF]     B --&gt; C([Idle off mode])   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

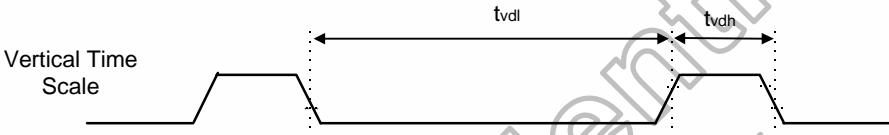
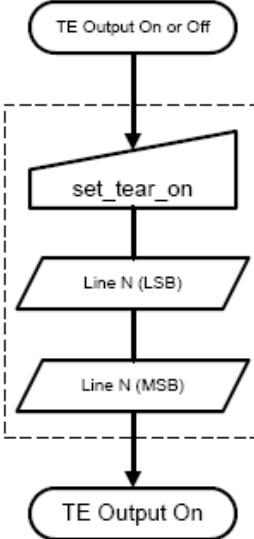
### 5.17.31 Enter\_Idle\_mode (39h)

39H	IDMON (Idle mode on)																																													
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	0	0	1	1	1	0	0	1	39																																				
Parameter	NO PARAMETER																																													
Description	<p>This command is used to enter into Idle mode on. In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B, 8 colour depth data is displayed.</p> <p>(Example)</p>  <p>Display Colour</p> <table border="1"> <thead> <tr> <th></th> <th>R7 – R0</th> <th>G7 – G0</th> <th>B7 – B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Magent</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> </tbody> </table> <p>X=don't care</p>											R7 – R0	G7 – G0	B7 – B0	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magent	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX
	R7 – R0	G7 – G0	B7 – B0																																											
Black	0XXXXX	0XXXXX	0XXXXX																																											
Blue	0XXXXX	0XXXXX	1XXXXX																																											
Red	1XXXXX	0XXXXX	0XXXXX																																											
Magent	1XXXXX	0XXXXX	1XXXXX																																											
Green	0XXXXX	1XXXXX	0XXXXX																																											
Cyan	0XXXXX	1XXXXX	1XXXXX																																											
Yellow	1XXXXX	1XXXXX	0XXXXX																																											
White	1XXXXX	1XXXXX	1XXXXX																																											
Restriction	This command has no effect when module is already in idle on mode.																																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																												
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Status	Default Value																																													
Power On Sequence	Off																																													
S/W Reset	Off																																													
H/W Reset	Off																																													
Flow Chart	 <pre> graph TD     A[Idle off mode] --&gt; B[IDMON]     B --&gt; C[Idle on mode]   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																																													

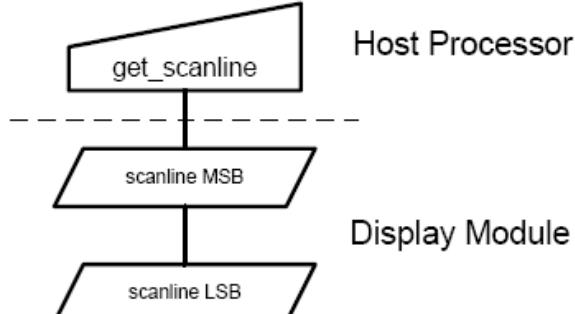
### 5.17.32 Set\_pixel\_format (3Ah)

3A H	COLMOD (Interface Pixel Format)																																													
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	0	0	1	1	1	0	1	0	3A																																				
1 <sup>st</sup> parameter	1	X	D6	D5	D4	X	X	X	X	XX																																				
Description	This command is used to define the format of RGB picture data. D6~D4 : DPI Pixel format Definition. Bits D7, D[3:0] : Reserved. The formats are shown in the table: <table border="1"> <thead> <tr> <th>Pixel Format</th> <th>D6</th> <th>D5</th> <th>D4</th> </tr> </thead> <tbody> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 Bit/Pixel</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 Bit/Pixel</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>24 Bit/Pixel</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> If the setting is not used then the corresponding bits in the parameter returned										Pixel Format	D6	D5	D4	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	Not Defined	0	1	1	Not Defined	1	0	0	16 Bit/Pixel	1	0	1	18 Bit/Pixel	1	1	0	24 Bit/Pixel	1	1	1
Pixel Format	D6	D5	D4																																											
Not Defined	0	0	0																																											
Not Defined	0	0	1																																											
Not Defined	0	1	0																																											
Not Defined	0	1	1																																											
Not Defined	1	0	0																																											
16 Bit/Pixel	1	0	1																																											
18 Bit/Pixel	1	1	0																																											
24 Bit/Pixel	1	1	1																																											
Restriction	There is no visible effect until the image data is written.																																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																												
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Status	Default Value																																													
Power On Sequence	70h																																													
S/W Reset	70h																																													
H/W Reset	70h																																													
Flow Chart	 <pre> graph TD     A([n Bit/Pixel Mode]) --&gt; B[Set Pixel Format]     B --&gt; C[Parameter]     C --&gt; D([New n Bit/Pixel Mode])     style A fill:none,stroke:none     style B fill:none,stroke:none     style C fill:none,stroke:none     style D fill:none,stroke:none     style E fill:#fff,stroke:#000,stroke-width:1px     style F fill:#fff,stroke:#000,stroke-width:1px     style G fill:#fff,stroke:#000,stroke-width:1px     style H fill:#fff,stroke:#000,stroke-width:1px     style I fill:#fff,stroke:#000,stroke-width:1px     style J fill:#fff,stroke:#000,stroke-width:1px     style K fill:#fff,stroke:#000,stroke-width:1px     style L fill:#fff,stroke:#000,stroke-width:1px     style M fill:#fff,stroke:#000,stroke-width:1px     style N fill:#fff,stroke:#000,stroke-width:1px     style O fill:#fff,stroke:#000,stroke-width:1px     style P fill:#fff,stroke:#000,stroke-width:1px     style Q fill:#fff,stroke:#000,stroke-width:1px     style R fill:#fff,stroke:#000,stroke-width:1px     style S fill:#fff,stroke:#000,stroke-width:1px     style T fill:#fff,stroke:#000,stroke-width:1px     style U fill:#fff,stroke:#000,stroke-width:1px     style V fill:#fff,stroke:#000,stroke-width:1px     style W fill:#fff,stroke:#000,stroke-width:1px     style X fill:#fff,stroke:#000,stroke-width:1px     style Y fill:#fff,stroke:#000,stroke-width:1px     style Z fill:#fff,stroke:#000,stroke-width:1px     style AA fill:#fff,stroke:#000,stroke-width:1px     style BB fill:#fff,stroke:#000,stroke-width:1px     style CC fill:#fff,stroke:#000,stroke-width:1px     style DD fill:#fff,stroke:#000,stroke-width:1px     style EE fill:#fff,stroke:#000,stroke-width:1px     style FF fill:#fff,stroke:#000,stroke-width:1px     style GG fill:#fff,stroke:#000,stroke-width:1px     style HH fill:#fff,stroke:#000,stroke-width:1px     style II fill:#fff,stroke:#000,stroke-width:1px     style JJ fill:#fff,stroke:#000,stroke-width:1px     style KK fill:#fff,stroke:#000,stroke-width:1px     style LL fill:#fff,stroke:#000,stroke-width:1px     style MM fill:#fff,stroke:#000,stroke-width:1px     style NN fill:#fff,stroke:#000,stroke-width:1px     style OO fill:#fff,stroke:#000,stroke-width:1px     style PP fill:#fff,stroke:#000,stroke-width:1px     style QQ fill:#fff,stroke:#000,stroke-width:1px     style RR fill:#fff,stroke:#000,stroke-width:1px     style SS fill:#fff,stroke:#000,stroke-width:1px     style TT fill:#fff,stroke:#000,stroke-width:1px     style UU fill:#fff,stroke:#000,stroke-width:1px     style VV fill:#fff,stroke:#000,stroke-width:1px     style WW fill:#fff,stroke:#000,stroke-width:1px     style XX fill:#fff,stroke:#000,stroke-width:1px     style YY fill:#fff,stroke:#000,stroke-width:1px     style ZZ fill:#fff,stroke:#000,stroke-width:1px     style AAA fill:#fff,stroke:#000,stroke-width:1px     style BBB fill:#fff,stroke:#000,stroke-width:1px     style CCC fill:#fff,stroke:#000,stroke-width:1px     style DDD fill:#fff,stroke:#000,stroke-width:1px     style EEE fill:#fff,stroke:#000,stroke-width:1px     style FFF fill:#fff,stroke:#000,stroke-width:1px     style GGG fill:#fff,stroke:#000,stroke-width:1px     style HHH fill:#fff,stroke:#000,stroke-width:1px     style III fill:#fff,stroke:#000,stroke-width:1px     style JJJ fill:#fff,stroke:#000,stroke-width:1px     style KKK fill:#fff,stroke:#000,stroke-width:1px     style LLL fill:#fff,stroke:#000,stroke-width:1px     style MLL fill:#fff,stroke:#000,stroke-width:1px     style NLL fill:#fff,stroke:#000,stroke-width:1px     style OLL fill:#fff,stroke:#000,stroke-width:1px     style PLL fill:#fff,stroke:#000,stroke-width:1px     style QLL fill:#fff,stroke:#000,stroke-width:1px     style RLL fill:#fff,stroke:#000,stroke-width:1px     style SLL fill:#fff,stroke:#000,stroke-width:1px     style TLL fill:#fff,stroke:#000,stroke-width:1px     style ULL fill:#fff,stroke:#000,stroke-width:1px     style VLL fill:#fff,stroke:#000,stroke-width:1px     style WLL fill:#fff,stroke:#000,stroke-width:1px     style XLL fill:#fff,stroke:#000,stroke-width:1px     style YLL fill:#fff,stroke:#000,stroke-width:1px     style ZLL fill:#fff,stroke:#000,stroke-width:1px     style AAQ fill:#fff,stroke:#000,stroke-width:1px     style BBQ fill:#fff,stroke:#000,stroke-width:1px     style CCQ fill:#fff,stroke:#000,stroke-width:1px     style DDQ fill:#fff,stroke:#000,stroke-width:1px     style EEQ fill:#fff,stroke:#000,stroke-width:1px     style FFQ fill:#fff,stroke:#000,stroke-width:1px     style GGQ fill:#fff,stroke:#000,stroke-width:1px     style HHQ fill:#fff,stroke:#000,stroke-width:1px     style IIQ fill:#fff,stroke:#000,stroke-width:1px     style JJQ fill:#fff,stroke:#000,stroke-width:1px     style KKQ fill:#fff,stroke:#000,stroke-width:1px     style LLQ fill:#fff,stroke:#000,stroke-width:1px     style MMQ fill:#fff,stroke:#000,stroke-width:1px     style NNQ fill:#fff,stroke:#000,stroke-width:1px     style OQQ fill:#fff,stroke:#000,stroke-width:1px     style PQQ fill:#fff,stroke:#000,stroke-width:1px     style QQQ fill:#fff,stroke:#000,stroke-width:1px     style RQQ fill:#fff,stroke:#000,stroke-width:1px     style SQQ fill:#fff,stroke:#000,stroke-width:1px     style TQQ fill:#fff,stroke:#000,stroke-width:1px     style UQQ fill:#fff,stroke:#000,stroke-width:1px     style VQQ fill:#fff,stroke:#000,stroke-width:1px     style WQQ fill:#fff,stroke:#000,stroke-width:1px     style XQQ fill:#fff,stroke:#000,stroke-width:1px     style YQQ fill:#fff,stroke:#000,stroke-width:1px     style ZQQ fill:#fff,stroke:#000,stroke-width:1px     style AAU fill:#fff,stroke:#000,stroke-width:1px     style BBU fill:#fff,stroke:#000,stroke-width:1px     style CCU fill:#fff,stroke:#000,stroke-width:1px     style DDU fill:#fff,stroke:#000,stroke-width:1px     style EEU fill:#fff,stroke:#000,stroke-width:1px     style FDU fill:#fff,stroke:#000,stroke-width:1px     style GGU fill:#fff,stroke:#000,stroke-width:1px     style HGU fill:#fff,stroke:#000,stroke-width:1px     style IAU fill:#fff,stroke:#000,stroke-width:1px     style JAU fill:#fff,stroke:#000,stroke-width:1px     style KAU fill:#fff,stroke:#000,stroke-width:1px     style LAU fill:#fff,stroke:#000,stroke-width:1px     style MAU fill:#fff,stroke:#000,stroke-width:1px     style NAU fill:#fff,stroke:#000,stroke-width:1px     style OAU fill:#fff,stroke:#000,stroke-width:1px     style PAU fill:#fff,stroke:#000,stroke-width:1px     style QAU fill:#fff,stroke:#000,stroke-width:1px     style RAU fill:#fff,stroke:#000,stroke-width:1px     style SAU fill:#fff,stroke:#000,stroke-width:1px     style TAU fill:#fff,stroke:#000,stroke-width:1px     style UAU fill:#fff,stroke:#000,stroke-width:1px     style VAU fill:#fff,stroke:#000,stroke-width:1px     style WAU fill:#fff,stroke:#000,stroke-width:1px     style XAU fill:#fff,stroke:#000,stroke-width:1px     style YAU fill:#fff,stroke:#000,stroke-width:1px     style ZAU fill:#fff,stroke:#000,stroke-width:1px     style AAQ fill:#fff,stroke:#000,stroke-width:1px     style BBQ fill:#fff,stroke:#000,stroke-width:1px     style CCQ fill:#fff,stroke:#000,stroke-width:1px     style DDQ fill:#fff,stroke:#000,stroke-width:1px     style EEQ fill:#fff,stroke:#000,stroke-width:1px     style FFQ fill:#fff,stroke:#000,stroke-width:1px     style GGQ fill:#fff,stroke:#000,stroke-width:1px     style HHQ fill:#fff,stroke:#000,stroke-width:1px     style IIQ fill:#fff,stroke:#000,stroke-width:1px     style JJQ fill:#fff,stroke:#000,stroke-width:1px     style KKQ fill:#fff,stroke:#000,stroke-width:1px     style LLQ fill:#fff,stroke:#000,stroke-width:1px     style MMQ fill:#fff,stroke:#000,stroke-width:1px     style NNQ fill:#fff,stroke:#000,stroke-width:1px     style OQQ fill:#fff,stroke:#000,stroke-width:1px     style PQQ fill:#fff,stroke:#000,stroke-width:1px     style QQQ fill:#fff,stroke:#000,stroke-width:1px     style RQQ fill:#fff,stroke:#000,stroke-width:1px     style SQQ fill:#fff,stroke:#000,stroke-width:1px     style TQQ fill:#fff,stroke:#000,stroke-width:1px     style UQQ fill:#fff,stroke:#000,stroke-width:1px     style VQQ fill:#fff,stroke:#000,stroke-width:1px     style WQQ fill:#fff,stroke:#000,stroke-width:1px     style XQQ fill:#fff,stroke:#000,stroke-width:1px     style YQQ fill:#fff,stroke:#000,stroke-width:1px     style ZQQ fill:#fff,stroke:#000,stroke-width:1px     style AAU fill:#fff,stroke:#000,stroke-width:1px     style BBU fill:#fff,stroke:#000,stroke-width:1px     style CCU fill:#fff,stroke:#000,stroke-width:1px     style DDU fill:#fff,stroke:#000,stroke-width:1px     style EEU fill:#fff,stroke:#000,stroke-width:1px     style FDU fill:#fff,stroke:#000,stroke-width:1px     style GGU fill:#fff,stroke:#000,stroke-width:1px     style HGU fill:#fff,stroke:#000,stroke-width:1px     style IAU fill:#fff,stroke:#000,stroke-width:1px     style JAU fill:#fff,stroke:#000,stroke-width:1px     style KAU fill:#fff,stroke:#000,stroke-width:1px     style LAU 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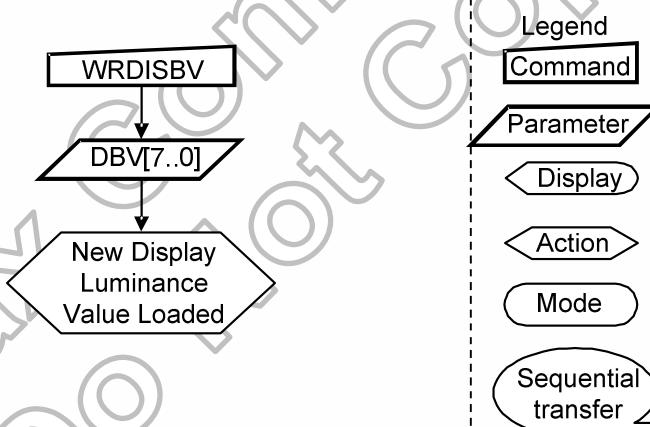
### 5.17.33 Set tear scan lines (44h)

44H	TESL (Tear Effect Scan Lines)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	0	0	1	0	0	44								
1 <sup>st</sup> parameter	1	TELINE[15:8](8'b0)								00..FF								
2 <sup>nd</sup> parameter	1	TELINE[7:0](8'b0)								00..FF								
Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p>  <p>Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.</p>																	
Restriction	The command has no effect when Tearing Effect output is already ON.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
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Status	Default Value																	
Power On Sequence	0000h																	
S/W Reset	0000h																	
H/W Reset	0000h																	
Flow Chart	 <pre> graph TD     A([TE Output On or Off]) --&gt; B[set_tear_on]     B --&gt; C[Line N (LSB)]     C --&gt; D[Line N (MSB)]     D --&gt; E([TE Output On])   </pre>																	

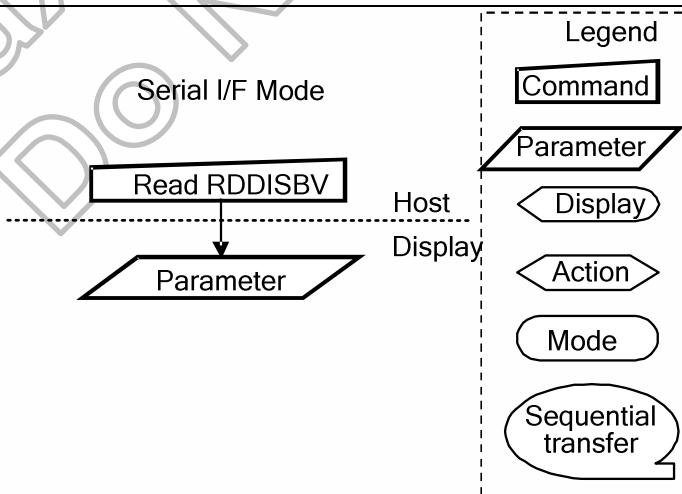
### 5.17.34 Get the current scanline(45h)

45H	GETSCAN (Get the current scanline)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	0	0	1	0	1	45								
1 <sup>st</sup> parameter	1	SLN[15:8](8'b0)								00..FF								
2 <sup>nd</sup> parameter	1	SLN[7:0](8'b0)								00..FF								
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
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Status	Default Value																	
Power On Sequence	0000h																	
S/W Reset	0000h																	
H/W Reset	0000h																	
Flow Chart	 <pre> graph TD     Host[Host Processor] -- "get_scanline" --&gt; DM[Display Module]     DM -- "scanline MSB" --&gt; Host     DM -- "scanline LSB" --&gt; Host   </pre>																	

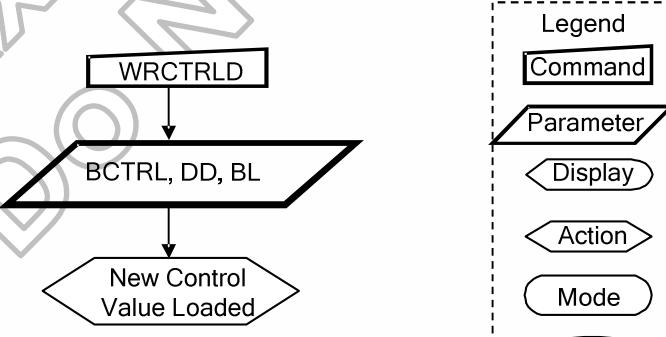
### 5.17.35 Write display brightness (51h)

51H	WRDISBV (Write Display Brightness)																		
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	0	1	0	1	0	0	0	1	51									
1 <sup>st</sup> parameter	1	DBV[7:0]																	
Description	<p>This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification.</p> <p>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>See chapter "5.13.3 Brightness Control Block".</p>																		
Restriction	-																		
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Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	 <pre> graph TD     WRDISBV[WRDISBV] --&gt; DBV[DBV[7..0]]     DBV --&gt; NewDisplay[New Display Luminance Value Loaded]     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																		

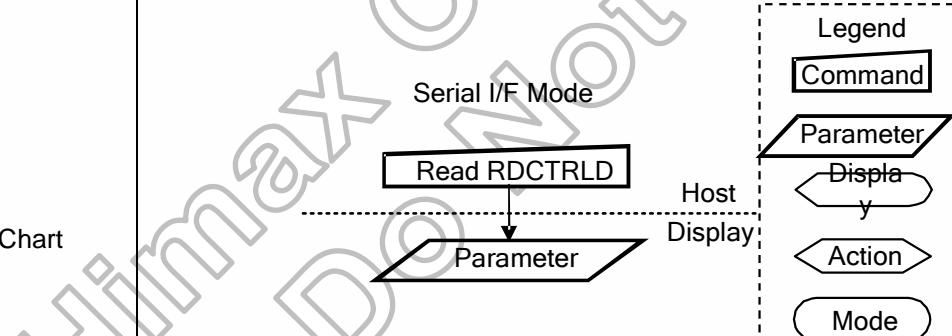
### 5.17.36 Read display brightness value (52h)

52H	RDDISBV (Read Display Brightness Value)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	1	0	0	1	0	52								
1 <sup>st</sup> parameter	1	DBV[7:0]							xx									
Description	<p>This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>See chapters: "5.13.3 Brightness Control Block", and "6.2.33 Write Display Brightness (51h)"</p> <p>DBV[7:0] is reset when display is in sleep-in mode.</p> <p>DBV[7:0] is '00h' when bit BCTRL of "6.2.35 Write CTRL Display (53h)" command is '0'.</p> <p>DBV[7:0] is manual set brightness specified with "6.2.35 Write CTRL Display (53h)" command when bit BCTRL is '1'.</p> <p>When bit BCTRL of "6.2.35 Write CTRL Display (53h)" command is '1' and bit C1/C0 of "6.2.37 Write Content Adaptive Brightness Control (55h)" are '0', DBV[7:0] output is the brightness value specified with "6.2.33 Write Display Brightness (51h)" command.</p>																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	 <p>Serial I/F Mode</p> <p>Read RDDISBV</p> <p>Host Display</p> <p>Parameter</p> <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

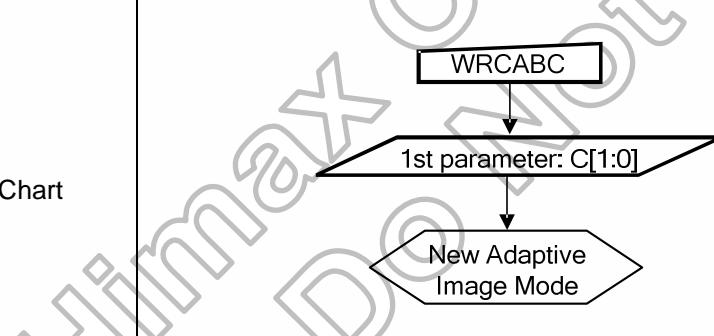
### 5.17.37 Write CTRL display (53h)

53H	WRCTRLD (Write Control Display)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	1	0	0	1	1	53								
1 <sup>st</sup> parameter	1	X	X	BCTRL	X	DD	BL	X	X	00..FF								
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low. ) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don't care.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	 <pre> graph TD     WRCTRLD[WRCTRLD] --&gt; BCTRL[BCTRL, DD, BL]     BCTRL --&gt; NewValue{New Control Value Loaded}   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

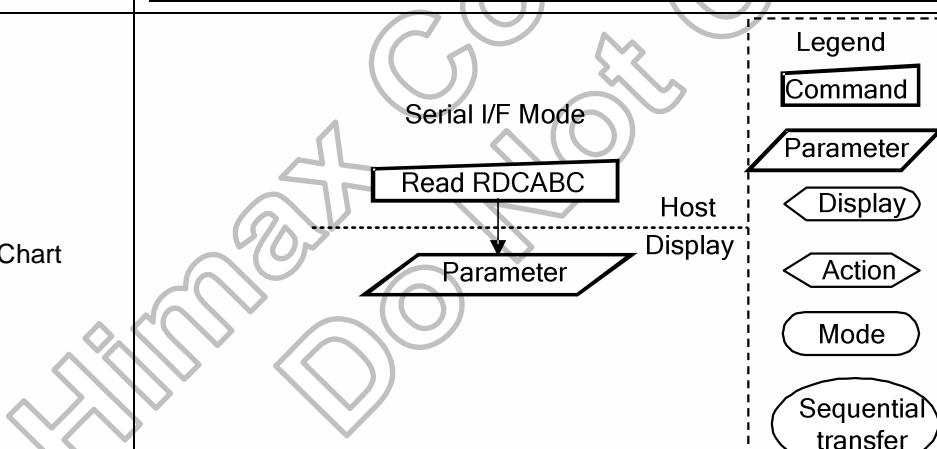
### 5.17.38 Read CTRL value display (54h)

54H	RDCTRLD (Read Control Value Display)																		
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	0	1	0	1	0	1	0	0	54									
1 <sup>st</sup> parameter	1	X	X	BCTRL	X	DD	BL	X	X	xx									
Description	This command returns ambient light and brightness control values, see chapter: "6.2.35 Write CTRL Display (53h)". BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On																		
Restriction	-																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes									
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Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																		

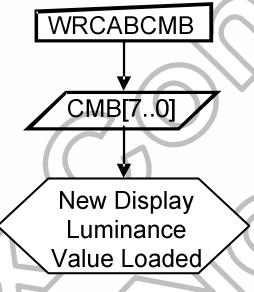
### 5.17.39 Write content adaptive brightness control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)																								
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	0	1	0	1	0	1	0	1	55															
1 <sup>st</sup> parameter	1	X	X	X	X	X	X	CABC[1:0]	xx																
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.13 Content Adaptive Brightness Control (CABC)".</p> <table border="1"> <thead> <tr> <th>C1</th> <th>C0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> </tr> </tbody> </table>										C1	C0	Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
C1	C0	Function																							
0	0	Off																							
0	1	User Interface Image																							
1	0	Still Picture																							
1	1	Moving Image																							
Restriction	-																								
Register Availability			<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes													
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Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	 <pre> graph TD     A[WRCABC] --&gt; B{1st parameter: C[1:0]}     B --&gt; C{New Adaptive Image Mode}   </pre>						<table border="1"> <tr> <td>Legend</td> </tr> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>					Legend	Command	Parameter	Display	Action	Mode	Sequential transfer							
Legend																									
Command																									
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Action																									
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Sequential transfer																									

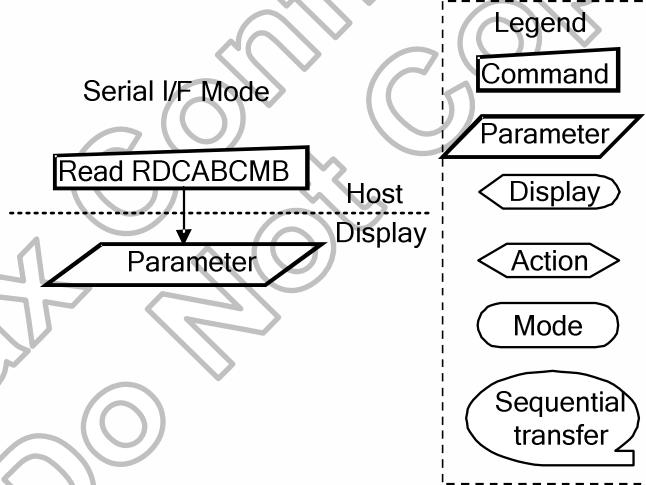
### 5.17.40 Read content adaptive brightness control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	1	1	0	56
1 <sup>st</sup> parameter	1	X	X	X	X	X	X	C1	C0	xx
Description	This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.13 Content Adaptive Brightness Control (CABC)".									
	C1	C0	Function							
	0	0	Off							
	0	1	User Interface Image							
	1	0	Still Picture							
	1	1	Moving Image							
Restriction										
Register Availability			Status		Availability					
	Normal Mode On, Idle Mode Off, Sleep Out		Yes							
	Normal Mode On, Idle Mode On, Sleep Out		Yes							
	Sleep In or Booster Off		Yes							
Default			Status		Default Value					
	Power On Sequence		00h							
	S/W Reset		00h							
	H/W Reset		00h							
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> <li>Command (Solid rectangle)</li> <li>Parameter (Solid parallelogram)</li> <li>Display (Open arrow pointing right)</li> <li>Action (Open arrow pointing left)</li> <li>Mode (Solid rounded rectangle)</li> <li>Sequential transfer (Open oval)</li> </ul>									

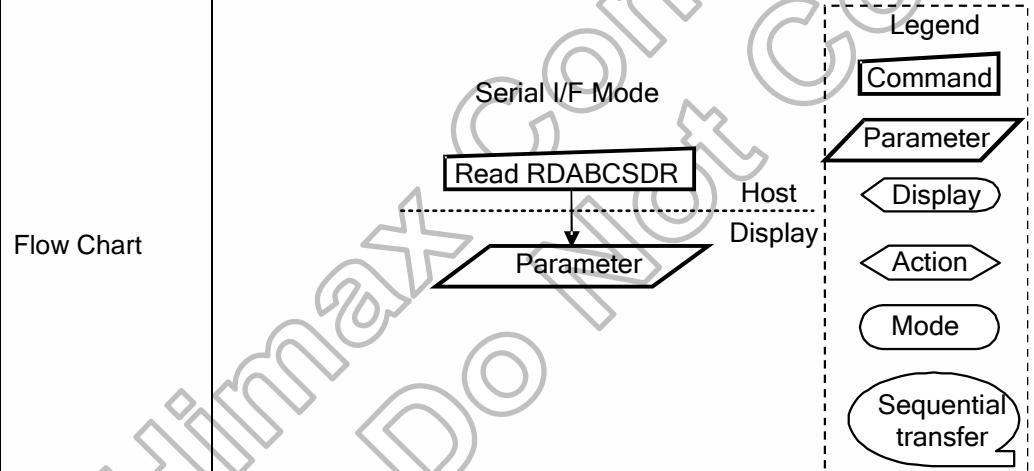
### 5.17.41 Write CABC minimum brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	1	1	1	1	0	5E								
1 <sup>st</sup> parameter	1	CMB[7:0]								00..FF								
Description	<p>This command is used to set the minimum brightness value of the display for CABC function.</p> <p>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.</p> <p>See chapter "5.13.4 Minimum brightness setting of CABC function".</p>																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	 <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <b>Legend</b> <ul style="list-style-type: none"> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px;"></span> Command</li> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px; transform: rotate(45deg);"></span> Parameter</li> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px; border-radius: 50%;"></span> Display</li> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px; border-radius: 50%; border: 1px solid black; border-width: 0 2px 2px 0; border-style: solid; transform: rotate(45deg);"></span> Action</li> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px; border-radius: 50%; border: 1px solid black; border-width: 0 1px 1px 0; transform: rotate(-45deg);"></span> Mode</li> <li><span style="border: 1px solid black; border-radius: 50%; display: inline-block; width: 15px; height: 15px;"></span> Sequential transfer</li> </ul> </div>																	

### 5.17.42 Read CABC minimum brightness (5Fh)

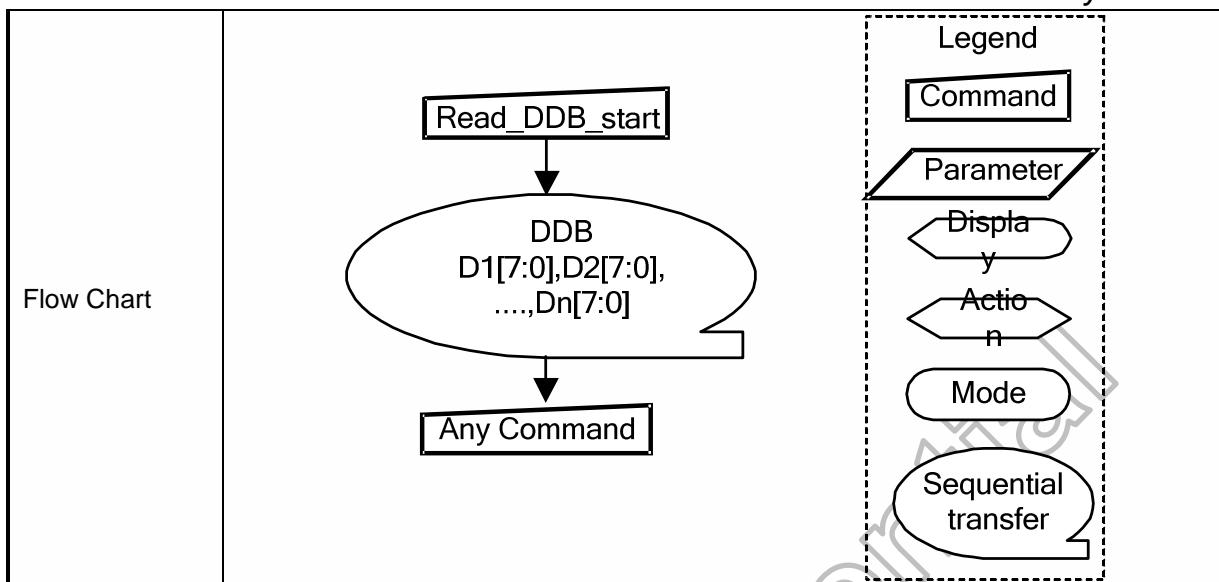
5FH	RDCABCMB (Read CABC minimum brightness)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	1	1	1	1	1	5F								
1 <sup>st</sup> parameter	1	CMB[7:0]								XX								
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter "5.13.4 Minimum brightness setting of CABC function". CMB[7:0] is CABC minimum brightness specified with "6.2.39 Write CABC minimum brightness (5Eh)" command.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
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H/W Reset	00h																	
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

### 5.17.43 Read automatic brightness control self-diagnostic result (68h)

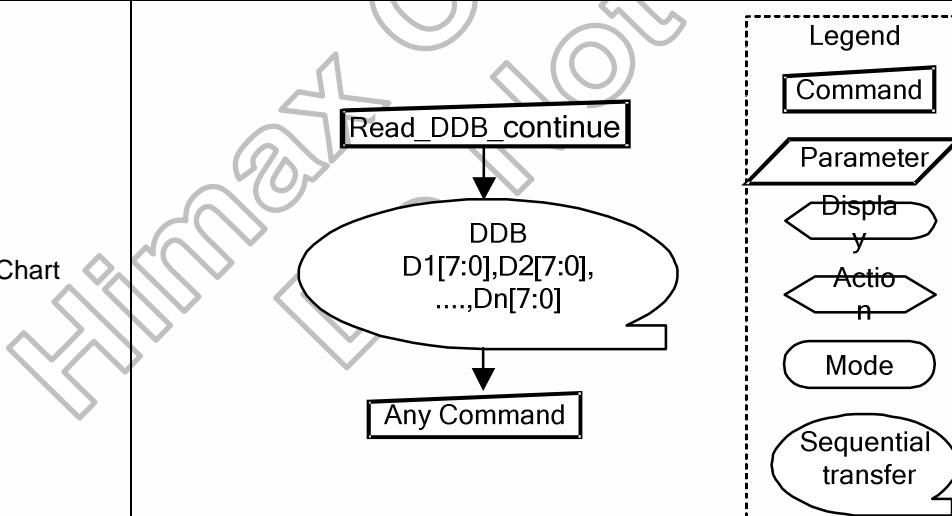
68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	1	0	1	0	0	0	68								
1 <sup>st</sup> parameter	1	D[7:6]	0	0	0	0	0	0	0	xx								
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out –command as described in the table below: Bit D7 – Register Loading Detection. See section “5.10.1 Register loading Detection”. Bit D6 – Functionality Detection. See section “5.10.2 Functionality Detection”. Bits D[5:0] are for future use and are set to ‘0’.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

### 5.17.44 Read\_DDB\_start (A1h)

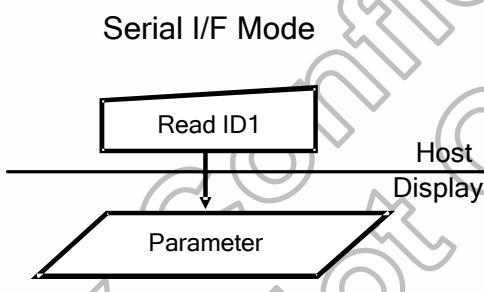
A1H	Read_DDB_start																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	0	1	0	0	0	0	1	A1								
1 <sup>st</sup> parameter	1	xx																
2 <sup>nd</sup> parameter	1	xx																
:	1	xx																
N <sup>th</sup> parameter	1	xx																
Description	<p>This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data.</p> <p>The format of returned data is as follows:</p> <ul style="list-style-type: none"> <li>Parameter 1: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.</li> <li>Parameter 2: MS (most significant) byte of Supplier ID.</li> <li>Parameter 3: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.</li> <li>Parameter 4: MS (most significant) byte of Supplier Elective Data</li> <li>Parameter 5: single-byte <i>Escape or Exit Code</i> (EEC). The code is interpreted as follows: <ul style="list-style-type: none"> <li>- FFh – Exit code – there is no more data in the Descriptor Block</li> <li>- 00h – Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard)</li> <li>- Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in <i>MIPI Alliance Standard for Device Descriptor Block (DDB)</i>.</li> </ul> </li> </ul> <p>DDBs may contain many more data fields providing information about the peripheral.</p> <p>In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command read_DDB_start from host processor to peripheral, which includes the bus turn-around token.</p> <p>The peripheral then takes control of the bus and returns the requested data. The peripheral response to read_DDB_start is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command.</p> <p>The response to a read_DDB_start command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a read_DDB_continue command to access the next portion of the DDB. A read_DDB_continue command begins the next read at the location following the last byte of the previous data read from the DDB.</p> <p>Subsequent read_DDB_continue commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any read_DDB_xxx command.</p>																	
Restrictions	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
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Status	Default Value																	
Power On Sequence	PA1st~4 <sup>th</sup> is OTP value, PA5th is FFh																	
S/W Reset	PA1st~4 <sup>th</sup> is OTP value, PA5th is FFh																	
H/W Reset	PA1st~4 <sup>th</sup> is OTP value, PA5th is FFh																	



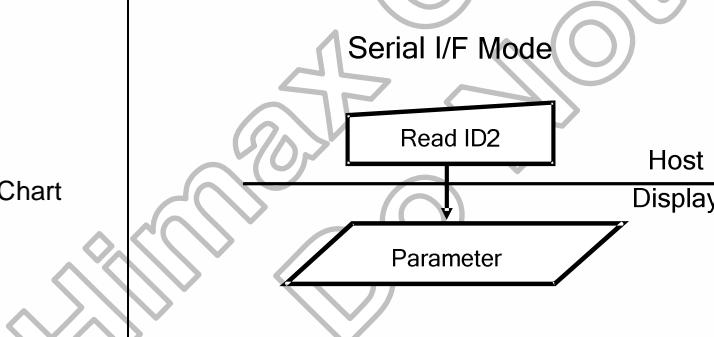
### 5.17.45 Read\_DDB\_continue (A8h)

A8H	Read_DDB_continue									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	1	0	0	0	A8
1 <sup>st</sup> parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2 <sup>nd</sup> parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
:	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
N <sup>th</sup> parameter	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.									
Restrictions	-									
Register Availability	Status		Availability							
	Normal Mode On, Idle Mode Off, Sleep Out		Yes							
	Normal Mode On, Idle Mode On, Sleep Out		Yes							
	Sleep In or Booster Off		Yes							
Default	Status		Default Value							
	Power On Sequence		Without A1h read, 1 <sup>st</sup> ~4 <sup>th</sup> read is the same as A8h 1 <sup>st</sup> ~4 <sup>th</sup> OTP value, after 5 <sup>th</sup> read is FFh.							
	S/W Reset		Without A1h read, 1 <sup>st</sup> ~4 <sup>th</sup> read is the same as A8h 1 <sup>st</sup> ~4 <sup>th</sup> OTP value, after 5 <sup>th</sup> read is FFh.							
	H/W Reset		Without A1h read, 1 <sup>st</sup> ~4 <sup>th</sup> read is the same as A8h 1 <sup>st</sup> ~4 <sup>th</sup> OTP value, after 5 <sup>th</sup> read is FFh.							
Flow Chart	 <pre> graph TD     A[Read_DDB_continue] --&gt; B((DDB D1[7:0], D2[7:0], ..., Dn[7:0]))     B --&gt; C[Any Command]     style B fill:none,stroke:none     style C fill:none,stroke:none     </pre> <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>									

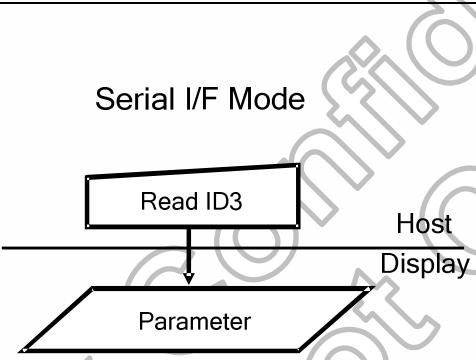
### 5.17.46 Read ID1 (DAh)

DAH	RDID1 (Read ID1)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	1	1	0	1	0	DA								
1 <sup>st</sup> parameter	1	module's manufacturer[7:0]								xx								
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
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Status	Default Value																	
Power On Sequence	OTP value																	
S/W Reset	OTP value																	
H/W Reset	OTP value																	
Flow Chart	<p style="text-align: center;">Serial I/F Mode</p>  <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <b>Legend</b> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> </div>																	

### 5.17.47 Read ID2 (DBh)

DBH	RDID2 (Read ID2)																														
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	1	1	0	1	1	0	1	1	DB																					
1 <sup>st</sup> parameter	1	1	LCD module/driver version [6:0]						xx																						
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table: <table border="1"> <thead> <tr> <th>ID Byte Value V[7:0]</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr> <td>80h</td> <td></td> <td></td> </tr> <tr> <td>81h</td> <td></td> <td></td> </tr> <tr> <td>82h</td> <td></td> <td></td> </tr> <tr> <td>83h</td> <td></td> <td></td> </tr> <tr> <td>84h</td> <td></td> <td></td> </tr> <tr> <td>85h</td> <td></td> <td></td> </tr> </tbody> </table> X= Don't care										ID Byte Value V[7:0]	Version	Changes	80h			81h			82h			83h			84h			85h		
ID Byte Value V[7:0]	Version	Changes																													
80h																															
81h																															
82h																															
83h																															
84h																															
85h																															
Restrictions	-																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes													
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In or Booster Off	Yes																														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP value</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	OTP value	S/W Reset	OTP value	H/W Reset	OTP value													
Status	Default Value																														
Power On Sequence	OTP value																														
S/W Reset	OTP value																														
H/W Reset	OTP value																														
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> <li>Command: Box</li> <li>Parameter: Box</li> <li>Display: Parallelogram</li> <li>Action: Diamond</li> <li>Mode: Oval</li> <li>Sequential transfer: Ellipse</li> </ul>																														

### 5.17.48 Read ID3 (DCh)

DCH	RDID3 (Read ID3)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	1	1	1	0	0	DC								
1 <sup>st</sup> parameter	1	LCD module/driver ID[7:0]								xx								
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.																	
Restrictions	-																	
Register Availability	Status		Availability															
	Normal Mode On, Idle Mode Off, Sleep Out		Yes															
	Normal Mode On, Idle Mode On, Sleep Out		Yes															
	Sleep In or Booster Off		Yes															
Default	Status		Default Value															
	Power On Sequence		OTP value															
	S/W Reset		OTP value															
	H/W Reset		OTP value															
Flow Chart	<p style="text-align: center;">Serial I/F Mode</p>  <pre> graph TD     Host -- "Read ID3" --&gt; Display     Display -- "Parameter" --&gt; Host     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																	

## 5.18 User Define Command Description

### 5.18.1 SETSEQUENCE: Set Sequence (B0h)

B0H	SETSEQUENCE( Set Sequence)																																															
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																						
Command	0	1	0	1	1	0	0	0	0	B0																																						
1 <sup>st</sup> parameter	1	DISP_BIST_EN				-				-																																						
2 <sup>nd</sup> parameter	1	-	-	-	-	-	-	-	OSC_EN	-																																						
3 <sup>rd</sup> parameter	1	-	VSN_EN	VSP_EN	VGL_EN	VGH_EN	VCL_EN	VDDDN_HZ	STB	-																																						
4 <sup>th</sup> parameter	1	-	-	-	-	GON	DTE	D[1:0]		-																																						
Description	<p>This command is used for DCS command auto sequence and manual mode debug use, please don't access this command in initial code.</p> <p>DISP_BIST_EN: Enable Free-running mode by software</p> <p>OSC_EN: Enable internal oscillator, High active.</p> <p>STB: When STB = "1", the HX8394-D enters the standby mode, where all display operation stops, suspend all the internal operations. But the internal R-C oscillator stop or not is determined by OSC_EN bit. To minimize the standby power, please set OSC_EN to 0. During the standby mode, only the following process can be executed.</p> <ul style="list-style-type: none"> <li>a. Exit the Standby mode (STB = "0")</li> <li>b. Enable or disable the oscillation</li> <li>c. Software reset</li> </ul> <p>VDDDN_HZ: Choose external or internal VDDDN power. VDDDN_HZ=0, VDDDN= -2.5V. VDDDN_HZ=1, VDDDN output High-Z. (For external VDDDN.)</p> <p>VCL_EN : ON/OFF the operation of VCL charge pump circuit.</p> <table border="1"> <tr> <td>VCL_EN</td> <td>Operation of VCL charge bump circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>VGH_EN: ON/OFF the operation of VGH charge pump circuit.</p> <table border="1"> <tr> <td>VGH_EN</td> <td>Operation of VGH charge bump circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>VGL_EN : ON/OFF the operation of VGL charge pump circuit.</p> <table border="1"> <tr> <td>VGL_EN</td> <td>Operation of VGL charge bump circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>VSP_EN: ON/OFF the operation of VSP circuit.</p> <table border="1"> <tr> <td>VSP_EN</td> <td>Operation of VSP DC/DC circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>VSN_EN: ON/OFF the operation of VSN circuit.</p> <table border="1"> <tr> <td>VSN_EN</td> <td>Operation of VSN DC/DC circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>D[1:0]: Setting Source driver output</p> <table border="1"> <tr> <td>D1</td> <td>D0</td> <td>Source Output</td> <td>Internal Operations</td> </tr> <tr> <td>0</td> <td>0</td> <td>Halt</td> <td>Halt</td> </tr> </table>										VCL_EN	Operation of VCL charge bump circuit	0	OFF	1	ON	VGH_EN	Operation of VGH charge bump circuit	0	OFF	1	ON	VGL_EN	Operation of VGL charge bump circuit	0	OFF	1	ON	VSP_EN	Operation of VSP DC/DC circuit	0	OFF	1	ON	VSN_EN	Operation of VSN DC/DC circuit	0	OFF	1	ON	D1	D0	Source Output	Internal Operations	0	0	Halt	Halt
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0	OFF																																															
1	ON																																															
D1	D0	Source Output	Internal Operations																																													
0	0	Halt	Halt																																													

	0	1	inhibited	inhibited								
	1	0	V255 or V0	Blanking								
	1	1	Normal	Operate								
GON: GIP control signal enable selection												
		GON	GIP Enable									
		0	GIP Off									
		1	GIP On									
DTE: Source output enable selection												
		DTE	Source Output									
		0	Source output off									
		1	Source output on									
Restrictions	SETEXTC turn on to enable this command.											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability											
Normal Mode On, Idle Mode Off, Sleep Out	Yes											
Normal Mode On, Idle Mode On, Sleep Out	Yes											
Sleep In or Booster Off	Yes											

### 5.18.2 SETPOWER: Set power (B1h)

B1H	SETPOWER( Set power related setting)																																																													
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																				
Command	0	1	0	1	1	0	0	0	1	B1																																																				
1 <sup>st</sup> parameter	1	DSTB	APF_EN	DD_TU	GASVCI_OPT[1:0]		AP[2:0]			-																																																				
2 <sup>nd</sup> parameter	1	-	INT_VCI			VRHP[4:0]				-																																																				
3 <sup>rd</sup> parameter	1	-	DT[1:0]			VRHN[4:0]				-																																																				
4 <sup>th</sup> parameter	1		FS0[3:0](VSP_pumping)			FS1[3:0]				-																																																				
5 <sup>th</sup> parameter	1	EQ_ON	EQ_MIX	EQ_VCL EN			FS2[3:0]			-																																																				
6 <sup>th</sup> parameter	1		VCL[2:0]			BTP[4:0]				-																																																				
7 <sup>th</sup> parameter	1	CLK_O PT[2]	CLK_O PT[1]	CLK_OP T[0]			BTN[4:0]			-																																																				
8 <sup>th</sup> parameter		POWMOD[1:0]							VGHS[8]																																																					
9 <sup>th</sup> parameter	1				VGHS[7:0]					-																																																				
10 <sup>th</sup> parameter	1				VGLS[7:0]					-																																																				
11 <sup>th</sup> parameter	1		XDK[2:0]			BTP_INIT[4:0]				-																																																				
12 <sup>th</sup> parameter	1	DCS[2]	A_DC[2]	-	-		DCDIV[3:0]																																																							
13 <sup>th</sup> parameter	1		DCS[1:0]		DTPS[2:0]		DTNS[2:0]			-																																																				
14 <sup>th</sup> parameter	1		A_DC[1:0]		A_DTP[2:0]		A_DTN[2:0]			-																																																				
15 <sup>th</sup> parameter	1	-	VGL2_E N	-		VGL2S[4:0]				-																																																				
26 <sup>th</sup> parameter	<p>DSTB: Set '1' to enter deep standby mode for saving power in SLPIN mode. User must enter SLPIN mode before enter deep standby mode and leave deep stand by mode before SLOUT.</p> <p>AP[2:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP[2:0] = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.</p> <table border="1"> <thead> <tr> <th>AP[2]</th> <th>AP[1]</th> <th>AP[0]</th> <th>Constant Current of Operational Amplifier</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Stop</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0.5μA</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1.0μA</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1.5μA</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2.0μA</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>2.5μA</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>3.0μA</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>3.5μA</td> </tr> </tbody> </table> <p>GASVCI_OPT[1:0]: Set the threshold voltage of GAS function(APF_EN =1)</p> <table border="1"> <thead> <tr> <th>GASVCI_OPT[1]</th> <th>GASVCI_OPT[0]</th> <th>GAS threshold voltage</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1.73V</td> </tr> <tr> <td>0</td> <td>1</td> <td>2.15V</td> </tr> <tr> <td>1</td> <td>0</td> <td>2.36V</td> </tr> <tr> <td>1</td> <td>1</td> <td>2.58V</td> </tr> </tbody> </table> <p>DD_TU: Set DD_TU="1", VDDD will increase at Sleep In mode.</p> <p>APF_EN: Abnormal power-off detection enable(GAS function). "1": Enable.</p> <p>INT_VCI : Use at External power mode, VCI voltage Setting to VSP voltage.</p> <p>DT[1:0]:Delay time of power on and power off sequence.</p>											AP[2]	AP[1]	AP[0]	Constant Current of Operational Amplifier	0	0	0	Stop	0	0	1	0.5μA	0	1	0	1.0μA	0	1	1	1.5μA	1	0	0	2.0μA	1	0	1	2.5μA	1	1	0	3.0μA	1	1	1	3.5μA	GASVCI_OPT[1]	GASVCI_OPT[0]	GAS threshold voltage	0	0	1.73V	0	1	2.15V	1	0	2.36V	1	1	2.58V
AP[2]	AP[1]	AP[0]	Constant Current of Operational Amplifier																																																											
0	0	0	Stop																																																											
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1	1	0	3.0μA																																																											
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0	0	1.73V																																																												
0	1	2.15V																																																												
1	0	2.36V																																																												
1	1	2.58V																																																												

0	0		5ms
0	1		10ms
1	0		15ms
1	1		20ms

VRHP[4:0]: VSPR regulator output control setting for source data output driving.

VRHP[4:0]					VSPR Voltage
0	0	0	0	0	VPREF
0	0	0	0	1	3.1V
0	0	0	1	0	3.2V
0	0	0	1	1	3.3V
0	0	1	0	0	3.4V
0	0	1	0	1	3.5V
0	0	1	1	0	3.6V
0	0	1	1	1	3.7V
0	1	0	0	0	3.8V
0	1	0	0	1	3.9V
0	1	0	1	0	4.0V
0	1	0	1	1	4.1V
0	1	1	0	0	4.2V
0	1	1	0	1	4.3V
0	1	1	1	0	4.4V
0	1	1	1	1	4.5V
1	0	0	0	0	4.6V
1	0	0	0	1	4.7V
1	0	0	1	0	4.8V
1	0	0	1	1	4.9V
1	0	1	0	0	5.0V
1	0	1	0	1	5.1V
1	0	1	1	0	5.2V
1	0	1	1	1	5.3V
1	1	0	0	0	5.4V
1	1	0	0	1	5.5V
1	1	0	1	0	5.6V
1	1	0	1	1	5.7V
1	1	1	0	0	5.8V
1	1	1	0	1	5.9V
1	1	1	1	0	6.0V
1	1	1	1	1	6.1V

VRHN[4:0]: VSNR regulator output control setting for source data output driving

VRHN[4:0]					VSNR Voltage
0	0	0	0	0	VNREF
0	0	0	0	1	-3.1V
0	0	0	1	0	-3.2V
0	0	0	1	1	-3.3V
0	0	1	0	0	-3.4V
0	0	1	0	1	-3.5V
0	0	1	1	0	-3.6V
0	0	1	1	1	-3.7V
0	1	0	0	0	-3.8V
0	1	0	0	1	-3.9V
0	1	0	1	0	-4.0V
0	1	0	1	1	-4.1V
0	1	1	0	0	-4.2V
0	1	1	0	1	-4.3V
0	1	1	1	0	-4.4V
0	1	1	1	1	-4.5V
1	0	0	0	0	-4.6V

1	0	0	0	1	-4.7V
1	0	0	1	0	-4.8V
1	0	0	1	1	-4.9V
1	0	1	0	0	-5.0V
1	0	1	0	1	-5.1V
1	0	1	1	0	-5.2V
1	0	1	1	1	-5.3V
1	1	0	0	0	-5.4V
1	1	0	0	1	-5.5V
1	1	0	1	0	-5.6V
1	1	0	1	1	-5.7V
1	1	1	0	0	-5.8V
1	1	1	0	1	-5.9V
1	1	1	1	0	-6.0V
1	1	1	1	1	-6.1V

FS0[3:0]: Set the operating frequency of the step-up circuit for VSP voltage generation.  
(Fosc\_pump=5MHz)

FS0[3]	FS0[2]	FS0[1]	FS0[0]	Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/2
0	0	0	1	Fosc_pump/4
0	0	1	0	Fosc_pump/8
0	0	1	1	Fosc_pump/16
0	1	0	0	Fosc_pump/32
0	1	0	1	Fosc_pump/48
0	1	1	0	Fosc_pump/64
0	1	1	1	Fosc_pump/80
1	0	0	0	Fosc_pump/96
1	0	0	1	Fosc_pump/112
1	0	1	0	Fosc_pump/128
1	0	1	1	Fosc_pump/144
1	1	0	0	Fosc_pump/160
1	1	0	1	Fosc_pump/176
1	1	1	0	Fosc_pump/192
1	1	1	1	Fosc_pump/208

FS1[3:0]: Set the operating frequency of the step-up circuit for VGH & VGL voltage generation. (Fosc\_pump=5MHz)

FS1[3]	FS1[2]	FS1[1]	FS1[0]	Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/32
0	0	0	1	Fosc_pump/64
0	0	1	0	Fosc_pump/96
0	0	1	1	Fosc_pump/128
0	1	0	0	Fosc_pump/160
0	1	0	1	Fosc_pump/192
0	1	1	0	Fosc_pump/224
0	1	1	1	Fosc_pump/256
1	0	0	0	Hsync*4
1	0	0	1	Hsync*2
1	0	1	0	Hsync
1	0	1	1	Hsync/2
1	1	0	0	Hsync/4
1	1	0	1	Hsync/8
1	1	1	0	Hsync/16
1	1	1	1	Inhibited

FS2[3:0]: Adjust the charge pump frequency of internal VCL. (Fosc\_pump=5MHz)

FS2[3]	FS2[2]	FS2[1]	FS2[0]	Operation Frequency of Step-up Circuit
0	0	0	0	Fosc_pump/32

0	0	0	1	Fosc_pump/64
0	0	1	0	Fosc_pump/96
0	0	1	1	Fosc_pump/128
0	1	0	0	Fosc_pump/160
0	1	0	1	Fosc_pump/192
0	1	1	0	Fosc_pump/224
0	1	1	1	Fosc_pump/256
1	0	0	0	Hsync*4
1	0	0	1	Hsync*2
1	0	1	0	Hsync
1	0	1	1	Hsync/2
1	1	0	0	Hsync/4
1	1	0	1	Hsync/8
1	1	1	0	Hsync/16
1	1	1	1	Inhibited

EQ\_ON/ EQ\_MIX: :

EQ_ON	0	0	1	1
EQ_MIX	0	1	0	1
EQ to VCI/VCL	Sharing mode	Frist line EQ	All line EQ	All line EQ

EQ\_VCLEN: VCL enable bit.0: disable(sharing mode), 1:enable(VCL level)

VCL[2:0]: Set the power level of VCL voltage.

VCL[2]	VCL[1]	VCL[0]	VCL Voltage
0	0	0	-2.5V
0	0	1	-2.6V
0	1	0	-2.7V
0	1	1	-2.8V
1	0	0	-2.9V
1	0	1	-3V
1	1	0	-3.1V
1	1	1	-VDD3

BTP[4:0]: Switch the output factor for DC/DC circuit for VSP voltage generation. The LCD drive voltage level VSP can be selected according to the characteristic of liquid crystal which panel used.

BTP[4]	BTP[3]	BTP[2]	BTP[1]	BTP[0]	VSP Voltage
0	0	0	0	0	3.00V
0	0	0	0	1	3.15V
0	0	0	1	0	3.30V
0	0	0	1	1	3.45V
0	0	1	0	0	3.60V
:					:
1	0	0	0	0	5.40V
1	0	0	0	1	5.55V
1	0	0	1	0	5.70V
1	0	0	1	1	5.85V
1	0	1	0	0	6.00V
1	0	1	0	1	6.15V
1	0	1	1	0	6.30V
1	0	1	1	1	6.45V
1	1	0	0	0	6.60V
Others					Inhibited

BTN[4:0]: Switch the output factor of DC/DC circuit for VSN voltage generation. The LCD drive voltage level VSN can be selected according to the characteristic of liquid crystal which panel used.

BTN4	BTN3	BTN2	BTN1	BTN0	VSN Voltage
0	0	0	0	0	-3.00V
0	0	0	0	1	-3.15V
0	0	0	1	0	-3.30V
0	0	0	1	1	-3.45V
0	0	1	0	0	-3.60V
:				:	
1	0	0	0	0	-5.40V
1	0	0	0	1	-5.55V
1	0	0	1	0	-5.70V
1	0	0	1	1	-5.85V
1	0	1	0	0	-6.00V
1	0	1	0	1	-6.15V
1	0	1	1	0	-6.30V
1	0	1	1	1	-6.45V
1	1	0	0	0	-6.60V
Others				Inhibited	

CLK\_OPT0: The pumping clock of VGH will reset with Hsync when CLK\_OPT0 = 1.

CLK\_OPT1: The pumping clock of VCL will reset with Hsync when CLK\_OPT1 = 1.

CLK\_OPT2: The pumping clock of VGL will reset with Hsync when CLK\_OPT2 = 1.

**POWMOD[1:0]:**

POWMOD[1]	POWMOD[0]	Power Mode
0	0	PFM Type A
0	1	PFM Type C
1	0	HX5186
1	1	HX5186

VGHS[8:6]: Specify the VGH voltage source.

VGHS8	VGHS7	VGHS6	VGH Voltage
0	0	0	VSP+VDD3
0	0	1	2*VSP
0	1	0	VSP-VSN+VDD3
0	1	1	2*VSP -VSN
1	0	0	VDD3-VSN+VSP-VSN
1	0	1	2*(VSP-VSN)
1	1	0	inhibited
1	1	1	inhibited

VGHS[5:0]: VGH regulator output voltage setting. The LCD drive voltage level VGH can be selected according to the characteristic of liquid crystal which panel used.

VGHS[5]	VGHS[4]	VGHS[3]	VGHS[2]	VGHS[1]	VGHS[0]	VGH Voltage
0	0	0	0	0	0	7.0V
0	0	0	0	0	1	7.2V
0	0	0	0	1	0	7.4V
0	0	0	0	1	1	7.6V
:						:
1	0	0	1	0	0	14.2V
:						:
1	1	1	1	0	1	19.2V
1	1	1	1	1	0	19.4V
1	1	1	1	1	1	19.6V

VGLS[7:6]: Specify the VGL voltage source.

VGLS[7]	VGLS[6]	VGL Voltage

0	0	VSN-VDD3
0	1	VSN-VSP
1	0	2*VSN-VDD3
1	1	2*VSN-VSP

VGLS[5:0]: VGL regulator output voltage setting. The LCD drive voltage level VGL can be selected according to the characteristic of liquid crystal which panel used.

VGLS[5]	VGLS[4]	VGLS[3]	VGLS[2]	VGLS[1]	VGLS[0]	VGL Voltage
0	0	0	0	0	0	-6.0V
0	0	0	0	0	1	-6.2V
0	0	0	0	1	0	-6.4V
0	0	0	0	1	1	-6.6V
:						:
1	0	0	1	0	0	-13.2V
:						:
1	1	0	0	0	0	-15.6V
1	1	0	0	0	1	-15.8V
1	1	0	0	1	0	-16.0V
Others						Inhibited

VGL2S\_EN: Turn on the DC/DC circuit for VGL2 voltage generation.

VGL2S[4:0]: Switch the output factor for DC/DC circuit for VGL2 voltage generation. The LCD drive voltage level VGL2 can be selected according to the characteristic of liquid crystal which panel used.

Dec.	VGL2S[4]	VGL2S[3]	VGL2S[2]	VGL2S[1]	VGL2S[0]	VGL2
0	0	0	0	0	0	-5.000
1	0	0	0	0	1	-5.200
2	0	0	0	1	0	-5.400
3	0	0	0	1	1	-5.600
4	0	0	1	0	0	-5.800
5	0	0	1	0	1	-6.000
6	0	0	1	1	0	-6.200
7	0	0	1	1	1	-6.400
8	0	1	0	0	0	-6.600
9	0	1	0	0	1	-6.800
10	0	1	0	1	0	-7.000
11	0	1	0	1	1	-7.200
12	0	1	1	0	0	-7.400
13	0	1	1	0	1	-7.600
14	0	1	1	1	0	-7.800
15	0	1	1	1	1	-8.000
16	1	0	0	0	0	-8.200
17	1	0	0	0	1	-8.400
18	1	0	0	1	0	-8.600
19	1	0	0	1	1	-8.800
20	1	0	1	0	0	-9.000
21	1	0	1	0	1	-9.200
22	1	0	1	1	0	-9.400
23	1	0	1	1	1	-9.600
24	1	1	0	0	0	-9.800
25	1	1	0	0	1	-10.000
26	1	1	0	1	0	-10.200
27	1	1	0	1	1	-10.400
28	1	1	1	0	0	-10.600
29	1	1	1	0	1	-10.800
30	1	1	1	1	0	-11.000
31	1	1	1	1	1	Inhibited

XDK[2:0]: Setting charge pump mode of VSP Voltage

XDK[2]	XDK[1]	XDK[0]	VSP
--------	--------	--------	-----

0	0	0	inhibit
0	0	1	X2
0	1	0	X1.5
0	1	1	inhibit
1	0	0	inhibit
1	0	1	inhibit
1	1	0	X3
1	1	1	X3

BTP\_INIT[4:0]: VSP first step power on voltage.

DCDIV[3:0]: Set the normal operate frequency FoscD of DC/DC converter circuit during normal mode.  
(Fosc=40MHz)

DCDIV[3:0]				Normal operate frequency of DC/DC converter(foscD)
0	0	0	0	Fosc/1
0	0	0	1	Fosc/2
0	0	1	0	Fosc/3
0	0	1	1	Fosc/4
0	1	0	0	Fosc/5
0	1	0	1	Fosc/6
0	1	1	0	Fosc/7
0	1	1	1	Fosc/8
1	0	0	0	Fosc/9
1	0	0	1	Fosc/10
1	0	1	0	Fosc/11
1	0	1	1	Fosc/12
1	1	0	0	Fosc/13
1	1	0	1	Fosc/14
1	1	1	0	Fosc/15
1	1	1	1	Fosc/16

DCS[2:0]: Set the soft start operating frequency of DC/DC clock for the internal DC/DC circuit

DTPS[2:0]: Set the soft start operating duty cycle of DC/DC circuit. (PFM DC/DC circuit).  
1 duty cycle = 1 foscD clock

DTPS[2]	DTPS[1]	DTPS[0]	Soft start operating duty cycle of DC/DC circuit
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTNS[2:0]: Set the soft start operating duty cycle of DC/DC circuit. (PFM DC/DC circuit).

1 duty cycle = 1 foscD clock

DTNS[2]	DTNS[1]	DTNS[0]	Soft start operating duty cycle of DC/DC circuit
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7

1	1	1	8
---	---	---	---

**A\_DC[2:0]:**

For PFM circuit: Set the operating frequency of DC/DC clock for the internal DC/DC circuit  
 When using the higher frequency, the driving ability of the DC/DC circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption. No use for HX5186-A/B/C design.

DC[2]	DC[1]	DC[0]	Operation Frequency of DC/DC Clock
0	0	0	foscD/4
0	0	1	foscD/5
0	1	0	foscD/6
0	1	1	foscD/7
1	0	0	foscD/8
1	0	1	foscD/10
1	1	0	foscD/11
1	1	1	foscD/12

**A\_DTP[2:0]:**

For PFM circuit: Set the operating duty cycle of DC/DC clock for VSP.  
 (PCCS[1:0]=0X)

1 duty cycle = 1 foscD clock

DTP[2]	DTP[1]	DTP[0]	Operation Duty Cycle of DC/DC Clock for VSP Generation
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

**A\_DTN[2:0]:**

For PFM circuit: Set the operating duty cycle of DC/DC clock for VSN.  
 (PCCS[1:0]=0X)

1 duty cycle = 1 foscD clock

DTN[2]	DTN[1]	DTN[0]	Operation Duty Cycle of DC/DC Clock for VSN Generation
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

	<table border="1"> <tr> <td colspan="2">VSP/VSN Phase</td><td colspan="2">VSP/VSN Phase</td><td colspan="2">VSP/VSN Phase</td></tr> <tr> <td>Charging Phase</td><td>Pumping Phase</td><td>Charging Phase</td><td>Pumping Phase</td><td>Charging Phase</td><td>Pumping Phase</td></tr> <tr> <td colspan="2">           DTP[2:0]            DTN[2:0]         </td><td colspan="2">           DTP[2:0]            DTN[2:0]         </td><td colspan="2"></td></tr> <tr> <td colspan="2">DC[2:0]</td><td colspan="2" rowspan="3">DC[2:0]</td><td colspan="2" rowspan="3"></td></tr> </table>						VSP/VSN Phase		VSP/VSN Phase		VSP/VSN Phase		Charging Phase	Pumping Phase	Charging Phase	Pumping Phase	Charging Phase	Pumping Phase	DTP[2:0] DTN[2:0]		DTP[2:0] DTN[2:0]				DC[2:0]		DC[2:0]			
VSP/VSN Phase		VSP/VSN Phase		VSP/VSN Phase																										
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DTP[2:0] DTN[2:0]		DTP[2:0] DTN[2:0]																												
DC[2:0]		DC[2:0]																												
26 <sup>th</sup> parameter	SETEXTC turn on to enable this command.																													
Description	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>						Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																
Status	Availability																													
Normal Mode On, Idle Mode Off, Sleep Out	Yes																													
Normal Mode On, Idle Mode On, Sleep Out	Yes																													
Sleep In or Booster Off	Yes																													

### 5.18.3 SETDISP: Set display related register (B2h)

B2H	SETDISP( Set display related register)																																																																																					
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																												
Command	0	1	0	1	1	0	0	1	0	B2																																																																												
1 <sup>st</sup> parameter	1	ZZ_LR	ZZ_EO	NW_PE[2:0]			NW[2:0]																																																																															
2 <sup>nd</sup> parameter	1			NL[7:0]																																																																																		
3 <sup>rd</sup> parameter	1			BP [7:0]																																																																																		
4 <sup>th</sup> parameter	1			FP [7:0]																																																																																		
5 <sup>th</sup> parameter		SAP[3:0]			OSC_T URBO	RES_SEL[2:0]				-																																																																												
6 <sup>th</sup> parameter	1			RTN[7:0]																																																																																		
7 <sup>th</sup> parameter				BP_PE[7:0]																																																																																		
8 <sup>th</sup> parameter	1			FP_PE[7:0]																																																																																		
9 <sup>th</sup> parameter	1			RTN_PE[7:0]																																																																																		
Description	This command is used to set display related register																																																																																					
	ZZ_LR: Zig-zag Left / Right mode selection.																																																																																					
	<table border="1"> <tr> <td>ZZ_LR</td><td>Zig-zag Left / Right mode selection</td></tr> <tr> <td>0</td><td>S1~SR1</td></tr> <tr> <td>1</td><td>SL1~S2400</td></tr> </table>										ZZ_LR	Zig-zag Left / Right mode selection	0	S1~SR1	1	SL1~S2400																																																																						
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ZZ_EO: Zig-zag Odd / Even mode selection.																																																																																						
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NW[2:0]: Inversion type setting.																																																																																						
NW_PE[2:0]: Inversion type setting on partial idle mode.																																																																																						
<table border="1"> <tr> <td>NW2</td><td>NW1</td><td>NW0</td><td>Inversion type</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>Column inversion</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1-dot inversion</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>2-dot inversion</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>4-dot inversion</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>8-dot inversion</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>Inhibited : keep for zig-zag</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>Pixel-column inversion</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>Inhibited</td></tr> </table>										NW2	NW1	NW0	Inversion type	0	0	0	Column inversion	0	0	1	1-dot inversion	0	1	0	2-dot inversion	0	1	1	4-dot inversion	1	0	0	8-dot inversion	1	0	1	Inhibited : keep for zig-zag	1	1	0	Pixel-column inversion	1	1	1	Inhibited																																									
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RES_SEL: X Resolution selection.																																																																																						
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Others					inhibited																																																																																	
NL[7:0]: Setting the number of lines to drive the LCD at an interval of 8 lines. The number of lines must be the same or more than the number of lines necessary for the size of the liquid																																																																																						

NL[7:0]									Line
0	0	0	0	0	0	0	0	0	480
0	0	0	0	0	0	0	0	1	488
0	0	0	0	0	0	1	0	0	496
0	0	0	0	0	0	0	1	1	504
...									...
...									...
0	1	0	1	0	0	1	0	0	1136
...									...
0	1	1	0	0	1	0	0	0	1280
...									...
1	0	1	1	0	1	0	0	0	1920
Others									Inhibited

BP[7:0] : Specify the amount of scan line for back porch(BP).

FP[7:0]: Specify the amount of scan line for front porch (FP).

BP\_PE[7:0]: Specify the amount of scan line for front porch (BP) on idle mode.

FP\_PE[7:0]: Specify the amount of scan line for front porch (FP) on idle mode.

RTN[7:0]: A cycle time of line width.

RTN\_PE[7:0]: A cycle time of line width on idle mode.

Need to set RTN equal to the time of line width

RTN[7:0]/ RTN_PE[7:0]	Clock per Line	
	clock numbers	time
8h'00	400 clocks	10 us
8h'01	404 clocks	10.1 us
8h'02	408 clocks	10.2 us
8h'03	412 clocks	10.3 us
...	...	...
8h'23	540 clocks	13.5 us
...	...	...
8'hFD	1412 clocks	35.3 us
8'hFE	1416 clocks	35.4 us
8'hFF	1440 clocks	35.5 us

SAP[3:0]: Set Current of Operational Amplifier for source driver

SAP\_PE[3:0]: Set Current of Operational Amplifier on idle mode

SAP3	SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
SAP_PE3	SAP_PE2	SAP_PE1	SAP_PE0	
0	0	0	0	1 * Iref
0	0	0	1	2 * Iref
0	0	1	0	3 * Iref
0	0	1	1	4 * Iref
0	1	0	0	5 * Iref
0	1	0	1	6 * Iref
0	1	1	0	7 * Iref
0	1	1	1	8 * Iref
.....				.....
1	1	1	1	16 * Iref

Restrictions SETEXTC turn on to enable this command

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

### 5.18.4 SETCYC: Set display waveform cycles (B4h)

B4H	SETCYC(Set panel driving timing)																																																							
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																														
Command	0	1	0	1	1	0	1	0	0	B4																																														
1 <sup>st</sup> parameter	1									-																																														
2 <sup>nd</sup> parameter	1									-																																														
3 <sup>rd</sup> parameter	1									-																																														
4 <sup>th</sup> parameter	1									-																																														
5 <sup>th</sup> parameter	1									-																																														
6 <sup>th</sup> parameter	1									-																																														
7 <sup>th</sup> parameter	1									-																																														
8 <sup>th</sup> parameter	1									-																																														
9 <sup>th</sup> parameter	1									-																																														
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21 <sup>th</sup> parameter	1									-																																														
22 <sup>th</sup> parameter	1									-																																														
Description	<p>This command is used to set display waveform cycles.</p> <p>GEN_ON[7:0]: Gamma OP turned on timing and in-house function not open.</p> <p>GEN_OFF[7:0]: Gamma OP turned off timing and in-house function not open.</p> <p>SPON[7:0]: Fine tune the Start and End signal delay from original starting point.</p> <table border="1"> <thead> <tr> <th>SPON[7:0]</th> <th>Start / END signal output start delay</th> </tr> </thead> <tbody> <tr> <td>0x00h</td> <td>0 x OSC CLK</td> </tr> <tr> <td>0x01h</td> <td>4 x OSC CLK</td> </tr> <tr> <td>0x02h</td> <td>8 x OSC CLK</td> </tr> <tr> <td>0x03h</td> <td>12 x OSC CLK</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0xFEh</td> <td>1016 OSC CLK</td> </tr> <tr> <td>0xFFh</td> <td>1020 OSC CLK</td> </tr> </tbody> </table> <p><b>Note:</b> When output Start / End signal width is 1- Hsync only, set SPON[7:0] &lt; SPOFF[7:0]</p> <p>SPOFF[7:0]: Fine tune the Start and End signal ending point.</p> <table border="1"> <thead> <tr> <th>SPON[7:0]</th> <th>Start / END signal output end delay</th> </tr> </thead> <tbody> <tr> <td>0x00h</td> <td>0 x OSC CLK</td> </tr> <tr> <td>0x01h</td> <td>4 x OSC CLK</td> </tr> <tr> <td>0x02h</td> <td>8 x OSC CLK</td> </tr> <tr> <td>0x03h</td> <td>12 x OSC CLK</td> </tr> <tr> <td>0x04h</td> <td>16 x OSC CLK</td> </tr> <tr> <td>0x05h</td> <td>20 x OSC CLK</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0xFEh</td> <td>1016 x OSC CLK</td> </tr> <tr> <td>0xFFh</td> <td>1020 x OSC CLK</td> </tr> </tbody> </table> <p>CON/CON1[7:0]: Fine tune the Clock signal delay from original starting point.</p> <table border="1"> <thead> <tr> <th>CON[7:0]</th> <th>Clock signal output start delay</th> </tr> </thead> <tbody> <tr> <td>0x00h</td> <td>0 x OSC CLK</td> </tr> <tr> <td>0x01h</td> <td>4 x OSC CLK</td> </tr> <tr> <td>0x02h</td> <td>8 x OSC CLK</td> </tr> <tr> <td>0x03h</td> <td>12 x OSC CLK</td> </tr> </tbody> </table>										SPON[7:0]	Start / END signal output start delay	0x00h	0 x OSC CLK	0x01h	4 x OSC CLK	0x02h	8 x OSC CLK	0x03h	12 x OSC CLK	...	...	0xFEh	1016 OSC CLK	0xFFh	1020 OSC CLK	SPON[7:0]	Start / END signal output end delay	0x00h	0 x OSC CLK	0x01h	4 x OSC CLK	0x02h	8 x OSC CLK	0x03h	12 x OSC CLK	0x04h	16 x OSC CLK	0x05h	20 x OSC CLK	...	...	0xFEh	1016 x OSC CLK	0xFFh	1020 x OSC CLK	CON[7:0]	Clock signal output start delay	0x00h	0 x OSC CLK	0x01h	4 x OSC CLK	0x02h	8 x OSC CLK	0x03h	12 x OSC CLK
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0xFFh	1016 OSC CLK
0xFFh	1020 OSC CLK

Note: When output Clock signal width is 1- Hsync only, set COFF[7:0]  $\geq$  CON[7:0] + 2

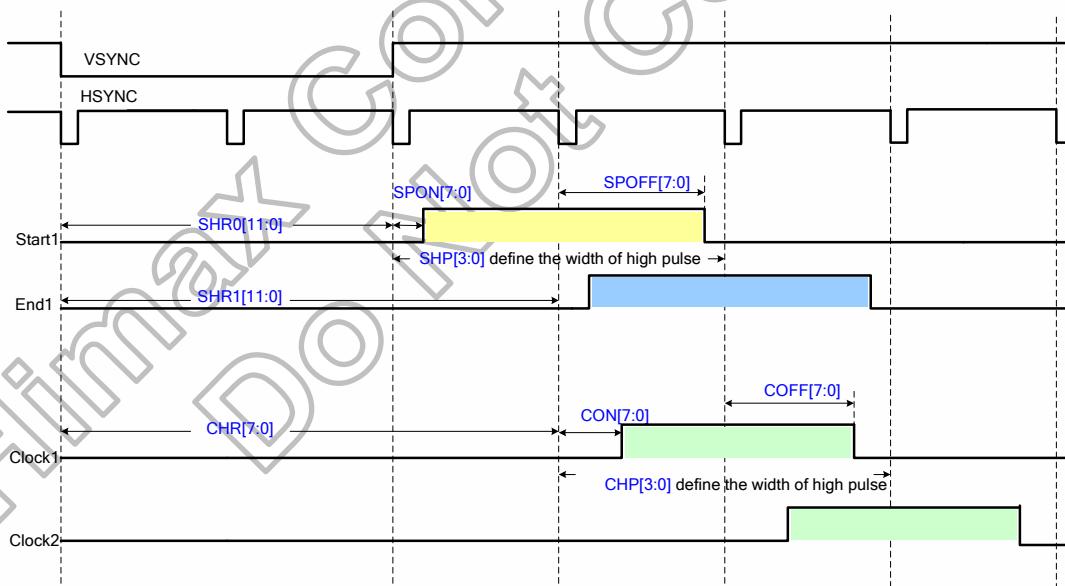
COFF/COFF1[7:0]: Fine tune the Start and End signal ending point.

COFF[7:0]	Clock signal output end delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
...	...
0xFFh	1020 OSC CLK

SON[7:0]: Source OP turn on time.

SOFF[7:0]: Source OP turn off time.

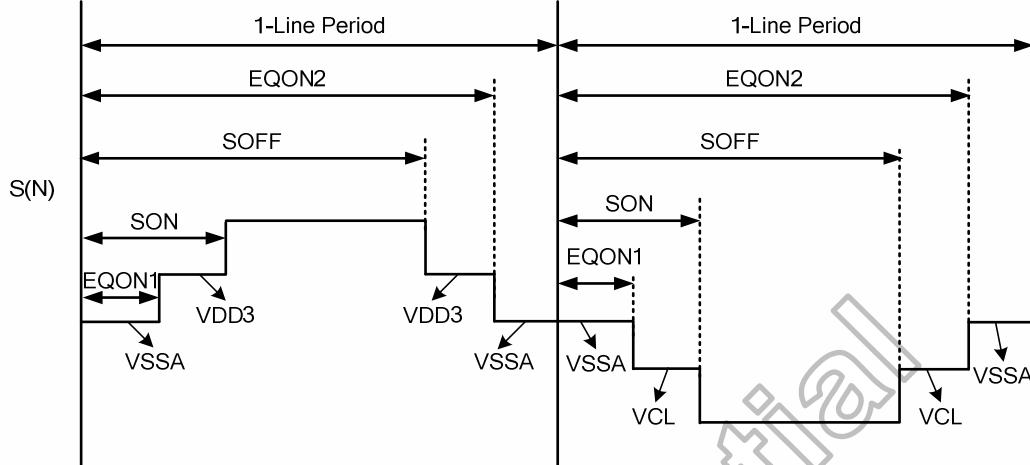
SON[7:0]/SOFF[7:0]	Source OP turn on/off time
0x00h	0 x OSC CLK
0x01h	1 x OSC CLK
0x02h	2 x OSC CLK
...	...
0xFEh	254 OSC CLK
0xFFh	255 OSC CLK



EQON1/EQON2[7:0]: Specify the source EQ period.

(Please note that the EQON1[7:0] < SON[7:0] < SOFF[7:0] < EQON2[7:0])

EQON1/EQON2[7:0]									Source EQ Period
0	0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	1	4 OSC clock cycle
0	0	0	0	0	0	1	0	0	8 OSC clock cycle
0	0	0	0	0	0	1	1	1	12 OSC clock cycle
0	0	0	0	0	1	0	0	0	16 OSC clock cycle
...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	0	0	0	1008 OSC clock cycle
1	1	1	1	1	1	0	1	1	1012 OSC clock cycle
1	1	1	1	1	1	1	0	1	1016 OSC clock cycle
1	1	1	1	1	1	1	1	1	1020 OSC clock cycle

**SPON\_MPU[7:0]:**

Fine tune the Start and End signal delay from original starting point for blanking frame

**SPOFF\_MPU[7:0]:**

Fine tune the Start and End signal ending point for blanking frame

**CON\_MPU/CON1\_MPU[7:0]:**

Fine tune the Clock signal delay from original starting point for blanking frame

**COFF\_MPU/COFF1\_MPU[7:0]:**

Fine tune the Clock signal ending point for blanking frame

**EQON1\_MPU/EQON2\_MPU[7:0]:**

Specify the source EQ period for blanking frame.

**Restrictions**

-

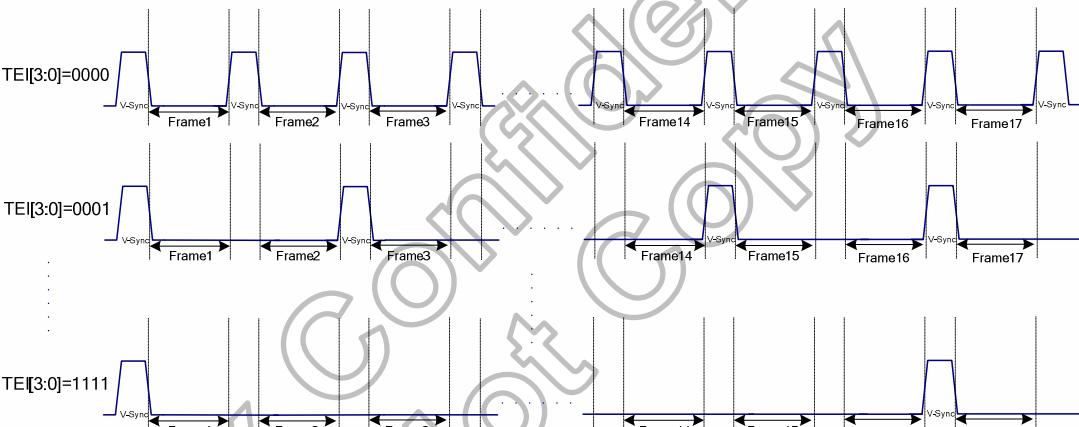
**Register Availability**

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

### 5.18.5 SETVCOM: Set VCOM voltage (B6h)

B6 H	SETVCOM ( Set VCOM Voltage)																																																																																																																																			
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																										
Command	0	1	0	1	1	0	1	1	0	B6																																																																																																																										
1 <sup>st</sup> parameter	1					VCMC_F[7:0]																																																																																																																														
2 <sup>nd</sup> parameter	1					VCMC_B[7:0]																																																																																																																														
3 <sup>rd</sup> parameter	1		VCOM_TIMES[2:0]		-	-	-	VCMC_B[8]	VCMC_F[8]	-																																																																																																																										
Description	<p>This command is used to set VCOM Voltage.</p> <p>VCMC_F[8:0]: Forward scan VCOM voltage control.</p> <p>VCMC_B[8:0]: Backward scan VCOM voltage control.</p> <table border="1"> <thead> <tr> <th colspan="9">VCMC_F[8:0]/VCMC_B[8:0]</th> <th>VCOM</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-0.30V</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-0.31V</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>-0.32V</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>-0.33V</td></tr> <tr><td colspan="9">:</td><td>:</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-3.98V</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-3.99V</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>-4.00V</td></tr> <tr><td colspan="9">Others</td><td>Inhibited</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>VSSA</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Hz</td></tr> </tbody> </table> <p>VCOM_TIMES[2:0]: Read the VCOM OTP programmed times.</p> <table border="1"> <thead> <tr> <th>VCOM_TIMES[2:0]</th> <th>VCOM OTP Programmed Times</th> </tr> </thead> <tbody> <tr><td>111</td><td>No programmed</td></tr> <tr><td>011</td><td>VCOM has been programmed 1 time</td></tr> <tr><td>001</td><td>VCOM has been programmed 2 times</td></tr> <tr><td>000</td><td>VCOM has been programmed 3 times</td></tr> </tbody> </table>		VCMC_F[8:0]/VCMC_B[8:0]									VCOM	0	0	0	0	0	0	0	0	0	-0.30V	0	0	0	0	0	0	0	0	1	-0.31V	0	0	0	0	0	0	0	1	0	-0.32V	0	0	0	0	0	0	0	1	1	-0.33V	:									:	1	0	1	1	1	0	0	0	0	-3.98V	1	0	1	1	1	0	0	0	1	-3.99V	1	0	1	1	1	0	0	1	0	-4.00V	Others									Inhibited	1	1	1	1	1	1	1	1	0	VSSA	1	1	1	1	1	1	1	1	1	Hz	VCOM_TIMES[2:0]	VCOM OTP Programmed Times	111	No programmed	011	VCOM has been programmed 1 time	001	VCOM has been programmed 2 times	000	VCOM has been programmed 3 times
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0	0	0	0	0	0	0	0	1	-0.31V																																																																																																																											
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Sleep In or Booster Off	Yes																																																																																																																																			

### 5.18.6 SETTE: Set internal TE function (B7h)

B7H	SETTE ( Set internal TE function)																																																																									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																
Command	0	1	0	1	1	0	1	1	1	B7																																																																
1 <sup>st</sup> parameter	1	-	-	TE_SEL[1:0]			TEI[3:0]			-																																																																
2 <sup>nd</sup> parameter	1	TEL_SEL[1:0]		TER_SEL[1:0]	-		TEP[10:8]			-																																																																
3 <sup>rd</sup> parameter	1				TEP[7:0]					-																																																																
Description	<p>TEI[3:0]: Set the output interval of TE signal according to the display data rewrite cycle and data transfer rate.</p> <table border="1"> <thead> <tr> <th>TEI[3]</th> <th>TEI[2]</th> <th>TEI[1]</th> <th>TEI[0]</th> <th>Output Interval</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1 frame</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>2 frames</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>3 frames</td> </tr> <tr> <td>...</td> <td>...</td> <td>...</td> <td>...</td> <td>...</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>15 frames</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>16 frames</td> </tr> </tbody> </table>  <p>TER_SEL/TEL_SEL[1:0]:</p> <table border="1"> <thead> <tr> <th>TER_SEL/TEL_SEL[1:0]</th> <th>TE_output</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Original TE signal</td> </tr> <tr> <td>01h</td> <td>V-blanking</td> </tr> <tr> <td>02h</td> <td>H-blanking</td> </tr> <tr> <td>03h</td> <td>Source Driving period</td> </tr> </tbody> </table> <p>TEP[10:0]: Set the output position of frame cycle signal. TE can be used as the trigger signal for frame synchronous write operation.</p> <p>Make sure the setting restriction <math>11'h000 \leq TEP[10:0] \leq \text{Numbers of Line}</math>.</p> <table border="1"> <thead> <tr> <th>TEP[10:0]</th> <th>Output position</th> </tr> </thead> <tbody> <tr> <td>000h</td> <td>0th line</td> </tr> <tr> <td>001h</td> <td>1<sup>st</sup> line</td> </tr> <tr> <td>002h</td> <td>2<sup>nd</sup> line</td> </tr> <tr> <td>003h</td> <td>3<sup>rd</sup> line</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>4FEh</td> <td>1278<sup>th</sup> line</td> </tr> <tr> <td>4FFh</td> <td>1279<sup>th</sup> line</td> </tr> <tr> <td>500h</td> <td>1280<sup>th</sup> line</td> </tr> </tbody> </table>	TEI[3]	TEI[2]	TEI[1]	TEI[0]	Output Interval	0	0	0	0	1 frame	0	0	0	1	2 frames	0	0	1	0	3 frames	...	...	...	...	...	1	1	1	0	15 frames	1	1	1	1	16 frames	TER_SEL/TEL_SEL[1:0]	TE_output	00h	Original TE signal	01h	V-blanking	02h	H-blanking	03h	Source Driving period	TEP[10:0]	Output position	000h	0th line	001h	1 <sup>st</sup> line	002h	2 <sup>nd</sup> line	003h	3 <sup>rd</sup> line	...	...	4FEh	1278 <sup>th</sup> line	4FFh	1279 <sup>th</sup> line	500h	1280 <sup>th</sup> line										
TEI[3]	TEI[2]	TEI[1]	TEI[0]	Output Interval																																																																						
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Restrictions	SETEXTC turn on to enable this command.																																																																									

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

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### 5.18.7 SETEXTC: Set extension command (B9h)

B9H	SETEXTC ( Set extended command set)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	0	1	1	1	0	0	1	B9								
1 <sup>st</sup> parameter	1					EXTC1[7:0]				-								
2 <sup>nd</sup> parameter	1					EXTC2[7:0]				-								
3 <sup>rd</sup> parameter	1					EXTC3[7:0]				-								
Description	This command is used to set extended command set access enable. <table border="1"> <tr> <td>Extend cmd</td> <td>Command description</td> </tr> <tr> <td>Enable</td> <td>After command (B9h), must write 3 parameters (FFh, 83h, 94h) by order</td> </tr> <tr> <td>Disable(default)</td> <td>After command(B9h), write 3 parameters (xxh,xxh,xxh) any value except (FFh, 83h, 94h)</td> </tr> </table>										Extend cmd	Command description	Enable	After command (B9h), must write 3 parameters (FFh, 83h, 94h) by order	Disable(default)	After command(B9h), write 3 parameters (xxh,xxh,xxh) any value except (FFh, 83h, 94h)		
Extend cmd	Command description																	
Enable	After command (B9h), must write 3 parameters (FFh, 83h, 94h) by order																	
Disable(default)	After command(B9h), write 3 parameters (xxh,xxh,xxh) any value except (FFh, 83h, 94h)																	
Restrictions	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

### 5.18.8 SETMIPI: Set MIPI control (BAh)

BAH	SETMIPI( Set MIPI control)																		
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	0	1	1	1	0	1	0	BA									
1 <sup>st</sup> parameter	1	-				DSISETUP0[6:0]				-									
2 <sup>nd</sup> parameter	1				DSISETUP1[7:0]					-									
Description	This command is used to set MIPI DSI Related Setting.																		
	<b>DSISETUP0</b>																		
	DSISETUP0[7]	Reserved																	
	DSISETUP0[6]	Tx Type: Define the LP-TX BTA behavior when there are error : 0: only BTA Error(default) 1: BTA Read + Error																	
	DSISETUP0[5]	CD_disable: Define the contention detection (LP-CD) function 0 : LP-CD function enable(default) 1: LP-CD function disable																	
	DSISETUP0[4]	Tx_OscDiv: LP-TX clock ( $T_{LPX}$ ) selection : 0 : 50ns ( $f_{LPX}=10MHz$ ) (default) 1 : 100ns ( $f_{LPX}=5MHz$ )																	
	DSISETUP0[3:2]	vc_main: Define the main function Virtual Channel ID(default=00)																	
	DSISETUP0[1:0]	LAN_NUM: Define the DSI lane number 00 : 1-lane 01 : 2-lane(default) 01 : 3-lane 11 : 4-lane																	
	<b>DSISETUP1</b>																		
	DSISETUP1[7]	CRC_enable: 1:Enable RX CRC Check( <b>default</b> ) 0:Disable RX CRC Check																	
	DSISETUP1[6]	ECC_ignore: Define the RX behavior when error occurring 0 : the transmission will be broken when there are ECC or CRC error(default) 1 : the transmission will keep when there are ECC or CRC error																	
	DSISETUP1[5]	RstTrig: Define the reset trigger function(46h) 0 : Disable reset trigger(default) 1 : same as HW_RESET function																	
	DSISETUP1[4]	PN_CHANGE: 0:Disable to Set PN change 1:Enable to Set PN change																	
	DSISETUP1[3:2]	Txe_Wait: BTA from Tx into Rx overlap waiting time counter( $T_{TA-GO}$ ) 00: TA-go = 2 Tlpz(default) 01: TA-go = 4 Tlpz 10: TA-go = 6 Tlpz 11: TA-go = 8 Tlpz																	
	DSISETUP1[1:0]	Rxs_Wait: BTA from Rx into Tx overlap waiting time counter( $T_{TA-GET}$ ) 00: Disable, no wait time 01: TA-get = 2 Tlpz 10: TA-get = 4 Tlpz 11: TA-get = 6 Tlpz( <b>default</b> )																	
Restrictions	SETEXTC turn on to enable this command.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		

### 5.18.9 SETOTP: Set OTP (BBh)

BBH	SETOTP( Set OTP Related Setting)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	0	1	1	1	0	1	1	BB								
1 <sup>st</sup> parameter	1					OTP_KEY0[7:0]				-								
2 <sup>nd</sup> parameter	1					OTP_KEY1[7:0]				-								
3 <sup>rd</sup> parameter	1					OTP_MASK[7:0]				-								
4 <sup>th</sup> parameter	1	INTVPP_EN	-	-	-	-	-		OTP_INDEX[9:8]	-								
5 <sup>th</sup> parameter	1					OTP_INDEX[7:0]				-								
6 <sup>th</sup> parameter	1	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM[1:0]	OTP_PWR_SEL	OTP_PROG		-								
7 <sup>th</sup> parameter	1					OTP_DATA[7:0]				-								
Description	This command is used to set OTP related setting.																	
	OTP_KEY0[7:0], OTP_KEY1[7:0]		Description			Note												
	OTP_KEY0[7:0] = 0xAh OTP_KEY1[7:0] = 0x55h		Enter OTP program mode															
	OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h		Leave OTP program mode															
	Other value		Invalid			If HX8394-D operate on OTP program mode, Then keep on OTP program mode. If HX8394-D operate on non-OTP program mode, Then keep on non-OTP program mode.												
	OTP_MASK[7:0]: Bit programming mask, "1" means this bit can't be programmed.																	
	OTP_INDEX[9:0]: Set index of OTP table for programming.																	
	NTVPP_EN: OTP_PWR power selected. "0": External OTP_PWR is selected when programmed. "1": Internal OTP_PWR (VGH short to OTP_PWR) is selected when programmed.																	
	OTP_PROG: When set to "1", the register content of OTP index is programmed.																	
	OTP_PWR_SEL: When written to "1", OTP power voltage is fed to OTP circuit.																	
	OTP_PTM[1:0]: For test mode using. Not open..																	
	OTP_PWE: OTP program write enable, "1" means OTP is able to be programmed.																	
	OTP_POR: Pulse for OTP data read operation.																	
	OTP_TEST: "0", setting OTP_PROG high will trigger internal state machine. "1", setting OTP_PROG high will not trigger internal state machine.																	
	OTP_LOAD_DISABLE: Normally the internal registers are auto-loaded from OTP when the SLPOUT command is received. Nevertheless, if this bit is set to 1, it will disable the auto loading function when the SLPOUT command was received. In general, this bit is used when OTP is not yet programmed.																	
	OTP_DATA[7:0]: Read back the OTP index data.																	

Restrictions	SETEXTC turn on to enable this command.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

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### 5.18.10 SETVDC: Set internal digital voltage (BCh)

BCH	SETVDC(Set internal digital voltage)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	0	BC
1 <sup>st</sup> parameter	1	-	-	-	-	-	VDC_SEL[2:0]	-	-	
<b>VDC_SEL[2:0]</b> is used to set internal digital voltage for digital circuit.										
Description	VDC_SEL2	VDC_SEL1	VDC_SEL0	VDDD						
	0	0	0	1.3						
	0	0	1	1.35						
	0	1	0	1.4						
	0	1	1	1.45						
	1	0	0	1.5						
	1	0	1	1.55						
	1	1	0	1.6						
	1	1	1	1.7						
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status		Availability							
	Normal Mode On, Idle Mode Off, Sleep Out		Yes							
	Normal Mode On, Idle Mode On, Sleep Out		Yes							
Sleep In or Booster Off		Yes								
Default	Refer to "6.1.2 User define command list table".									

### 5.18.11 SET\_BANK: Set register bank (BDh)

BDH	SET_DSI_COMBO(Set DS1 ERR/SPI combo)																								
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	1	1	1	0	0	0	1	BD															
1 <sup>st</sup> parameter	1	-	-	-	-	-	-	BANK_INDEX [1:0]	-																
Set the register bank for some Commands that beyond 64 parameters  This command is active only for C1h/D1h For example: Write C1h, PA44~PA85 Step1: write BDh,0x01 Step2: write C1h,PA1~42  Read C1h, PA86~PA127 Step1: write BDh,0x02 Step2: read C1h,PA1~42																									
Description	<table border="1"> <tr> <th>BANK INDEX[1:0]</th> <th>C1h (SETDGCLUT)</th> <th>D1h (SET_SLR)</th> </tr> <tr> <td>00(Bank 0)</td> <td>1~43(R)</td> <td>1~10</td> </tr> <tr> <td>01(Bank 1)</td> <td>44~85(G)</td> <td>NA</td> </tr> <tr> <td>10(Bank 2)</td> <td>86~127B)</td> <td>NA</td> </tr> <tr> <td>11(Bank 3)</td> <td>NA</td> <td>NA</td> </tr> </table>										BANK INDEX[1:0]	C1h (SETDGCLUT)	D1h (SET_SLR)	00(Bank 0)	1~43(R)	1~10	01(Bank 1)	44~85(G)	NA	10(Bank 2)	86~127B)	NA	11(Bank 3)	NA	NA
BANK INDEX[1:0]	C1h (SETDGCLUT)	D1h (SET_SLR)																							
00(Bank 0)	1~43(R)	1~10																							
01(Bank 1)	44~85(G)	NA																							
10(Bank 2)	86~127B)	NA																							
11(Bank 3)	NA	NA																							
Restrictions	SETEXTC turn on to enable this command.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes							
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	Refer to "6.1.2 User define command list table".																								

### 5.18.12 SETDGCLUT: Set DGC LUT (C1h)

C1H	SETDGCLUT ( Set DGC LUT )									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	0	1	C1
Bank 0 1 <sup>st</sup> parameter	1	-	-	-	-	-	-	-	DGC_E_N	-
2 <sup>nd</sup> parameter	1			R_GAMMA0[9:2]						-
3 <sup>rd</sup> parameter	1			R_GAMMA1[9:2]						-
4 <sup>th</sup> parameter	1			R_GAMMA2[9:2]						-
5 <sup>th</sup> parameter	1			R_GAMMA3[9:2]						-
6 <sup>th</sup> parameter	1			R_GAMMA4[9:2]						-
7 <sup>th</sup> parameter	1			R_GAMMA5[9:2]						-
8 <sup>th</sup> parameter	1			R_GAMMA6[9:2]						-
9 <sup>th</sup> parameter	1			R_GAMMA7[9:2]						-
10 <sup>th</sup> parameter	1			R_GAMMA8[9:2]						-
11 <sup>th</sup> parameter	1			R_GAMMA9[9:2]						-
12 <sup>th</sup> parameter	1			R_GAMMA10[9:2]						-
13 <sup>th</sup> parameter	1			R_GAMMA11[9:2]						-
14 <sup>th</sup> parameter	1			R_GAMMA12[9:2]						-
15 <sup>th</sup> parameter	1			R_GAMMA13[9:2]						-
16 <sup>th</sup> parameter	1			R_GAMMA14[9:2]						-
17 <sup>th</sup> parameter	1			R_GAMMA15[9:2]						-
18 <sup>th</sup> parameter	1			R_GAMMA16[9:2]						-
19 <sup>th</sup> parameter	1			R_GAMMA17[9:2]						-
20 <sup>th</sup> parameter	1			R_GAMMA18[9:2]						-
21 <sup>th</sup> parameter	1			R_GAMMA19[9:2]						-
22 <sup>th</sup> parameter	1			R_GAMMA20[9:2]						-
23 <sup>th</sup> parameter	1			R_GAMMA21[9:2]						-
24 <sup>th</sup> parameter	1			R_GAMMA22[9:2]						-
25 <sup>th</sup> parameter	1			R_GAMMA23[9:2]						-
26 <sup>th</sup> parameter	1			R_GAMMA24[9:2]						-
27 <sup>th</sup> parameter	1			R_GAMMA25[9:2]						-
28 <sup>th</sup> parameter	1			R_GAMMA26[9:2]						-
29 <sup>th</sup> parameter	1			R_GAMMA27[9:2]						-
30 <sup>th</sup> parameter	1			R_GAMMA28[9:2]						-
31 <sup>th</sup> parameter	1			R_GAMMA29[9:2]						-
32 <sup>th</sup> parameter	1			R_GAMMA30[9:2]						-
33 <sup>th</sup> parameter	1			R_GAMMA31[9:2]						-
34 <sup>th</sup> parameter	1			R_GAMMA32[9:2]						-
35 <sup>th</sup> parameter	1	R_GAMMA0[1:0]	R_GAMMA1[1:0]	R_GAMMA2[1:0]	R_GAMMA3[1:0]					-
36 <sup>th</sup> parameter	1	R_GAMMA4[1:0]	R_GAMMA5[1:0]	R_GAMMA6[1:0]	R_GAMMA7[1:0]					-
37 <sup>th</sup> parameter	1	R_GAMMA8[1:0]	R_GAMMA9[1:0]	R_GAMMA10[1:0]	R_GAMMA11[1:0]					-
38 <sup>th</sup> parameter	1	R_GAMMA12[1:0]	R_GAMMA13[1:0]	R_GAMMA14[1:0]	R_GAMMA15[1:0]					-
39 <sup>th</sup> parameter	1	R_GAMMA16[1:0]	R_GAMMA17[1:0]	R_GAMMA18[1:0]	R_GAMMA19[1:0]					-
40 <sup>th</sup> parameter	1	R_GAMMA20[1:0]	R_GAMMA21[1:0]	R_GAMMA22[1:0]	R_GAMMA23[1:0]					-
41 <sup>th</sup> parameter	1	R_GAMMA24[1:0]	R_GAMMA25[1:0]	R_GAMMA26[1:0]	R_GAMMA27[1:0]					-
42 <sup>th</sup> parameter	1	R_GAMMA28[1:0]	R_GAMMA29[1:0]	R_GAMMA30[1:0]	R_GAMMA31[1:0]					-
43 <sup>th</sup> parameter	1	R_GAMMA32[1:0]	-	-	-	-	-	-	-	-
Bank 1 1 <sup>st</sup> parameter	1			G_GAMMA0[9:2]						-
2 <sup>nd</sup> parameter	1			G_GAMMA1[9:2]						-
3 <sup>rd</sup> parameter	1			G_GAMMA2[9:2]						-
4 <sup>th</sup> parameter	1			G_GAMMA3[9:2]						-
5 <sup>th</sup> parameter	1			G_GAMMA4[9:2]						-
6 <sup>th</sup> parameter	1			G_GAMMA5[9:2]						-
7 <sup>th</sup> parameter	1			G_GAMMA6[9:2]						-
8 <sup>th</sup> parameter	1			G_GAMMA7[9:2]						-

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9 <sup>th</sup> parameter	1	G_GAMMA8[9:2]					-
10 <sup>th</sup> parameter	1	G_GAMMA9[9:2]					-
11 <sup>th</sup> parameter	1	G_GAMMA10[9:2]					-
12 <sup>th</sup> parameter	1	G_GAMMA11[9:2]					-
13 <sup>th</sup> parameter	1	G_GAMMA12[9:2]					-
14 <sup>th</sup> parameter	1	G_GAMMA13[9:2]					-
15 <sup>th</sup> parameter	1	G_GAMMA14[9:2]					-
16 <sup>th</sup> parameter	1	G_GAMMA15[9:2]					-
17 <sup>th</sup> parameter	1	G_GAMMA16[9:2]					-
18 <sup>th</sup> parameter	1	G_GAMMA17[9:2]					-
19 <sup>th</sup> parameter	1	G_GAMMA18[9:2]					-
20 <sup>th</sup> parameter	1	G_GAMMA19[9:2]					-
21 <sup>th</sup> parameter	1	G_GAMMA20[9:2]					-
22 <sup>th</sup> parameter	1	G_GAMMA21[9:2]					-
23 <sup>th</sup> parameter	1	G_GAMMA22[9:2]					-
24 <sup>th</sup> parameter	1	G_GAMMA23[9:2]					-
25 <sup>th</sup> parameter	1	G_GAMMA24[9:2]					-
26 <sup>th</sup> parameter	1	G_GAMMA25[9:2]					-
27 <sup>th</sup> parameter	1	G_GAMMA26[9:2]					-
28 <sup>th</sup> parameter	1	G_GAMMA27[9:2]					-
29 <sup>th</sup> parameter	1	G_GAMMA28[9:2]					-
30 <sup>th</sup> parameter	1	G_GAMMA29[9:2]					-
31 <sup>th</sup> parameter	1	G_GAMMA30[9:2]					-
32 <sup>th</sup> parameter	1	G_GAMMA31[9:2]					-
33 <sup>th</sup> parameter	1	G_GAMMA32[9:2]					-
34 <sup>th</sup> parameter	1	G_GAMMA0[1:0]	G_GAMMA1[1:0]	G_GAMMA2[1:0]	G_GAMMA3[1:0]		-
35 <sup>th</sup> parameter	1	G_GAMMA4[1:0]	G_GAMMA5[1:0]	G_GAMMA6[1:0]	G_GAMMA7[1:0]		-
36 <sup>th</sup> parameter	1	G_GAMMA8[1:0]	G_GAMMA9[1:0]	G_GAMMA10[1:0]	G_GAMMA11[1:0]		-
37 <sup>th</sup> parameter	1	G_GAMMA12[1:0]	G_GAMMA13[1:0]	G_GAMMA14[1:0]	G_GAMMA15[1:0]		-
38 <sup>th</sup> parameter	1	G_GAMMA16[1:0]	G_GAMMA17[1:0]	G_GAMMA18[1:0]	G_GAMMA19[1:0]		-
39 <sup>th</sup> parameter	1	G_GAMMA20[1:0]	G_GAMMA21[1:0]	G_GAMMA22[1:0]	G_GAMMA23[1:0]		-
40 <sup>th</sup> parameter	1	G_GAMMA24[1:0]	G_GAMMA25[1:0]	G_GAMMA26[1:0]	G_GAMMA27[1:0]		-
41 <sup>th</sup> parameter	1	G_GAMMA28[1:0]	G_GAMMA29[1:0]	G_GAMMA30[1:0]	G_GAMMA31[1:0]		-
42 <sup>th</sup> parameter	1	G_GAMMA32[1:0]	-	-	-	-	-
Bank 2	1	B_GAMMA0[9:2]					-
1 <sup>st</sup> parameter		B_GAMMA1[9:2]					-
2 <sup>nd</sup> parameter	1	B_GAMMA2[9:2]					-
3 <sup>rd</sup> parameter	1	B_GAMMA3[9:2]					-
4 <sup>th</sup> parameter	1	B_GAMMA4[9:2]					-
5 <sup>th</sup> parameter	1	B_GAMMA5[9:2]					-
6 <sup>th</sup> parameter	1	B_GAMMA6[9:2]					-
7 <sup>th</sup> parameter	1	B_GAMMA7[9:2]					-
8 <sup>th</sup> parameter	1	B_GAMMA8[9:2]					-
9 <sup>th</sup> parameter	1	B_GAMMA9[9:2]					-
10 <sup>th</sup> parameter	1	B_GAMMA10[9:2]					-
11 <sup>th</sup> parameter	1	B_GAMMA11[9:2]					-
12 <sup>th</sup> parameter	1	B_GAMMA12[9:2]					-
13 <sup>th</sup> parameter	1	B_GAMMA13[9:2]					-
14 <sup>th</sup> parameter	1	B_GAMMA14[9:2]					-
15 <sup>th</sup> parameter	1	B_GAMMA15[9:2]					-
16 <sup>th</sup> parameter	1	B_GAMMA16[9:2]					-
17 <sup>th</sup> parameter	1	B_GAMMA17[9:2]					-
18 <sup>th</sup> parameter	1	B_GAMMA18[9:2]					-
19 <sup>th</sup> parameter	1	B_GAMMA19[9:2]					-
20 <sup>th</sup> parameter	1	B_GAMMA20[8:2]					-
21 <sup>th</sup> parameter	1	B_GAMMA20[8:2]					-

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22 <sup>th</sup> parameter	1	B_GAMMA21[9:2]				-
23 <sup>th</sup> parameter	1	B_GAMMA22[9:2]				-
24 <sup>th</sup> parameter	1	B_GAMMA23[9:2]				-
25 <sup>th</sup> parameter	1	B_GAMMA24[9:2]				-
26 <sup>th</sup> parameter	1	B_GAMMA25[9:2]				-
27 <sup>th</sup> parameter	1	B_GAMMA26[9:2]				-
28 <sup>th</sup> parameter	1	B_GAMMA27[9:2]				-
29 <sup>th</sup> parameter	1	B_GAMMA28[9:2]				-
30 <sup>th</sup> parameter	1	B_GAMMA29[9:2]				-
31 <sup>th</sup> parameter	1	B_GAMMA30[9:2]				-
32 <sup>th</sup> parameter	1	B_GAMMA31[9:2]				-
33 <sup>th</sup> parameter	1	B_GAMMA32[9:2]				-
34 <sup>th</sup> parameter	1	B_GAMMA0[1:0]	B_GAMMA1[1:0]	B_GAMMA2[1:0]	B_GAMMA3[1:0]	-
35 <sup>th</sup> parameter	1	B_GAMMA4[1:0]	B_GAMMA5[1:0]	B_GAMMA6[1:0]	B_GAMMA7[1:0]	-
36 <sup>th</sup> parameter	1	B_GAMMA8[1:0]	B_GAMMA9[1:0]	B_GAMMA10[1:0]	B_GAMMA11[1:0]	-
37 <sup>th</sup> parameter	1	B_GAMMA12[1:0]	B_GAMMA13[1:0]	B_GAMMA14[1:0]	B_GAMMA15[1:0]	-
38 <sup>th</sup> parameter	1	B_GAMMA16[1:0]	B_GAMMA17[1:0]	B_GAMMA18[1:0]	B_GAMMA19[1:0]	-
39 <sup>th</sup> parameter	1	B_GAMMA20[1:0]	B_GAMMA21[1:0]	B_GAMMA22[1:0]	B_GAMMA23[1:0]	-
40 <sup>th</sup> parameter	1	B_GAMMA24[1:0]	B_GAMMA25[1:0]	B_GAMMA26[1:0]	B_GAMMA27[1:0]	-
41 <sup>th</sup> parameter	1	B_GAMMA28[1:0]	B_GAMMA29[1:0]	B_GAMMA30[1:0]	B_GAMMA31[1:0]	-
42 <sup>th</sup> parameter	1	B_GAMMA31[1:0]	-	-	-	-

This command is used to set Digital Gamma Curve Look-Up Table.

Before read/write this command, user must set BDh first to select different banks

No default value in this command

Bank0 keep all the read path but bank1&bank2 only keep 1<sup>st</sup> and 42<sup>th</sup> read path.

DGC\_EN: Enable the DGC function

### Description

LUT data input (Hex)	LUT data output
00h	GAMMA0[9:0]
08h	GAMMA1[9:0]
10h	GAMMA2[9:0]
18h	GAMMA3[9:0]
20h	GAMMA4[9:0]
28h	GAMMA5[9:0]
30h	GAMMA6[9:0]
38h	GAMMA7[9:0]
40h	GAMMA8[9:0]
48h	GAMMA9[9:0]
50h	GAMMA10[9:0]
58h	GAMMA11[9:0]
60h	GAMMA12[9:0]
68h	GAMMA13[9:0]
70h	GAMMA14[9:0]
78h	GAMMA15[9:0]
80h	GAMMA16[9:0]
88h	GAMMA17[9:0]
90h	GAMMA18[9:0]
98h	GAMMA19[9:0]
A0h	GAMMA20[9:0]
A8h	GAMMA21[9:0]
B0h	GAMMA22[9:0]
B8h	GAMMA23[9:0]
C0h	GAMMA24[9:0]
C8h	GAMMA25[9:0]
D0h	GAMMA26[9:0]
D8h	GAMMA27[9:0]
E0h	GAMMA28[9:0]

	E8h	GAMMA29[9:0]	
	F0h	GAMMA30[9:0]	
	F8h	GAMMA31[9:0]	
	FFh	GAMMA32[9:0]	
Restrictions	SETEXTC turn on to enable this command.		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In or Booster Off	Yes	

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### 5.18.13 SETID: Set ID (C3h)

C3H	SETID ( Set ID)																		
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	1	0	0	0	0	1	1	C3									
1 <sup>st</sup> parameter	1					ID1[7:0]				-									
2 <sup>nd</sup> parameter	1					ID2[7:0]				-									
3 <sup>rd</sup> parameter	1					ID3[7:0]				-									
4 <sup>th</sup> parameter	1					ID4[7:0]				-									
5 <sup>th</sup> parameter	1		ID_TIMES[2:0]		-	-	-	-	-	-									
Description	ID1[7:0] is used to set ID RDAh value.																		
	ID2[7:0] is used to set ID RDBh value.																		
	ID3[7:0] is used to set ID RDCh value.																		
	ID4[7:0] is used to set the fourth ID.																		
	ID_TIMES[2:0]: Read the ID OTP programmed times.																		
	<table border="1"> <tr> <td>ID_TIMES[2:0]</td> <td>ID OTP Programmed Times</td> </tr> <tr> <td>111</td> <td>No programmed</td> </tr> <tr> <td>011</td> <td>ID has been programmed 1 time</td> </tr> <tr> <td>001</td> <td>ID has been programmed 2 times</td> </tr> <tr> <td>000</td> <td>ID has been programmed 3 times</td> </tr> </table>										ID_TIMES[2:0]	ID OTP Programmed Times	111	No programmed	011	ID has been programmed 1 time	001	ID has been programmed 2 times	000
ID_TIMES[2:0]	ID OTP Programmed Times																		
111	No programmed																		
011	ID has been programmed 1 time																		
001	ID has been programmed 2 times																		
000	ID has been programmed 3 times																		
Restrictions	SETEXTC turn on to enable this command.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		

### 5.18.14 SETCABC: Set CABC control (C9h)

C9H	SETCABC (Set CABC Control)																																																																																																																				
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																											
Command	0	1	1	0	0	1	0	0	1	C9																																																																																																											
1 <sup>st</sup> Parameter	1	PWM_PERIO D[16]		SEL_PWMCLK[2:0]		SEL_GAIN[1:0]		INVPU LS(1)	SEL_B LDUTY (1)	-																																																																																																											
2 <sup>nd</sup> Parameter	1			PWM_PERIOD[15:8]						-																																																																																																											
3 <sup>rd</sup> Parameter	1			PWM_PERIOD[7:0]						-																																																																																																											
4 <sup>th</sup> Parameter	1	CABC_FSYNC			DIM_FRAME[6:0]					-																																																																																																											
5 <sup>th</sup> Parameter	1	CABC_DD	-	-	BC_CT RL_EN		CABC_FLM[3:0]			-																																																																																																											
6 <sup>th</sup> Parameter	1			PWM_PERIOD[6:0]						-																																																																																																											
7 <sup>th</sup> Parameter	1	-		SAVEPOWER[6:0]						-																																																																																																											
8 <sup>th</sup> Parameter	1	DATAGAIN_AIN_EN	-	-	-	-	-	DATAGAIN_VALUE[9:8]																																																																																																													
9 <sup>th</sup> Parameter	1	-		PWM_PERIOD[7:0]																																																																																																																	
Description	This command is used to set CABC parameter.																																																																																																																				
	SEL_BLDUTY: Backlight pwm output duty on/off control when CABC operation. '0', The Backlight pwm output duty is 100%. '1', The Backlight pwm output duty is calculate from CABC operation..																																																																																																																				
	INVPULS: The backlight PWM output polarity select. '0', The backlight PWM output is low level active. '1', The backlight PWM output is high level active.																																																																																																																				
	SEL_GAIN[1:0]: CABC gain select.																																																																																																																				
	<table border="1"> <tr> <td>SEL_GAIN[1:0]</td><td></td><td>Gain</td></tr> <tr> <td>00</td><td></td><td>Use 1.00 as CABC calculate gain</td></tr> <tr> <td>01</td><td></td><td>Use 0.5x CABC calculate gain</td></tr> <tr> <td>10</td><td></td><td>Use 0.75x as CABC calculate gain</td></tr> <tr> <td>11</td><td></td><td>Use CABC calculate gain</td></tr> </table>										SEL_GAIN[1:0]		Gain	00		Use 1.00 as CABC calculate gain	01		Use 0.5x CABC calculate gain	10		Use 0.75x as CABC calculate gain	11		Use CABC calculate gain																																																																																												
SEL_GAIN[1:0]		Gain																																																																																																																			
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11		Use CABC calculate gain																																																																																																																			
SEL_PWMCLK[2:0] : Internal PWM_CLK divider for CABC clock.																																																																																																																					
<table border="1"> <tr> <th>SEL_PWMCLK[2:0]</th><th colspan="10">Brightness Control Clock frequency</th></tr> <tr> <td>0 0 0</td><td colspan="9">PWM_CLK / 1</td><td></td></tr> <tr> <td>0 0 1</td><td colspan="9">PWM_CLK / 2</td><td></td></tr> <tr> <td>0 1 0</td><td colspan="9">PWM_CLK / 4</td><td></td></tr> <tr> <td>0 1 1</td><td colspan="9">PWM_CLK / 6</td><td></td></tr> <tr> <td>1 0 0</td><td colspan="9">PWM_CLK / 8</td><td></td></tr> <tr> <td>1 0 1</td><td colspan="9">PWM_CLK / 10</td><td></td></tr> <tr> <td>1 1 0</td><td colspan="9">PWM_CLK / 12</td><td></td></tr> <tr> <td>1 1 1</td><td colspan="9">PWM_CLK / 14</td><td></td></tr> </table>										SEL_PWMCLK[2:0]	Brightness Control Clock frequency										0 0 0	PWM_CLK / 1										0 0 1	PWM_CLK / 2										0 1 0	PWM_CLK / 4										0 1 1	PWM_CLK / 6										1 0 0	PWM_CLK / 8										1 0 1	PWM_CLK / 10										1 1 0	PWM_CLK / 12										1 1 1	PWM_CLK / 14																		
SEL_PWMCLK[2:0]	Brightness Control Clock frequency																																																																																																																				
0 0 0	PWM_CLK / 1																																																																																																																				
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1 1 1	PWM_CLK / 14																																																																																																																				
PWM_PERIOD[16:0]: The backlight PWM output period setting.																																																																																																																					
When PWM_PERIOD[16]=0, PWM_PERIOD[15:6] setting inhibited.																																																																																																																					
<table border="1"> <tr> <th colspan="6">PWM_PERIOD [5:0]</th><th colspan="5">CABC_PWM_OUT signal frequency</th></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="5">[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/500</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td colspan="5">[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/513</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="5">[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/527</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td colspan="5">[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/541</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td colspan="5">[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/556</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td colspan="5">[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/572</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="5">[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/589</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td colspan="5">[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/607</td></tr> </table>										PWM_PERIOD [5:0]						CABC_PWM_OUT signal frequency					0	0	0	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/500					0	0	0	0	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/513					0	0	0	0	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/527					0	0	0	0	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/541					0	0	0	1	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/556					0	0	0	1	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/572					0	0	0	1	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/589					0	0	0	1	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/607					
PWM_PERIOD [5:0]						CABC_PWM_OUT signal frequency																																																																																																															
0	0	0	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/500																																																																																																														
0	0	0	0	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/513																																																																																																														
0	0	0	0	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/527																																																																																																														
0	0	0	0	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/541																																																																																																														
0	0	0	1	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/556																																																																																																														
0	0	0	1	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/572																																																																																																														
0	0	0	1	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/589																																																																																																														
0	0	0	1	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/607																																																																																																														

0	0	1	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/625
0	0	1	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/646
0	0	1	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/667
0	0	1	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/690
0	0	1	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/715
0	0	1	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/741
0	0	1	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/770
0	0	1	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/800
0	1	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/834
0	1	0	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/870
0	1	0	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/910
0	1	0	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/953
0	1	0	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1000
0	1	0	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1053
0	1	0	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1112
0	1	0	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1177
0	1	1	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1250
0	1	1	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1334
0	1	1	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1429
0	1	1	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1539
0	1	1	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1667
0	1	1	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/1819
0	1	1	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/2000
0	1	1	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/2223
1	0	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/2500
1	0	0	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/2858
1	0	0	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/3334
1	0	0	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/4000
1	0	0	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/5000
1	0	0	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/6667
1	0	0	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/10000
1	0	0	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/20000
1	0	1	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/22223
1	0	1	0	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/25000
1	0	1	0	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/28572
1	0	1	0	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/33334
1	0	1	1	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/40000
1	0	1	1	0	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/50000
1	0	1	1	1	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/66667
1	0	1	1	1	1	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/100000
1	1	0	0	0	0	[(Fosc/ABC_OSCDIV[1:0])/SEL_PWMCLK[2:0]]/200000
Others					Inhibited	

When PWM\_PERIOD[16]=1:

CABC\_PWM\_OUT frequency=

[(Fosc/ABC\_OSCDIV[1:0])/SEL\_PWMCLK[2:0]]/( PWM\_PERIOD[15:0]+1)

Note: PWM\_PERIOD[15:0]=0000h is inhibited.

DIM\_FRAME[6:0] : Manual brightness setting dimming period.

CABC\_FSYNC: Reset CABC\_PWM\_OUT signal by each VSYNC.

CABC\_DD: CABC dimming function enable bit.

'0', Disable CABC dimming.

'1', Enable CABC dimming.

CABC\_STEP[7:0]: CABC step numbers during dimming period.

CABC\_FLM[3:0]: CABC dimming frame number for each step.

BC\_CTRL\_EN: Enable Backlight & PMIC.

SAVEPOWER[6:0] : Minimum CABC gain / maximum CABC duty output select.

SAVEPOWER [6:0]							Min. Gain	Max. Duty
0	0	x	x	x	x	x	Reserve	
0	1	0	0	0	0	0	1+0/32	100%
0	1	0	0	0	0	1	1+1/32	96.97%
0	1	0	0	0	1	0	1+2/32	94.12%
0	1	0	0	0	1	1	1+3/32	91.43%
0	1	0	0	1	0	0	1+4/32	88.89%
0	1	0	0	1	0	1	1+5/32	86.49%
0	1	0	0	1	1	0	1+6/32	84.21%
0	1	0	0	1	1	1	1+7/32	82.05%
0	1	0	1	0	0	0	1+8/32	80%
0	1	0	1	0	0	1	1+9/32	78.05%
0	1	0	1	0	1	0	1+10/32	76.19%
0	1	0	1	0	1	1	1+11/32	74.42%
0	1	0	1	1	0	0	1+12/32	72.73%
0	1	0	1	1	0	1	1+13/32	71.11%
0	1	0	1	1	1	0	1+14/32	69.57%
0	1	0	1	1	1	1	1+15/32	68.09%
0	1	1	0	0	0	0	1+16/32	66.67%
0	1	1	0	0	0	1	1+17/32	65.31%
0	1	1	0	0	1	0	1+18/32	64%
0	1	1	0	0	1	1	1+19/32	62.75%
0	1	1	0	1	0	0	1+20/32	61.54%
0	1	1	0	1	0	1	1+21/32	60.38%
0	1	1	0	1	1	0	1+22/32	59.26%
0	1	1	0	1	1	1	1+23/32	58.18%
0	1	1	1	0	0	0	1+24/32	57.14%
0	1	1	1	0	0	1	1+25/32	56.14%
0	1	1	1	0	1	0	1+26/32	55.17%
0	1	1	1	0	1	1	1+27/32	54.24%
0	1	1	1	1	0	0	1+28/32	53.33%
0	1	1	1	1	0	1	1+29/32	52.46%
0	1	1	1	1	1	0	1+30/32	51.61%
0	1	1	1	1	1	1	1+31/32	50.79%
1	0	0	0	0	0	0	1+32/32	50%

For details, please refer to chapter "5.13.2 CABC Block".

DATAGAIN\_EN : unit data gain enable

1:data gain follow unit data gain DATAGAIN\_VALUE[9:0]

0:data gain follow RCEh setting

DATAGAIN\_VALUE[9:0] : set unit gain value.

Restriction SETEXTC turn on to enable this command.

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

### 5.18.15 SETCABCGAIN (CAh)

CAH	SETCABCGAIN									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	1	0	CA
1 <sup>st</sup> Parameter	1	-				DBG0[6:0]				-
2 <sup>nd</sup> parameter	1	-				DBG1[6:0]				-
3 <sup>rd</sup> parameter	1	-				DBG2[6:0]				-
4 <sup>th</sup> parameter	1	-				DBG3[6:0]				-
5 <sup>th</sup> parameter	1	-				DBG4[6:0]				-
6 <sup>th</sup> parameter	1	-				DBG5[6:0]				-
7 <sup>th</sup> parameter	1	-				DBG6[6:0]				-
8 <sup>th</sup> parameter	1	-				DBG7[6:0]				-
9 <sup>th</sup> parameter	1	-				DBG8[6:0]				-
Description	DBG0~8[6:0] : Gain select register 0~8.									
	DBG0~8[6:0]							CABC Gain	CABC Duty	
	0	0	x	x	x	x	x	Reserve		
	0	1	0	0	0	0	0	1+0/32	100%	
	0	1	0	0	0	0	1	1+1/32	96.97%	
	0	1	0	0	0	1	0	1+2/32	94.12%	
	0	1	0	0	0	1	1	1+3/32	91.43%	
	0	1	0	0	1	0	0	1+4/32	88.89%	
	0	1	0	0	1	0	1	1+5/32	86.49%	
	0	1	0	0	1	1	0	1+6/32	84.21%	
	0	1	0	0	1	1	1	1+7/32	82.05%	
	0	1	0	1	0	0	0	1+8/32	80%	
	0	1	0	1	0	0	1	1+9/32	78.05%	
	0	1	0	1	0	1	0	1+10/32	76.19%	
	0	1	0	1	0	1	1	1+11/32	74.42%	
	0	1	0	1	1	0	0	1+12/32	72.73%	
	0	1	0	1	1	0	1	1+13/32	71.11%	
	0	1	0	1	1	1	0	1+14/32	69.57%	
	0	1	0	1	1	1	1	1+15/32	68.09%	
	0	1	1	0	0	0	0	1+16/32	66.67%	
	0	1	1	0	0	0	1	1+17/32	65.31%	
	0	1	1	0	0	1	0	1+18/32	64%	
	0	1	1	0	0	1	1	1+19/32	62.75%	
	0	1	1	0	1	0	0	1+20/32	61.54%	
	0	1	1	0	1	0	1	1+21/32	60.38%	
	0	1	1	0	1	1	0	1+22/32	59.26%	
	0	1	1	0	1	1	1	1+23/32	58.18%	
	0	1	1	1	0	0	0	1+24/32	57.14%	
	0	1	1	1	0	0	1	1+25/32	56.14%	
	0	1	1	1	0	1	0	1+26/32	55.17%	
	0	1	1	1	0	1	1	1+27/32	54.24%	
	0	1	1	1	1	0	0	1+28/32	53.33%	
	0	1	1	1	1	0	1	1+29/32	52.46%	
	0	1	1	1	1	1	0	1+30/32	51.61%	
	0	1	1	1	1	1	1	1+31/32	50.79%	
	1	0	0	0	0	0	0	1+32/32	50%	
Restrictions	For details, please refer to chapter "5.13.2 CABC Block".									
Register Availability	SETEXTC turn on to enable this command.									
	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				

### 5.18.16 SETPANEL (CCh)

CCH	SETPANEL( Set panel related register)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	0	1	1	0	0	CC								
1 <sup>st</sup> parameter	1	-	-	-	-	SS_PA NEL	GS_PA NEL	REV_P ANEL	BGR_P ANEL	-								
Description0	<p>This command is used to set setting of panel related register and make panel module meets below spec from viewpoint of user</p> <p>BGR_PANEL: The order of &lt;R&gt;&lt;G&gt;&lt;B&gt; dot color for module supplier, default value is stored in OTP. If color filter of panel is &lt;B&gt;&lt;G&gt;&lt;R&gt; type, setting BGR_PANEL = 1, if color filter of panel is &lt;R&gt;&lt;G&gt;&lt;B&gt; type, setting BGR_PANEL = 0. This bit is to make panel module look like a &lt;R&gt;&lt;G&gt;&lt;B&gt; type panel form the user viewpoint.</p> <p>REV_PANEL: Select the inversion of the display of all characters and graphics. This setting allows the display of the same data on both normally-white and normally-black panels.      REV_PANEL = 1 normal-white panel      REV_PANEL = 0 normal-black panel</p> <p>GS_PANEL: Specify the shift direction of gate driver output.      When GS_PANEL = 0, the panel control signal is normal scan.      When GS_PANEL = 1, the panel control signal is reverse scan.</p> <p>SS_PANEL: Specify the shift direction of source driver output. When SS_PANEL = 0, the shift direction from S1 to S1620 When SS_PANEL = 1, the shift direction from S1280 to S1.</p>																	
Restrictions	SETEXTC turn on to enable this command																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

### 5.18.17 SETCABCLUT (CEh)

CEH	SETCABCLUT									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	1	1	0	CE
1 <sup>st</sup> parameter	1					DATAGAIN1_00D32[7:0]				-
2 <sup>nd</sup> parameter	1					DATAGAIN1_01D32[7:0]				-
3 <sup>rd</sup> parameter	1					DATAGAIN1_02D32[7:0]				-
4 <sup>th</sup> parameter	1					DATAGAIN1_03D32[7:0]				-
5 <sup>th</sup> parameter	1					DATAGAIN1_04D32[7:0]				-
6 <sup>th</sup> parameter	1					DATAGAIN1_05D32[7:0]				-
7 <sup>th</sup> parameter	1					DATAGAIN1_06D32[7:0]				-
8 <sup>th</sup> parameter	1					DATAGAIN1_07D32[7:0]				-
9 <sup>th</sup> parameter	1					DATAGAIN1_08D32[7:0]				-
10 <sup>th</sup> parameter	1					DATAGAIN1_09D32[7:0]				-
11 <sup>th</sup> parameter	1					DATAGAIN1_10D32[7:0]				-
12 <sup>th</sup> parameter	1					DATAGAIN1_11D32[7:0]				-
13 <sup>th</sup> parameter	1					DATAGAIN1_12D32[7:0]				-
14 <sup>th</sup> parameter	1					DATAGAIN1_13D32[7:0]				-
15 <sup>th</sup> parameter	1					DATAGAIN1_14D32[7:0]				-
16 <sup>th</sup> parameter	1					DATAGAIN1_15D32[7:0]				-
17 <sup>th</sup> parameter	1					DATAGAIN1_16D32[7:0]				-
18 <sup>th</sup> parameter	1					DATAGAIN1_17D32[7:0]				-
19 <sup>th</sup> parameter	1					DATAGAIN1_18D32[7:0]				-
20 <sup>th</sup> parameter	1					DATAGAIN1_19D32[7:0]				-
21 <sup>st</sup> parameter	1					DATAGAIN1_20D32[7:0]				-
22 <sup>nd</sup> parameter	1					DATAGAIN1_21D32[7:0]				-
23 <sup>rd</sup> parameter	1					DATAGAIN1_22D32[7:0]				-
24 <sup>th</sup> parameter	1					DATAGAIN1_23D32[7:0]				-
25 <sup>th</sup> parameter	1					DATAGAIN1_24D32[7:0]				-
26 <sup>th</sup> parameter	1					DATAGAIN1_25D32[7:0]				-
27 <sup>th</sup> parameter	1					DATAGAIN1_26D32[7:0]				-
28 <sup>th</sup> parameter	1					DATAGAIN1_27D32[7:0]				-
29 <sup>th</sup> parameter	1					DATAGAIN1_28D32[7:0]				-
30 <sup>th</sup> parameter	1					DATAGAIN1_29D32[7:0]				-
31 <sup>st</sup> parameter	1					DATAGAIN1_30D32[7:0]				-
32 <sup>nd</sup> parameter	1					DATAGAIN1_31D32[7:0]				-
33 <sup>rd</sup> parameter	1					DATAGAIN2_00D32[7:0]				-
34 <sup>th</sup> parameter	1	0	0	0	0	0	0	0	DATAGAIN2_00D32[9:8]	-
Description	This command is used for CABC LUT test Keep 2 <sup>nd</sup> and 32 <sup>nd</sup> ,34 <sup>th</sup> write path only.									
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status	Availability								
	Normal Mode On, Idle Mode Off, Sleep Out	Yes								
	Normal Mode On, Idle Mode On, Sleep Out	Yes								
	Sleep In or Booster Off	Yes								

**5.18.18 SET\_SLR\_MODE (D0H)**

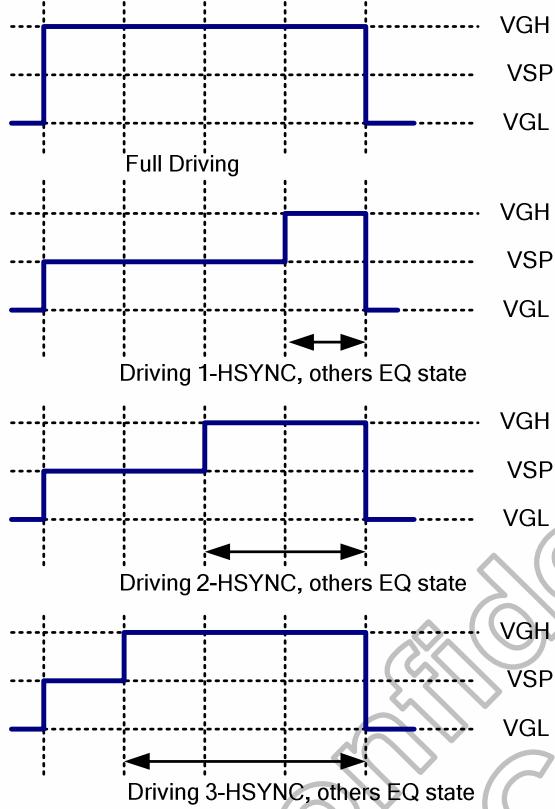
D0H	SET_SLR_MODE																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	1	0	0	0	0	D0								
1 <sup>st</sup> parameter	1	reg_amb_val[7:0]								80								
2 <sup>nd</sup> parameter	1	reg_CTRL_EHLV[7:0]								40								
3 <sup>rd</sup> parameter	1	-	-	-	-	slr_sel_opt	slr_demo_on	slr_bp_s_en	reg_slr_en	00								
Description	<p>This command is used for sun light readability.</p> <p>reg_amb_val[7:0]: Set larger value for reg_amb_val if brighter ambient light is detected via a sensor. Value ranges from 0 ~ 80.</p> <p>reg_CTRL_EHLV[7:0]: Set the enhanced level of SLR. User-defined enhance strength. 40h: normal enhancement; 20h: weak enhancement; 00h: zero enhancement;</p> <p>slr_sel_opt: SLR resolution related register choose option. 0: auto set resolution related registers. 1: manual set resolution related registers.</p> <p>slr_demo_on: SLR demo mode signal, for demo only. 0: apply SLR normal display mode. 1: enable SLR demo mode, only the right side of the current frame will be enhanced.</p> <p>slr_bps_en: SLR bypass signal, for debug only. 0: apply SLR enhancement onto output. 1: ignore SLR enhancement for debugging (output is copied from input).</p> <p>reg_slr_en: SLR function enable. 0: Disable. 1: Enable.</p>																	
Restrictions	SETEXTC turn on to enable this command.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

**5.18.19 SET\_SLR(D1H)**

D1H	SET_SLR									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	0	0	0	1	D1
1 <sup>st</sup> parameter	1					reg_smp_H[7:0]				-
2 <sup>nd</sup> parameter	1					reg_smp_V[7:0]				-
3 <sup>rd</sup> parameter	1	-	-	-	-	-	-	-	reg_smp_RES_H_max[8]	-
4 <sup>rd</sup> parameter	1				reg_smp_RES_H_max[7:0]					-
5 <sup>rd</sup> parameter	1	-	-	-	-	-	-	-	reg_smp_RES_V_max[8]	-
6 <sup>rd</sup> parameter	1				reg_smp_RES_V_max[7:0]					-
7 <sup>rd</sup> parameter	1				reg_blue_col_cnt_th[15:8]					-
8 <sup>rd</sup> parameter	1				reg_blue_col_cnt_th[7:0]					-
9 <sup>rd</sup> parameter	1				reg_grad_col_cnt_th[15:8]					-
10 <sup>rd</sup> parameter	1				reg_grad_col_cnt_th[7:0]					-
Register Availability	Status				Availability					
	Normal Mode On, Idle Mode Off, Sleep Out				Yes					
	Normal Mode On, Idle Mode On, Sleep Out				Yes					
	Sleep In or Booster Off				Yes					

### 5.18.20 SETGIP\_0: Set GIP option 0 (D3h)

D3H	SETGIP_0											
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	0	1	0	0	1	1	D3		
1 <sup>st</sup> parameter	1	-	-	GIP_MODE[1:0]	-	EQ_DELAY_HSYNC[3:0]	-	-	-	-		
2 <sup>nd</sup> parameter	1	-	-	-	EQ_DELAY[7:0]	-	-	-	-	-		
GIP_MODE[1:0]: GIP EQ (pre-charge) type selection												
GIP_MODE[1]		GIP_MODE[0]		GIP EQ Type								
0		0		Both rising / falling EQ								
0		1		Only rising edge EQ								
1		0		Only falling edge EQ								
1		1		EQ Off								
EQ_DELAY[7:0]: Set GIP control signal EQ period												
EQ_DELAY [7:0]								GIP EQ Period				
0	0	0	0	0	0	0	0	0 OSC clock cycle				
0	0	0	0	0	0	0	1	8 OSC clock cycle				
0	0	0	0	0	0	1	0	16 OSC clock cycle				
0	0	0	0	0	0	1	1	24 OSC clock cycle				
0	0	0	0	0	1	0	0	32 OSC clock cycle				
.....								.....				
1	1	1	1	1	1	0	0	2016 OSC clock cycle				
1	1	1	1	1	1	0	1	2024 OSC clock cycle				
1	1	1	1	1	1	1	0	2032 OSC clock cycle				
1	1	1	1	1	1	1	1	2040 OSC clock cycle				
Description	Rising GIP EQ_DELAY				Falling GIP EQ_DELAY				VGH			
	SPON	/CON	VSSA	VGL	SPOFF	/COFF						
EQ_DELAY_HSYNC[3:0]: Set the EQ period in HSYNC width.												
EQ_DELAY_HSYNC[3]		EQ_DELAY_HSYNC[2]		EQ_DELAY_HSYNC[1]		EQ_DELAY_HSYNC[0]		EQ Period in HSYNC width				
0		0		0		0		Normal Driving				
0		0		0		1		1 x Hsync				
0		0		1		0		2 x Hsync				
0		0		1		1		3 x Hsync				
.....												
1		1		1		0		14 x Hsync				
1		1		1		1		15 x Hsync				

									
Restrictions	-								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th><th style="text-align: center;">Availability</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td style="text-align: center;">Sleep In or Booster Off</td><td style="text-align: center;">Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In or Booster Off	Yes								
Default	Refer to "6.1.2 User define command list table".								

### 5.18.21 SETGPO (D9h)

D9H	SETGPO									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	1	0	0	1	D9
1 <sup>st</sup> parameter	1	ESD_DET	-	-	-	-	-	-	-	-
2 <sup>nd</sup> parameter	1	EXT_PWR_CTRL	-	-	-	-	-	-	-	-
3 <sup>rd</sup> parameter	1	-	-	-	-	-	-	-	-	CABC_GPO[3:0]
4 <sup>th</sup> parameter	1	-	-	-	-	-	-	-	-	SDO_GPO[3:0]
Description	ESD_DET: ESD Det Pin.,normal state active hi-level,when ESD interference,ESD_DET become to low-level.  EXT_PWR_CTRL: normal state active when TE/TE1/CABC/SDO_GPO[3] set to b'1011,the GPO pin output EXT_PWR_CTRL, If EXT_PWR_CTRL active low-level, EXT_PWR_CTRL will auto enable to low-level.  TE_GPO[3:0]: set the output pin TE.  TE1_GPO[3:0] : set the output pin TE1.  CABC_GPO[3:0]: : set the output pin CABC.  SDO_GPO[3:0]: Set the output pin SDO.									
	TE/TE1/CABC/SDO_GPO[3]	TE/TE1/CABC/SDO_GPO[2]	TE/TE1/CABC/SDO_GPO[1]	TE/TE1/CABC/SDO_GPO[0]	TE/TE1/CABC/SDO Output signal					
	0	0	0	0	TE					
	0	0	0	1	TE1					
	0	0	1	0	CABC					
	0	0	1	1	HSYNC					
	0	1	0	0	VSYNC					
	0	1	0	1	DE					
	0	1	1	1	SDO					
	1	0	0	1	BC_CTRL					
	1	0	1	1	ESD_DET					
	Others			Inhibited						
Restrictions	SETEXTC turn on to enable this command									
Register Availability	Status				Availability					
	Normal Mode On, Idle Mode Off, Sleep Out				Yes					
	Normal Mode On, Idle Mode On, Sleep Out				Yes					
	Sleep In or Booster Off				Yes					

### 5.18.22 SETSENSOR (DEH)

DEH	SETSENSOR																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	1	1	1	1	0	DE								
1 <sup>st</sup> parameter	1	TSENS OR_EN	LT_EN	HT_EN				TEMP_GAP[2:0]		-								
Description	TSENSOR_EN: temperature enable bit. LT_EN: Low temp enable bit. HT_EN: High temp anable bit. TEMP_GAP[2:0]:																	
Restrictions	SETEXTC turn on to enable this command.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

### 5.18.23 SETGAMMA: Set red gamma curve related setting (E0h)

E0H	SETGAMMA									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	0	0	0	0	E0
1 <sup>st</sup> Parameter	1	-	-			VRP0[5:0]				-
2 <sup>nd</sup> parameter	1	-	-			VRP1[5:0]				-
3 <sup>rd</sup> parameter	1	-	-			VRP2[5:0]				-
4 <sup>th</sup> parameter	1	-	-			VRP3[5:0]				-
5 <sup>th</sup> parameter	1	-	-			VRP4[5:0]				-
6 <sup>th</sup> parameter	1	-	-			VRP5[5:0]				-
7 <sup>th</sup> parameter	1	-			PRP0[6:0]					-
8 <sup>th</sup> parameter	1	-			PRP1[6:0]					-
9 <sup>th</sup> parameter	1	-	-	-		PKP0[4:0]				-
10 <sup>th</sup> parameter	1	-	-	-		PKP1[4:0]				-
11 <sup>th</sup> parameter	1	-	-	-		PKP2[4:0]				-
12 <sup>th</sup> parameter	1	-	-	-		PKP3[4:0]				-
13 <sup>th</sup> parameter	1	-	-	-		PKP4[4:0]				-
14 <sup>th</sup> parameter	1	-	-	-		PKP5[4:0]				-
15 <sup>th</sup> parameter	1	-	-	-		PKP6[4:0]				-
16 <sup>th</sup> parameter	1	-	-	-		PKP7[4:0]				-
17 <sup>th</sup> parameter	1	-	-	-		PKP8[4:0]				-
18 <sup>th</sup> parameter						PKP9[4:0]				
19 <sup>th</sup> parameter						PKP10[4:0]				
20 <sup>th</sup> parameter						PKP11[4:0]				
21 <sup>st</sup> parameter						PKP12[4:0]				
22 <sup>nd</sup> parameter	1	-	-			VRN0[5:0]				-
23 <sup>rd</sup> parameter	1	-	-			VRN1[5:0]				-
24 <sup>th</sup> parameter	1	-	-			VRN2[5:0]				-
25 <sup>th</sup> parameter	1	-	-			VRN3[5:0]				-
26 <sup>th</sup> parameter	1	-	-			VRN4[5:0]				-
27 <sup>th</sup> parameter	1	-	-			VRN5[5:0]				-
28 <sup>th</sup> parameter	1	-			PRN0[6:0]					-
29 <sup>th</sup> parameter	1	-			PRN1[6:0]					-
30 <sup>th</sup> parameter	1	-				PKN0[4:0]				-
31 <sup>st</sup> parameter	1	-				PKN1[4:0]				-
32 <sup>nd</sup> parameter	1	-				PKN2[4:0]				-
33 <sup>rd</sup> parameter	1	-				PKN3[4:0]				-
34 <sup>th</sup> parameter	1	-	-	-		PKN4[4:0]				-
35 <sup>th</sup> parameter	1	-	-	-		PKN5[4:0]				-
36 <sup>th</sup> parameter	1	-	-	-		PKN6[4:0]				-
37 <sup>th</sup> parameter	1	-	-	-		PKN7[4:0]				-
38 <sup>th</sup> parameter	1	-	-	-		PKN8[4:0]				-
39 <sup>th</sup> parameter	1	-	-	-		PKN9[4:0]				
40 <sup>th</sup> parameter	1	-	-	-		PKN10[4:0]				
41 <sup>st</sup> parameter	1	-	-	-		PKN11[4:0]				
42 <sup>nd</sup> parameter	1	-	-	-		PKN12[4:0]				
Description	Register Groups	Positive Polarity	Negative Polarity	Description						
	Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor (PRP/N0) for center adjustment						
		PRP1 6-0	PRN1 6-0	Variable resistor (PRP/N1)for center adjustment						
	Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of VV12)						
		PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of VV20)						
		PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of VV28)						
		PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of VV40)						
		PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of VV76)						
		PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale VV100)						
		PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale VV132)						

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		PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale VV156)
		PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale VV180)
		PKP9 4-0	PKN9 4-0	32-to-1 selector (voltage level of VV 216)
		PKP10 4-0	PKN10 4-0	32-to-1 selector (voltage level of VV228 )
		PKP11 4-0	PKN11 4-0	32-to-1 selector (voltage level of grayscale VV236)
		PKP12 4-0	PKN412 4-0	32-to-1 selector (voltage level of grayscale VV243)
	Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
		VRP1 5-0	VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
		VRP2 5-0	VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
		VRP3 5-0	VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment
		VRP4 5-0	VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
		VRP5 5-0	VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment
Restriction	SETEXTC turn on to enable this command.			
Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In or Booster Off		Yes	

### 5.18.24 SETCEMODE (E4h)

E4H	SETCEMODE (Set color enhancement mode)																																																
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1	1	1	0	0	1	0	0	E4																																							
1 <sup>st</sup> parameter	1	HUE_MODE[1:0]	SE_MODE[1:0]	BE_MODE[1:0]	CE_MODE[1:0]					-																																							
2 <sup>nd</sup> parameter	1	-	-	-	-	-	-	-	DYN_C EH_EN	-																																							
Description	<p>This command is to set color enhancement mode.</p> <p>CE_MODE [1:0]: Set color saturation enhancement in static mode.</p> <p>BE_MODE [1:0]: Set brightness enhancement in static mode.</p> <p>SE_MODE [1:0]: Set sharpness enhancement in static mode.</p> <p>Enhance effort selection. When SE/BE/CE/HUE turn on, the enhancement magnitude depends on default gain setting which is read from the ROM table. And there are three magnitudes to be selected.</p> <table border="1"> <thead> <tr> <th>HUE/SE/BE/CE[1]</th> <th>HUE/SE/BE/CE[0]</th> <th>Enhance</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>Low</td> </tr> <tr> <td>1</td> <td>0</td> <td>Medium</td> </tr> <tr> <td>1</td> <td>1</td> <td>High</td> </tr> </tbody> </table> <p>DYN_CEH_EN: 0: STA mode, 1: DYN mode</p> <p>If DYN mode is selected, there are 3 kinds of enhancement defined by HIMAX can be chosen by 1<sup>st</sup> parameter</p> <p>If STA mode is selected, enhancement can be adjusted by E5h&amp;E6h</p> <p>Color Enhancement</p> <table border="1"> <thead> <tr> <th>Off</th> <th>Low</th> <th>Medium</th> <th>High</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p>Brightness Enhancement</p> <table border="1"> <thead> <tr> <th>Off</th> <th>Low</th> <th>Medium</th> <th>High</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p>Sharpness Enhancement</p> <table border="1"> <thead> <tr> <th>Off</th> <th>Low</th> <th>Medium</th> <th>High</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>										HUE/SE/BE/CE[1]	HUE/SE/BE/CE[0]	Enhance	0	0	Off	0	1	Low	1	0	Medium	1	1	High	Off	Low	Medium	High					Off	Low	Medium	High					Off	Low	Medium	High				
HUE/SE/BE/CE[1]	HUE/SE/BE/CE[0]	Enhance																																															
0	0	Off																																															
0	1	Low																																															
1	0	Medium																																															
1	1	High																																															
Off	Low	Medium	High																																														
Off	Low	Medium	High																																														
Off	Low	Medium	High																																														
Restrictions	SETEXTC turn on to enable this command.																																																

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

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## 5.18.25 SET CE (E5h)

E5H	SET CE (Set color enhancement, static/OTP)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Def Val
Command	0	1	1	1	0	0	1	0	1	E5
1 <sup>st</sup> parameter	1					MEAN_OFFSET_CE[7:0]				-
2 <sup>nd</sup> parameter	1	-	-	-			SG0_F[4:0]			-
3 <sup>rd</sup> parameter	1	-	-	-			SG64_F[4:0]			-
4 <sup>th</sup> parameter	1	-	-	-			SG128_F[4:0]			-
5 <sup>th</sup> parameter	1	-	-	-			SG192_F[4:0]			-
6 <sup>th</sup> parameter	1	-	-	-			SG255_F[4:0]			-
7 <sup>th</sup> parameter	1					TH_SAT[7:0]				-
8 <sup>th</sup> parameter	1					TH_WHITE[7:0]				-
9 <sup>th</sup> parameter	1					TH_COLOR[7:0]				-
10 <sup>th</sup> parameter	1					TH_GRAY[7:0]				-
11 <sup>th</sup> parameter	1				MEAN_OFFSET_BE[7:0]					-
12 <sup>th</sup> parameter	1	-	-	-		CG0_F[4:0]				-
13 <sup>th</sup> parameter	1	-	-	-		CG64_F[4:0]				-
14 <sup>th</sup> parameter	1	-	-	-		CG128_F[4:0]				-
15 <sup>th</sup> parameter	1	-	-	-		CG192_F[4:0]				-
16 <sup>th</sup> parameter	1	-	-	-		CG255_F[4:0]				-
17 <sup>th</sup> parameter	1				THC[7:0]					-
18 <sup>th</sup> parameter	1	-	-	-	-	EG2_F[1:0]	EG1_F[1:0]			-
19 <sup>th</sup> parameter	1				TH_RFL[7:0]					-
20 <sup>th</sup> parameter	1	-	-	-		SG16_F[4:0]				-
21 <sup>st</sup> parameter	1	-	-	-		SG32_F[4:0]				-
22 <sup>nd</sup> parameter	1	-	-	-		SG48_F[4:0]				-
23 <sup>rd</sup> parameter	1	-	-	-		SG80_F[4:0]				-
24 <sup>th</sup> parameter	1	-	-	-		SG96_F[4:0]				-
25 <sup>th</sup> parameter	1	-	-	-		SG112_F[4:0]				-
26 <sup>th</sup> parameter	1	-	-	-		SG144_F[4:0]				-
27 <sup>th</sup> parameter	1	-	-	-		SG160_F[4:0]				-
28 <sup>th</sup> parameter	1	-	-	-		SG176_F[4:0]				-
29 <sup>th</sup> parameter	1	-	-	-		SG208_F[4:0]				-
30 <sup>th</sup> parameter	1	-	-	-		SG224_F[4:0]				-
31 <sup>st</sup> parameter	1	-	-	-		SG240_F[4:0]				-
32 <sup>nd</sup> parameter	1	-	-	-		CG16_F[4:0]				-
33 <sup>rd</sup> parameter	1	-	-	-		CG32_F[4:0]				-
34 <sup>th</sup> parameter	1	-	-	-		CG48_F[4:0]				-
35 <sup>th</sup> parameter	1	-	-	-		CG80_F[4:0]				-
36 <sup>th</sup> parameter	1	-	-	-		CG96_F[4:0]				-
37 <sup>th</sup> parameter	1	-	-	-		CG112_F[4:0]				-
38 <sup>th</sup> parameter	1	-	-	-		CG144_F[4:0]				-
39 <sup>th</sup> parameter	1	-	-	-		CG160_F[4:0]				-
40 <sup>th</sup> parameter	1	-	-	-		CG176_F[4:0]				-
41 <sup>st</sup> parameter	1	-	-	-		CG208_F[4:0]				-
42 <sup>nd</sup> parameter	1	-	-	-		CG224_F[4:0]				-
43 <sup>rd</sup> parameter	1	-	-	-		CG240_F[4:0]				-
Description	No default value in this command									

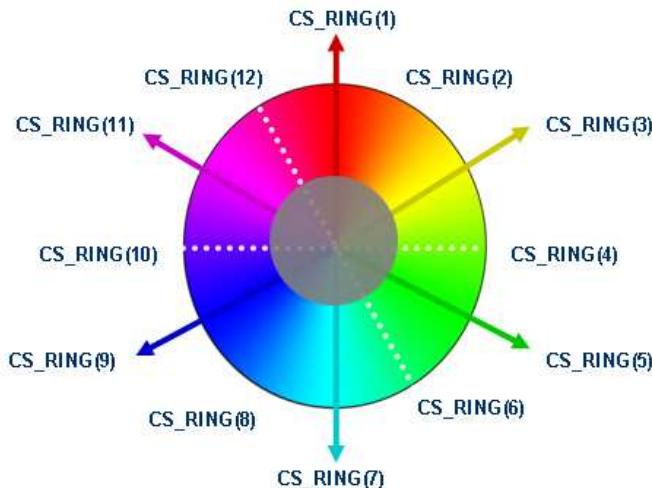
	<p>Parameters for CE function.</p> <p>MEAN_OFFSET_CE[7:0]: Def:00h      SG0_F[4:0] : L:00h; M:04h; H:08h; Def:00h      SG16[4:0] : L:02h; M:05h; H:08h; Def:02h      SG32[4:0] : L:04h; M:08h; H:09h; Def:03h      SG48[4:0] : L:06h; M:0Ah; H:0Ah; Def:04h      SG64_F[4:0]: L:08h; M:0Bh; H:0Eh; Def:06h      SG80[4:0] : L:08h; M:0Bh; H:0Eh; Def:06h      SG96[4:0] : L:08h; M:0Ah; H:0Bh; Def:05h      SG112[4:0] : L:07h; M:09h; H:0Bh; Def:05h      SG128_F[4:0]: L:06h; M:08h; H:0Ah; Def:04h      SG144[4:0] : L:06h; M:08h; H:0Ah; Def:04h      SG160[4:0] : L:06h; M:08h; H:0Ah; Def:04h      SG176[4:0] : L:05h; M:07h; H:09h; Def:03h      SG192_F[4:0]: L:04h; M:06h; H:08h; Def:02h      SG208[4:0] : L:03h; M:05h; H:06h; Def:02h      SG224[4:0] : L:02h; M:04h; H:05h; Def:01h      SG240[4:0] : L:01h; M:02h; H:03h; Def:01h      SG255_F[4:0]: L:00h; M:00h; H:00h; Def:00h      TH_SAT[7:0] : L:20h; M:20h; H:20h; Def:20h      TH_WHITE[7:0] : L:20h; M:20h; H:20h; Def:20h      TH_COLOR[7:0] : L:20h; M:20h; H:20h; Def:20h      TH_GRAY[7:0] : L:10h; M:10h; H:10h; Def:20h      TH_RFL[7:0] : L:20h; M:20h; H:20h; Def:20h</p> <p>Parameters for BE function</p> <p>MEAN_OFFSET_BE[7:0]: Def:00h      CG0_F[4:0] : L:00h; M:04h; H:08h; Def:00h      CG16[4:0] : L:02h; M:05h; H:09h; Def:02h      CG32[4:0] : L:03h; M:07h; H:0Ah; Def:04h      CG48[4:0] : L:05h; M:09h; H:0Bh; Def:06h      CG64_F[4:0]: L:08h; M:0Ah; H:0Ch; Def:08h      CG80[4:0] : L:08h; M:0Ah; H:0Ch; Def:08h      CG96[4:0] : L:07h; M:0Ah; H:0Bh; Def:07h      CG112[4:0] : L:07h; M:09h; H:0Bh; Def:07h      CG128_F[4:0]: L:06h; M:08h; H:0Ah; Def:06h      CG144[4:0] : L:06h; M:08h; H:0Ah; Def:06h      CG160[4:0] : L:05h; M:07h; H:0Ah; Def:05h      CG176[4:0] : L:05h; M:07h; H:09h; Def:05h      CG192_F[4:0]: L:04h; M:06h; H:08h; Def:04h      CG208[4:0] : L:03h; M:05h; H:07h; Def:03h      CG224[4:0] : L:02h; M:04h; H:06h; Def:02h      CG240[4:0] : L:01h; M:03h; H:03h; Def:01h      CG255_F[4:0]: L:00h; M:00h; H:00h; Def:00h      THC[7:0]: L:80h; M:80h; H:80h; Def:80h</p> <p>Parameters for SE function</p> <p>{ EG2_F[1:0],EG1_F[1:0] }: L:0Ah; M: 09h; H:08h; Def:0Eh</p>								
Restrictions	SETEXTC turn on to enable this command.								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In or Booster Off	Yes								

### 5.18.26 SETCESEL: Enable color enhance (E6h)

E6H	SETCESEL(Enable color enhancement)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Def Val
Command	0	1	1	1	0	0	1	1	0	E6
1 <sup>st</sup> parameter	1	ENCH00_SEL[6:0]								ENCH00_SAMPLE_E_SEL
2 <sup>nd</sup> parameter	1	ENCH01_SW[4:0]				ENCH01_SE_OFF	ENCH01_BE_OFF	ENCH01_CE_OFF		-
3 <sup>rd</sup> parameter	1	ENCH02_DS[4:0]				ENCH02_SE_DS	ENCH02_BE_DS	ENCH02_CE_DS		-
4 <sup>th</sup> parameter	1	ENCH03_reg[7:0]								-
5 <sup>th</sup> parameter	1	ENCH04_reg[7:0]								-
6 <sup>th</sup> parameter	1	ENCH05_reg[7:0]								-
7 <sup>th</sup> parameter	1	ENCH06_reg[7:0]								-
8 <sup>th</sup> parameter	1	ENCH07_reg[7:0]								-
9 <sup>th</sup> parameter	1	ENCH08_reg[7:0]								-
10 <sup>th</sup> parameter	1	ENCH09_reg[7:0]								-
11 <sup>th</sup> parameter	1	ENCH10_reg[7:0]								-
12 <sup>th</sup> parameter	1	ENCH11_reg[7:0]								-
13 <sup>th</sup> parameter	1	ENCH12_reg[7:0]								-
14 <sup>th</sup> parameter	1	ENCH13_reg[7:0]								-
15 <sup>th</sup> parameter	1	ENCH14_reg[7:0]								-
16 <sup>th</sup> parameter	1	ENCH15_reg[7:0]								-
17 <sup>th</sup> parameter	1	ENCH16_reg[7:0]								-
218 <sup>th</sup> parameter	1	ENCH17_reg[7:0]								-
19 <sup>th</sup> parameter	1	ENCH18_reg[7:0]								-
20 <sup>th</sup> parameter	1	ENCH19_reg[7:0]								-
21 <sup>st</sup> parameter	1	ENCH20_reg[7:0]								-
22 <sup>nd</sup> parameter	1	ENCH21_reg[7:0]								-
23 <sup>rd</sup> parameter	1	ENCH22_reg[7:0]								-
24 <sup>th</sup> parameter	1	ENCH23_reg[7:0]								-
25 <sup>th</sup> parameter	1	ENCH24_reg[7:0]								-
26 <sup>th</sup> parameter	1	ENCH25_reg[7:0]								-
27 <sup>th</sup> parameter	1	ENCH26_reg[7:0]								-
28 <sup>th</sup> parameter	1	ENCH27_reg[7:0]								-
29 <sup>th</sup> parameter	1	ENCH28_reg[7:0]								-
30 <sup>th</sup> parameter	1	ENCH29_reg[7:0]								-
31 <sup>st</sup> parameter	1	ENCH30_reg[7:0]								-
32 <sup>nd</sup> parameter	1	ENCH31_reg[7:0]								-
33 <sup>rd</sup> parameter	1	ENCH32_reg[7:0]								-
34 <sup>th</sup> parameter	1	ENCH33_reg[7:0]								-
35 <sup>th</sup> parameter	1	REG_skin00[7:0]								-
36 <sup>th</sup> parameter	1	REG_skin01[7:0]								-
37 <sup>th</sup> parameter	1	REG_skin02[7:0]								-
38 <sup>th</sup> parameter	1	RO_DAVG[7:0]								(RO)
39 <sup>th</sup> parameter	1	RO_YAVG[7:0]								(RO)
Description	No default value in this command, except 4 <sup>th</sup> ,5 <sup>th</sup> ,35 <sup>th</sup> ,36 <sup>th</sup> ,37 <sup>th</sup> keep the default value  ENCH00_sample_sel: ENCH00_SEL: ENCH01_CE_OFF:									

ENCH01\_BE\_OFF:  
 ENCH01\_SE\_OFF:  
 ENCH01\_SW:  
 ENCH02\_CE\_DS:  
 ENCH02\_BE\_DS:  
 ENCH02\_SE\_DS:  
 ENCH02\_DS:  
 ENCH0x\_reg:  
 RO\_DAVG: (Read Only)  
 RO\_YAVG: (Read Only)

12 hues can be adjusted to enhance the specified colors.



CS\_RING(1) is adjusted by ENCH05\_reg[7:0]

CS\_RING(2) is adjusted by ENCH06\_reg[7:0]

.....

CS\_RING(11) is adjusted by ENCH15\_reg[7:0]

CS\_RING(12) is adjusted by ENCH16\_reg[7:0]

CS\_RING1~12 setting range is 00h~20h

Restrictions	SETEXTC turn on to enable this command	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

### 5.18.27 SETREADINDEX: Set SPI Read Index (FEh)

FEH	SET SPI READ INDEX (Set SPI READ Command Address)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	1	1	1	1	1	0	FE								
1 <sup>st</sup> parameter	1	CMD_ADD[7:0]								-								
Description	SET SPI Read Command Address for User defined Command.																	
Restrictions	SETEXTC turn on to enable this command																	
Register Availability	Status					Availability												
	Normal Mode On, Idle Mode Off, Sleep Out					Yes												
	Normal Mode On, Idle Mode On, Sleep Out					Yes												
	Sleep In or Booster Off					Yes												

## 6. Layout Recommendation

### 6.1 Maximum layout resistance

Name	Type	Maximum series resistance	Unit
VDD1	Power supply	5	Ω
VDD3	Power supply	5	Ω
VPP	Power supply	5	Ω
HS_VCC	Power supply	5	Ω
HS_VSS	Power supply	5	Ω
VSSD	Power supply	5	Ω
VSSA	Power supply	5	Ω
VSSAC	Power supply	20	Ω
BS[2:0]	Input	100	Ω
PCCS[1:0]	Input	100	Ω
CSX, DCX, RESX, SCL	Input	100	Ω
HSYNC, DE, VSYNC, PCLK	Input	100	Ω
SDI	Input	100	Ω
SDO	Output	100	Ω
DB[23:0]	Input	100	Ω
CABC_PWM_OUT, TE, TE1	Output	100	Ω
VCOM	Output	10	Ω
VCOMR	Input	100	Ω
HS_CP, HS_CN	Input	5	Ω
HS_D0P, HS_D0N	Input / Output	5	Ω
HS_D1P, HS_D1N	Input	5	Ω
HS_D2P, HS_D2N	Input	5	Ω
HS_D3P, HS_D3N	Input	5	Ω
VDDD	Capacitor Connection	5	Ω
VCL	Capacitor Connection	10	Ω
VSP, VSN	Capacitor Connection	10	Ω
VSPC, VSNC	Input	50	Ω
VSPR, VSNR	Capacitor Connection	50	Ω
VREF	Capacitor Connection	20	Ω
VGH, VGL	Capacitor Connection	10	Ω
HS_LDO	Capacitor Connection	5	Ω
OSC	Input	100	Ω
C21P, C21N, C22P, C22N, C31P, C31N, C41P, C41N	Capacitor Connection	5	Ω
VCSW1, VCSW2	Output	10	Ω
GOUT_L1~22, GOUT_R1~22	Output	10	Ω
TEST[2:0]	Input	100	Ω
FRM	Input	100	Ω
VTESTOUTP, VTESTOUTN	Output	100	Ω

Table 6.1: Maximum Layout Resistance

## 6.2 External components connection

### HX5186-A/B/C mode:

Pad Name	Symbol	Connection	Typical Component Value
VDD3	C1	Connect to Capacitor (Max 10V): VDD3 ---(+)---   --- (-)----VSSA	2.2 $\mu$ F
VDD1	C2	Connect to Capacitor (Max 6V): VDD1 ---(+)---   --- (-)----VSSA	2.2 $\mu$ F
HS_VCC	C3	Connect to Capacitor (Max 6V): HS_VCC ---(+)---   --- (-)----VSSA	2.2 $\mu$ F
C41P – C41N	C4	Connect to Capacitor (Max 6V): C41P ---(+)---   --- (-)----C41N	1.0 $\mu$ F
	C5	Connect to Capacitor (Max 6V): VCL ---(-)---   --- (+)---- VSSA	1.0 $\mu$ F
VCL	D3	Connect to Schottky Diode(VR $\geq$ 30V): VSSA ---(-)---  ◀--- (+)---- VCL	VF < 0.4V / 20mA @ 25°C, VR $\geq$ 30V (Recommended diode: RB521S-30)
C21P – C21N	C6	Connect to Capacitor (Max 16V): C21P ---(+)---   --- (-)----C21N	1.0 $\mu$ F
C22P – C22N	C7	Connect to Capacitor (Max 16V): C22P ---(+)---   --- (-)----C22N	1.0 $\mu$ F
C31P – C31N	C8	Connect to Capacitor (Max 16V): C31P ---(+)---   --- (-)----C31N	1.0 $\mu$ F
	C9	Connect to Capacitor (Max 25V): VGL ---(-)---   --- (+)---- VSSA	1.0 $\mu$ F
VGL	D2	Connect to Schottky Diode(VR $\geq$ 30V): VSSA ---(-)---  ◀--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR $\geq$ 30V (Recommended diode: RB521S-30)
VGH	C10	Connect to Capacitor (Max 25V): VGH ---(+)---   --- (-)---- VSSA	1.0 $\mu$ F
VREF	C12	Connect to Capacitor (Max 6V): VREF ---(+)---   --- (-)----VSSA	1.0 $\mu$ F
VCOM	C14	Connect to Capacitor (Max 6V): VCOM ---(-)---   --- (+)---- VSSA	1.0 $\mu$ F
VSNR	C15	Connect to Capacitor (Max 10V): VSNR ---(+)---   --- (-)----VSSA	1.0 $\mu$ F
VSPR	C16	Connect to Capacitor (Max 10V): VSPR ---(-)---   --- (+)----VSSA	1.0 $\mu$ F
VDDD	C17	Connect to Capacitor (Max 6V): VDDD ---(+)---   --- (-)----VSSA	1.0 $\mu$ F
HS_LDO	C18	Connect to Capacitor (Max 6V): HS_LDO ---(+)---   --- (-)----HS_VSS	1.0 $\mu$ F
VSP	C19	Connect to Capacitor (Max 10V): VSP ---(+)---   --- (-)----VSSA	2.2 $\mu$ F
VSN	C20	Connect to Capacitor (Max 10V): VSN ---(-)---   --- (+)----VSSA	2.2 $\mu$ F
HX5186-A/B/C	U1	Please refer HX5186-A/B/C datasheet	-
HX5186	C21	Please refer HX5186-A datasheet	1.0uF
HX5186	C22	Please refer HX5186-A datasheet	1.0uF
HX5186	C23	Please refer HX5186-A datasheet	1.0uF

Table 6.2: HX5186-A/B/C mode external components

**PFM type A mode:**

Pad Name	Symbol	Connection	Typical Component Value
VDD3	C1	Connect to Capacitor (Max 10V): VDD3 ---(+----   --- (-)----VSSA	2.2 $\mu$ F
VDD1	C2	Connect to Capacitor (Max 6V): VDD1 ---(+----   --- (-)----VSSA	2.2 $\mu$ F
HS_VCC	C3	Connect to Capacitor (Max 6V): HS_VCC ---(+----   --- (-)----VSSA	2.2 $\mu$ F
C41P – C41N	C4	Connect to Capacitor (Max 6V): C41P ---(+----   --- (-)----C41N	1.0 $\mu$ F
VCL	C5	Connect to Capacitor (Max 6V): VCL ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
	D3	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----  ◀--- (+)---- VCL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
C21P – C21N	C6	Connect to Capacitor (Max 16V): C21P ---(+----   --- (-)----C21N	1.0 $\mu$ F
C22P – C22N	C7	Connect to Capacitor (Max 16V): C22P ---(+----   --- (-)----C22N	1.0 $\mu$ F
C31P – C31N	C8	Connect to Capacitor (Max 16V): C31P ---(+----   --- (-)----C31N	1.0 $\mu$ F
VGL	C9	Connect to Capacitor (Max 25V): VGL ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----  ◀--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VGH	C10	Connect to Capacitor (Max 25V): VGH ---(+----   --- (-)---- VSSA	1.0 $\mu$ F
VREF	C12	Connect to Capacitor (Max 6V): VREF ---(+----   --- (-)----VSSA	1.0 $\mu$ F
VCOM	C14	Connect to Capacitor (Max 6V): VCOM ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
VSNR	C15	Connect to Capacitor (Max 10V): VSNR ---(+----   --- (-)----VSSA	1.0 $\mu$ F
VSPR	C16	Connect to Capacitor (Max 10V): VSPR ---(-----   --- (+)----VSSA	1.0 $\mu$ F
VDDD	C17	Connect to Capacitor (Max 6V): VDDD ---(+----   --- (-)----VSSA	1.0 $\mu$ F
HS_LDO	C18	Connect to Capacitor (Max 6V): HS_LDO ---(+----   --- (-)----HS_VSS	1.0 $\mu$ F
VSN	C19	Connect to Capacitor (Max 10V): VSN ---(-----   --- (+)----VSSA	4.7 $\mu$ F
VSP	C20	Connect to Capacitor (Max 10V): VSP ---(+----   --- (-)----VSSA	4.7 $\mu$ F
PFM	L1	Inductance,please refer PFM type A connection.	10.0uH
PFM	D2	Schottky Diode , please refer PFM type A connection.	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	D3	Schottky Diode , please refer PFM type A connection.	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	SW1	MOS switch, please refer PFM type A connection.	-
PFM	SW2	MOS switch, please refer PFM type A connection.	-

**Table 6.3: PFM type A external components**

**PFM type C mode:**

Pad Name	Symbol	Connection	Typical Component Value
VDD3	C1	Connect to Capacitor (Max 10V): VDD3 ---(+----   --- (-)----VSSA	2.2 $\mu$ F
VDD1	C2	Connect to Capacitor (Max 6V): VDD1 ---(+----   --- (-)----VSSA	2.2 $\mu$ F
HS_VCC	C3	Connect to Capacitor (Max 6V): HS_VCC ---(+----   --- (-)----VSSA	2.2 $\mu$ F
C41P – C41N	C4	Connect to Capacitor (Max 6V): C41P ---(+----   --- (-)----C41N	1.0 $\mu$ F
VCL	C5	Connect to Capacitor (Max 6V): VCL ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
	D3	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----  ◀--- (+)---- VCL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
C21P – C21N	C6	Connect to Capacitor (Max 16V): C21P ---(+----   --- (-)----C21N	1.0 $\mu$ F
C22P – C22N	C7	Connect to Capacitor (Max 16V): C22P ---(+----   --- (-)----C22N	1.0 $\mu$ F
C31P – C31N	C8	Connect to Capacitor (Max 16V): C31P ---(+----   --- (-)----C31N	1.0 $\mu$ F
VGL	C9	Connect to Capacitor (Max 25V): VGL ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----  ◀--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VGH	C10	Connect to Capacitor (Max 25V): VGH ---(+----   --- (-)---- VSSA	1.0 $\mu$ F
VREF	C12	Connect to Capacitor (Max 6V): VREF ---(+----   --- (-)----VSSA	1.0 $\mu$ F
VCOM	C14	Connect to Capacitor (Max 6V): VCOM ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
VSNR	C15	Connect to Capacitor (Max 10V): VSNR ---(+----   --- (-)----VSSA	1.0 $\mu$ F
VSPR	C16	Connect to Capacitor (Max 10V): VSPR ---(-----   --- (+)----VSSA	1.0 $\mu$ F
VDDD	C17	Connect to Capacitor (Max 6V): VDDD ---(+----   --- (-)----VSSA	1.0 $\mu$ F
HS_LDO	C18	Connect to Capacitor (Max 6V): HS_LDO ---(+----   --- (-)----HS_VSS	1.0 $\mu$ F
VSN	C19	Connect to Capacitor (Max 10V): VSN ---(-----   --- (+)----VSSA	4.7 $\mu$ F
VSP	C20	Connect to Capacitor (Max 10V): VSP ---(+----   --- (-)----VSSA	4.7 $\mu$ F
PFM	L1	Inductance,please refer PFM type C connection.	10uH
PFM	D2	Schottky Diode , please refer PFM type C connection.	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	D3	Schottky Diode , please refer PFM type C connection.	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	D4	Schottky Diode , please refer PFM type C connection.	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
PFM	SW1	MOS switch, please refer PFM type C connection.	-
PFM	C21	Capacitor, please refer PFM type C connection.	1.0 $\mu$ F

Table 6.4: PFM type C external components

**PFM type D mode:**

Pad Name	Symbol	Connection	Typical Component Value
VDD3	C1	Connect to Capacitor (Max 10V): VDD3 ---(+----   --- (-)----VSSA	2.2 $\mu$ F
VDD1	C2	Connect to Capacitor (Max 6V): VDD1 ---(+----   --- (-)----VSSA	2.2 $\mu$ F
HS_VCC	C3	Connect to Capacitor (Max 6V): HS_VCC ---(+----   --- (-)----VSSA	2.2 $\mu$ F
C41P – C41N	C4	Connect to Capacitor (Max 6V): C41P ---(+----   --- (-)----C41N	1.0 $\mu$ F
VCL	C5	Connect to Capacitor (Max 6V): VCL ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
	D3	Connect to Schottky Diode(VR $\geq$ 30V): VSSA ---(-----   --- (+)---- VCL	VF < 0.4V / 20mA @ 25°C, VR $\geq$ 30V (Recommended diode: RB521S-30)
C21P – C21N	C6	Connect to Capacitor (Max 16V): C21P ---(+----   --- (-)----C21N	1.0 $\mu$ F
C22P – C22N	C7	Connect to Capacitor (Max 16V): C22P ---(+----   --- (-)----C22N	1.0 $\mu$ F
C31P – C31N	C8	Connect to Capacitor (Max 16V): C31P ---(+----   --- (-)----C31N	1.0 $\mu$ F
VGL	C9	Connect to Capacitor (Max 25V): VGL ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
	D1	Connect to Schottky Diode(VR $\geq$ 30V): VSSA ---(-----   --- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR $\geq$ 30V (Recommended diode: RB521S-30)
VGH	C10	Connect to Capacitor (Max 25V): VGH ---(+----   --- (-)---- VSSA	1.0 $\mu$ F
VREF	C12	Connect to Capacitor (Max 6V): VREF ---(+----   --- (-)----VSSA	1.0 $\mu$ F
VCOM	C14	Connect to Capacitor (Max 6V): VCOM ---(-----   --- (+)---- VSSA	1.0 $\mu$ F
VSNR	C15	Connect to Capacitor (Max 10V): VSNR ---(+----   --- (-)----VSSA	1.0 $\mu$ F
VSPR	C16	Connect to Capacitor (Max 10V): VSPR ---(-----   --- (+)----VSSA	1.0 $\mu$ F
VDDD	C17	Connect to Capacitor (Max 6V): VDDD ---(+----   --- (-)----VSSA	1.0 $\mu$ F
HS_LDO	C18	Connect to Capacitor (Max 6V): HS_LDO ---(+----   --- (-)----HS_VSS	1.0 $\mu$ F
VSN	C19	Connect to Capacitor (Max 10V): VSN ---(-----   --- (+)----VSSA	4.7 $\mu$ F
VSP	C20	Connect to Capacitor (Max 10V): VSP ---(+----   --- (-)----VSSA	4.7 $\mu$ F
PFM	L1	Inductance,please refer PFM type D connection.	10.0uH
PFM	D2	Schottky Diode , please refer PFM type D connection.	VF < 0.4V / 20mA @ 25°C, VR $\geq$ 30V (Recommended diode: RB521S-30)
PFM	SW1	MOS switch, please refer PFM type Dconnection.	-

Table 6.5: PFM type D external components

**External VSP / VSN / VGH / VGL mode:**

Pad Name	Symbol	Connection	Typical Component Value
VSP	C1	Connect to Capacitor (Max 10V): VSP ---(+)---   --- (-)---VSSA	2.2 $\mu$ F
VSN	C2	Connect to Capacitor (Max 10V): VSN ---(-)---   --- (+)---VSSA	2.2 $\mu$ F
VDD3	C3	Connect to Capacitor (Max 6V): VDD3 ---(+)---   --- (-)---VSSA	2.2 $\mu$ F
HS_VCC	C4	Connect to Capacitor (Max 6V): HS_VCC ---(+)---   --- (-)---VSSA	2.2 $\mu$ F
VDD3	C5	Connect to Capacitor (Max 10V): VDD3 ---(+)---   --- (-)---VSSA	2.2 $\mu$ F
C41P – C41N	C6	Connect to Capacitor (Max 6V): C41P ---(+)---   --- (-)---C41N	1.0 $\mu$ F
VCL	C5	Connect to Capacitor (Max 6V): VCL ---(-)---   --- (+)--- VSSA	1.0 $\mu$ F
	D3	Connect to Schottky Diode(VR≥30V): VSSA ---(-)---  ↗--- (+)--- VCL (Recommended diode: RB521S-30)	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VGL	C8	Connect to Capacitor (Max 25V): VGL ---(-)---   --- (+)--- VSSA	1.0 $\mu$ F
	D1	Connect to Schottky Diode(VR≥30V): VSSA ---(-)---  ↗--- (+)--- VGL (Recommended diode: RB521S-30)	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VGH	C9	Connect to Capacitor (Max 25V): VGH ---(+)---   --- (-)--- VSSA	1.0 $\mu$ F
VREF	C11	Connect to Capacitor (Max 6V): VREF ---(+)---   --- (-)---VSSA	1.0 $\mu$ F
VCOM	C13	Connect to Capacitor (Max 6V): VCOM ---(-)---   --- (+)--- VSSA	1.0 $\mu$ F
VSNR	C14	Connect to Capacitor (Max 10V): VSNR ---(+)---   --- (-)---VSSA	1.0 $\mu$ F
VSPR	C15	Connect to Capacitor (Max 10V): VSPR ---(-)---   --- (+)---VSSA	1.0 $\mu$ F
VDDD	C16	Connect to Capacitor (Max 6V): VDDD ---(+)---   --- (-)---VSSA	1.0 $\mu$ F
HS_LDO	C17	Connect to Capacitor (Max 6V): HS_LDO ---(+)---   --- (-)---HS_VSS	1.0 $\mu$ F

Table 6.6: External VDD3 / VSP / VSN / VGH / VGL external components

**External VSP / VSN mode:**

Pad Name	Symbol	Connection	Typical Component Value
VSP	C1	Connect to Capacitor (Max 10V): VSP ---(+)---   --- (-)---VSSA	2.2 $\mu$ F
VSN	C2	Connect to Capacitor (Max 10V): VSN ---(-)---   --- (+)---VSSA	2.2 $\mu$ F
VDD1	C3	Connect to Capacitor (Max 6V): VDD1 ---(+)---   --- (-)---VSSA	2.2 $\mu$ F
HS_VCC	C4	Connect to Capacitor (Max 6V): HS_VCC ---(+)---   --- (-)---VSSA	2.2 $\mu$ F
VDD3	C5	Connect to Capacitor (Max 10V): VDD3 ---(+)---   --- (-)---VSSA	2.2 $\mu$ F
C41P – C41N	C6	Connect to Capacitor (Max 6V): C41P ---(+)---   --- (-)---C41N	1.0 $\mu$ F
VCL	C5	Connect to Capacitor (Max 6V): VCL ---(-)---   --- (+)--- VSSA	1.0 $\mu$ F
	D3	Connect to Schottky Diode(VR $\geq$ 30V): VSSA ---(-)---   --- (+)--- VCL (Recommended diode: RB521S-30)	VF < 0.4V / 20mA @ 25°C, VR $\geq$ 30V (Recommended diode: RB521S-30)
C21P – C21N	C8	Connect to Capacitor (Max 16V): C21P ---(+)---   --- (-)---C21N	1.0 $\mu$ F
C22P – C22N	C9	Connect to Capacitor (Max 16V): C22P ---(+)---   --- (-)---C22N	1.0 $\mu$ F
C31P – C31N	C10	Connect to Capacitor (Max 16V): C31P ---(+)---   --- (-)---C31N	1.0 $\mu$ F
VGL	C11	Connect to Capacitor (Max 25V): VGL ---(-)---   --- (+)--- VSSA	1.0 $\mu$ F
	D1	Connect to Schottky Diode(VR $\geq$ 30V): VSSA ---(-)---   --- (+)--- VGL (Recommended diode: RB521S-30)	VF < 0.4V / 20mA @ 25°C, VR $\geq$ 30V (Recommended diode: RB521S-30)
VGH	C12	Connect to Capacitor (Max 25V): VGH ---(+)---   --- (-)--- VSSA	1.0 $\mu$ F
VREF	C14	Connect to Capacitor (Max 6V): VREF ---(+)---   --- (-)---VSSA	1.0 $\mu$ F
VCOM	C16	Connect to Capacitor (Max 6V): VCOM ---(-)---   --- (+)--- VSSA	1.0 $\mu$ F
VSNR	C17	Connect to Capacitor (Max 10V): VSNR ---(+)---   --- (-)---VSSA	1.0 $\mu$ F
VSPR	C18	Connect to Capacitor (Max 10V): VSPR ---(-)---   --- (+)---VSSA	1.0 $\mu$ F
VDDD	C19	Connect to Capacitor (Max 6V): VDDD ---(+)---   --- (-)---VSSA	1.0 $\mu$ F
HS_LDO	C20	Connect to Capacitor (Max 6V): HS_LDO ---(+)---   --- (-)---HS_VSS	1.0 $\mu$ F

Table 6.7: External VDD3 / VSP / VSN external components

## 7. Electrical Characteristics

### 7.1 Absolute maximum ratings

The absolute maximum ratings are listed on Table 7.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDD1~ VSSD	V	-0.3 to +3.6	Note <sup>(1),(2)</sup>
Power Supply Voltage 3	VDD3 ~ VSSA	V	-0.3 to +3.6	Note <sup>(1)(4)</sup>
Power Supply Voltage 4	HS_VCC ~ HS_VSS	V	-0.3 to +3.6	Note <sup>(1)(5)</sup>
Power Supply Voltage 5	VSP ~ VSSA	V	-0.3 to +6.6	Note <sup>(6)</sup>
Power Supply Voltage 6	VSSA ~ VSN	V	0 to -6.6	Note <sup>(7)</sup>
Power Supply Voltage 7	VGH ~ VSSA	V	-0.3 to +19.6	Note <sup>(8)</sup>
Power Supply Voltage 8	VSSA ~ VGL	V	0 to -16	Note <sup>(9)</sup>
Operating Temperature	Topr	°C	-40 to +85	Note <sup>(10)</sup>
Storage Temperature	Tstg	°C	-55 to +110	Note <sup>(11)</sup>
Input Voltage	V <sub>IN</sub>	V	-0.3 to VDD1+0.3	Note <sup>(12)</sup>
HS Input Voltage	V <sub>HSIN</sub>	V	-0.3 to +2	Note <sup>(13)</sup>

**Note:** (1) VDD1, VSSD must be maintained.

(2) To make sure  $VDD1 \geq VSSD$ .

(4) To make sure  $VDD3 \geq VSSA$ .

(5) To make sure  $HS\_VCC \geq HS\_VSS$ .

(6) To make sure  $VSP \geq VSSA$ .

(7) To make sure  $VSSA \geq VSN$

(8) To make sure  $VGH \geq VSSA$ .

(9) To make sure  $VSSA \geq VGL$ ,  $VGH + |VGL| < 32V$

(10) For die and wafer products, specified up to +85°C.

(11) This temperature specifications apply to the TCP package.

(12) This specifications include input signals but without following: CP, CN, D0P, D0N, D1P, D1N, D2P, D2N, D3P, D3N.

(13) This specifications include following signals: CP, CN, D0P, D0N, D1P, D1N, D2P, D2N, D3P, D3N.

**Table 7.1: Absolute maximum rating**

## 7.2 DC characteristics

(VDD3=2.5 ~ 3.6V, VDD1=1.65~3.6V, TA=-40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V <sub>IH</sub>	V	VDD1= 1.65 ~ 3.6V VDD3= 2.5 ~ 3.6V	0.7 V <sub>DD1</sub>	-	VDD1	-
Input low voltage	V <sub>IL</sub>	V		0	-	0.3 V <sub>DD1</sub>	-
VPP	V <sub>IH</sub>	V	VPP	7.25	7.5	7.75	(1)
	V <sub>IL</sub>	V					
Output high voltage (SDO, CABC_PWM_OUT)	V <sub>OH1</sub>	V	I <sub>OH</sub> = -1.0 mA	0.8 V <sub>DD1</sub>	-	VDD1	-
Output low voltage (SDO, CABC_PWM_OUT)	V <sub>OL1</sub>	V	VDD1= 1.65 ~ 3.6V I <sub>OL</sub> = 1.0 mA	0	-	0.2 V <sub>DD1</sub>	-
Logic High level input current	I <sub>IH</sub>	uA	VSYNC, HSYNC	-	-	1	-
			RESX, DCX, CSX, SCL	-	-	1	-
	I <sub>IHD</sub>	uA	DB[23:0], SDI, DCX	-	-	1	-
			DB[23:0]	-	-	1	-
Logic Low level input current	I <sub>IL</sub>	uA	VSYNC, HSYNC	-1	-	-	-
			RESX, DCX, CSX, SCL	-1	-	-	-
	I <sub>ILD</sub>	uA	DB[23:0], SDI, DCX	-1	-	-	-
			DB[23:0]	-1	-	-	-
Current consumption standby mode (VDD3-VSSA)	I <sub>ST(VDD)</sub>	µA	VDD3/HS_VCC=2.8V, VDD1=1.8V TA =25°C (DSI Ultra Low Power mode)	-	10	30	-
Current consumption standby mode ( VDD1– VSSD)	I <sub>ST(VDD1)</sub>	µA		-	10	30	-
Current consumption standby mode which include HS_VCC ( HS_VCC-HS_VSS)	I <sub>ST(VDD1)</sub>	µA		-	10	30	-
Oscillator tolerance	△OSC	%	T <sub>A</sub> =25°C	-3	-	3	-
			T <sub>A</sub> =-40°C~85°C	-5	-	5	-

**Note:** (1) The VPP pin is open on normal mode and in used while OTP programming condition.

**Table 7.2: DC characteristic**

## 7.3 AC characteristics

### 7.3.1 DBI Type C interface characteristics

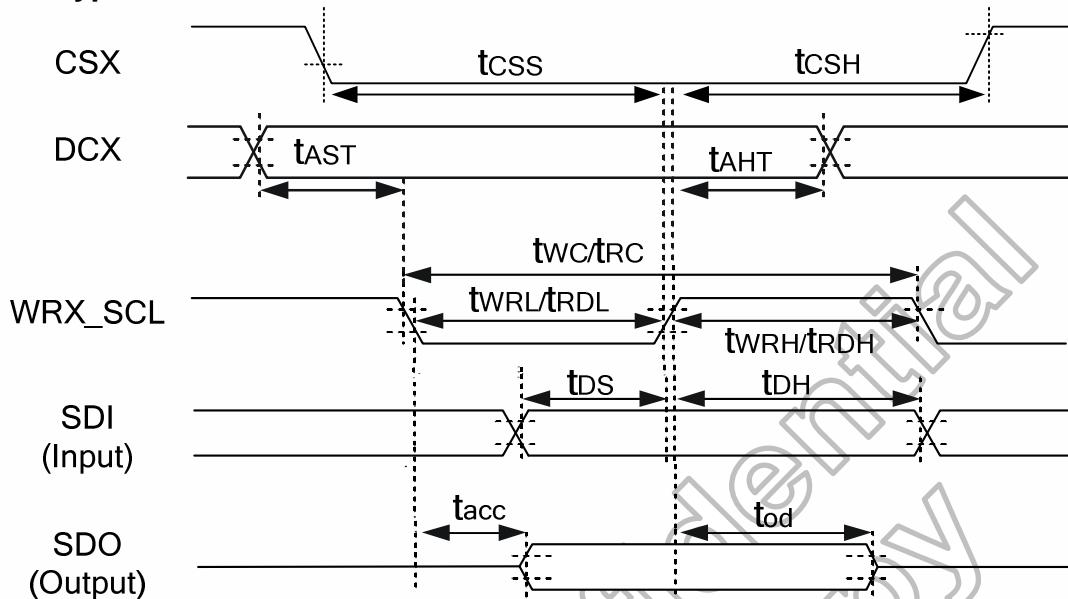


Figure 7.1: DBI Type C interface characteristics

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V,  $T_A = 25^\circ\text{C}$ )

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	$t_{CSS}$	Chip select setup time (Write)	40	-	ns	-
	$t_{CSH}$	Chip select setup time (Read)	40	-	ns	-
DCX	$t_{AST}$	Address setup time	10	-	ns	-
	$t_{AHT}$	Address hold time (Write/Read)	10	-	ns	-
WRX_SCL (Write)	$t_{WC}$	Write cycle	100	-	ns	-
	$t_{WRH}$	Control pulse "H" duration	40	-	ns	-
	$t_{WRL}$	Control pulse "L" duration	40	-	ns	-
WRX_SCL (Read)	$t_{RC}$	Read cycle	150	-	ns	-
	$t_{RDH}$	Control pulse "H" duration	60	-	ns	-
	$t_{RDL}$	Control pulse "L" duration	60	-	ns	-
SDI/SDO (Input)	$t_{DS}$	Data setup time	30	-	ns	For maximum $C_L=30\text{pF}$ For minimum $C_L=8\text{pF}$
	$t_{DT}$	Data hold time	30	-	ns	
SDI/SDO (Output)	$t_{RACC}$	Read access time	10	-	ns	For maximum $C_L=30\text{pF}$ For minimum $C_L=8\text{pF}$
	$t_{OD}$	Output disable time	10	50	ns	

Note: The input signal rise time and fall time ( $t_r, t_f$ ) is specified at 15 ns or less.

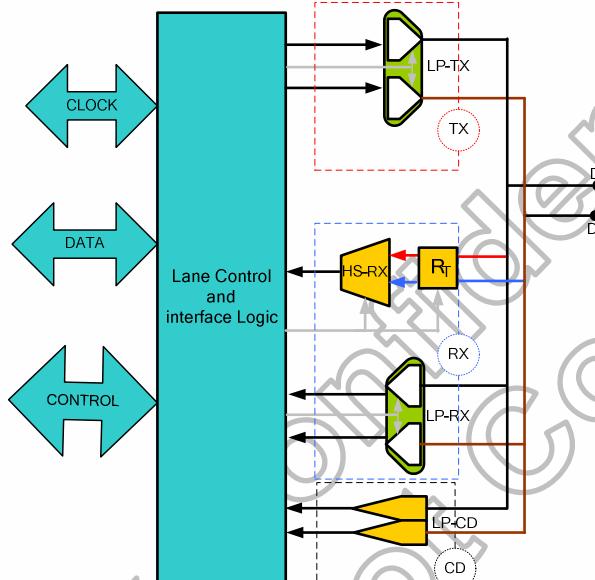
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 7.3: DBI Type C interface characteristics

### 7.3.2 DSI D-PHY electrical characteristics

#### 7.3.2.1 Electrical characteristics of D-PHY layer

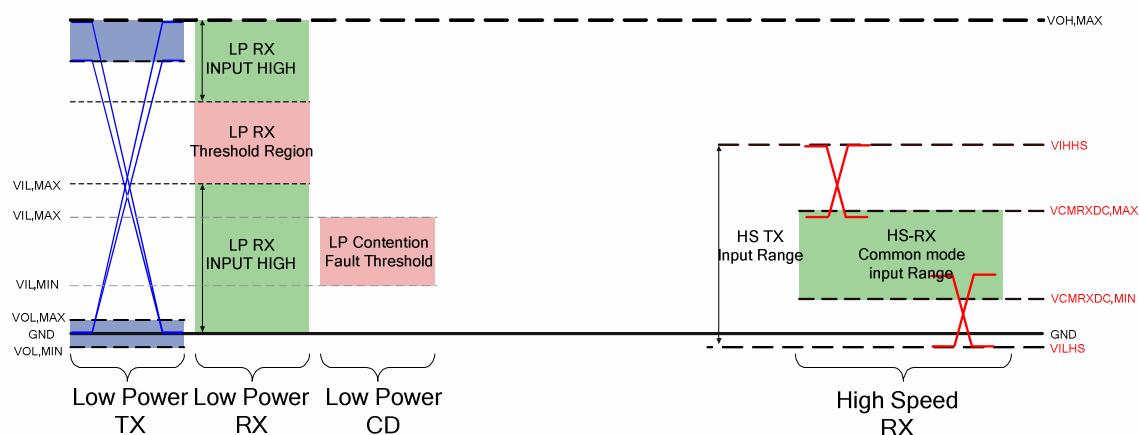
In general, the DSI D-PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 7.5 shows the complete set of electrical functions required for a fully featured PHY transceiver.



**Figure 7.2: Electrical functions of a fully D-PHY transceiver**

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 7.6 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.



**Figure 7.3: Shows both the HS and LP signal levels**

### 7.3.2.2 Electrical characteristics of low-power transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes. It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{OL}$	Thevenin output low level	-50	-	50	mV	-
$V_{OH}$	Thevenin output high level	1.1	1.2	1.3	V	-
$Z_{OLP}$	Output impedance of LP-TX	110	-	-	$\Omega$	(1)

**Note:** (1) Though no maximum value for  $Z_{OLP}$  is specified, the LP transmitter output impedance shall ensure the  $t_{RLP}/t_{FLP}$  specification is met.

**Table 7.4: LP transmitter DC specifications**

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$t_{RLP}/t_{FLP}$	15%-85% rise time and fall time	-	-	25	ns	(1)
$\delta V/\delta t_{SR}$	Slew rate @ $C_{LOAD} = 0\text{pF}$	-	-	500	$\text{mV/ns}$	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 5\text{pF}$	-	-	300	$\text{mV/ns}$	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 20\text{pF}$	-	-	250	$\text{mV/ns}$	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 70\text{pF}$	-	-	150	$\text{mV/ns}$	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 0$ to $70\text{pF}$ (Falling Edge Only)	30	-	-	$\text{mV/ns}$	(1),(2),(3)
	Slew rate @ $C_{LOAD} = 0$ to $70\text{pF}$ (Rising Edge Only)	30	-	-	$\text{mV/ns}$	(1),(3),(7)
	Slew rate @ $C_{LOAD} = 0$ to $70\text{pF}$ (Rising Edge Only)	30 – 0.075 *	(VO,INST - 700)	-	$\text{mV/ns}$	(1),(8),(9)
$C_{LOAD}$	Load capacitance	0	-	70	$\text{pF}$	-

**Note:** (1)  $C_{LOAD}$  includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be  $<10\text{pF}$ . The distributed line capacitance can be up to  $50\text{pF}$  for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN(absmax).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700 mV and 930 mV.

**Table 7.5: LP transmitter AC specifications**

### 7.3.2.3 Electrical characteristics of receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

#### 7.3.2.4 High-speed receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination,  $Z_{ID}$ , between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{IDTH}$	Differential input high threshold	-	-	70	mV	-
$V_{IDL}$	Differential input low threshold	-70	-	-	mV	-
$V_{ILHS}$	Single-ended input low voltage	-40	-	-	mV	(1)
$V_{IHHS}$	Single-ended input high voltage	-	-	460	mV	(1)
$V_{CMRXDC}$	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
$Z_{ID}$	Differential input impedance	80	100	125	$\Omega$	-

**Note:** (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

**Table 7.6: HS receiver DC Specifications**

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	$mV_{PP}$	(1)
$C_{CM}$	Common mode termination	-	-	60	pF	(2)

**Note:** (1)  $\Delta V_{CMRX(HF)}$  is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

**Table 7.7: HS receiver AC Specifications**

### 7.3.2.5 Low-power receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSpike. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 7.7 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

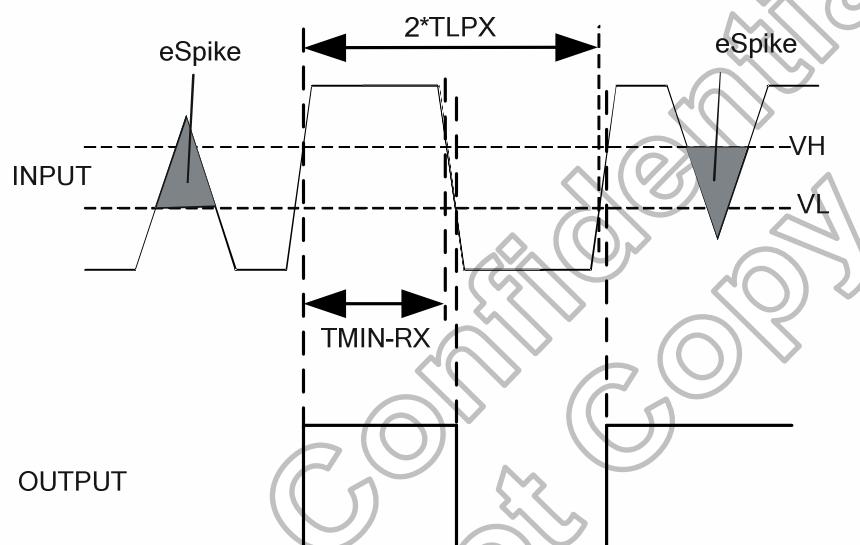


Figure 7.4: Input glitch rejections of low-power receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{IL}$	Logic 0 input threshold	-	-	550	mV	-
$V_{IH}$	Logic 1 input threshold	880	-	-	mV	-

Table 7.8: LP receiver DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
eSPIKE	Input pulse rejection	-	-	300	V.ps	(1), (2), (3)
$T_{MIN-RX}$	Minimum pulse width response	20	-	-	ns	(4)
$V_{INT}$	Peak-to-peak interference voltage	-	-	200	mV	-
$f_{INT}$	Interference frequency	450	-	-	MHz	-

**Note:** (1) Time-voltage integration of a spike above  $V_{IL}$  when being in LP-0 state or below  $V_{IH}$  when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Table 7.9: LP receiver AC specifications

### 7.3.2.6 Line contention detection

Contention can be inferred from any of the following conditions:

- A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than  $V_{IL}$ .
- B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than  $V_{IL}$ .

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{IHCD}$	Logic 1 contention threshold	450	-	-	mV	-
$V_{ILCD}$	Logic 0 contention threshold	-	-	200	mV	-

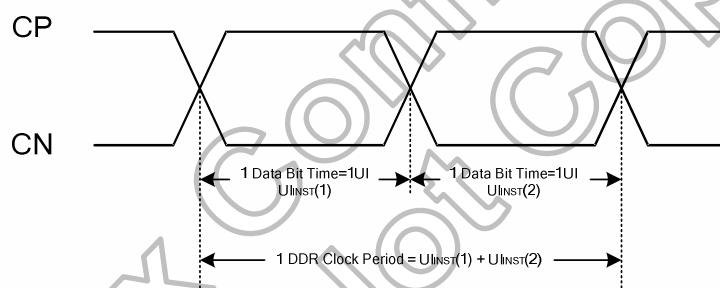
Table 7.10: Contention detector DC specifications

### 7.3.2.7 High-speed data-clock timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CP – CN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 7.8.



**Figure 7.5: DDR clock definition**

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UI<sub>INST</sub> specifications for the Clock signal are summarized in Table 7.11.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI <sub>INST</sub>	-	-	12.5	ns	(1), (2), (3), (4), (5)

**Note:** (1) This value corresponds to a minimum 80 Mbps data rate.

(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

(3) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

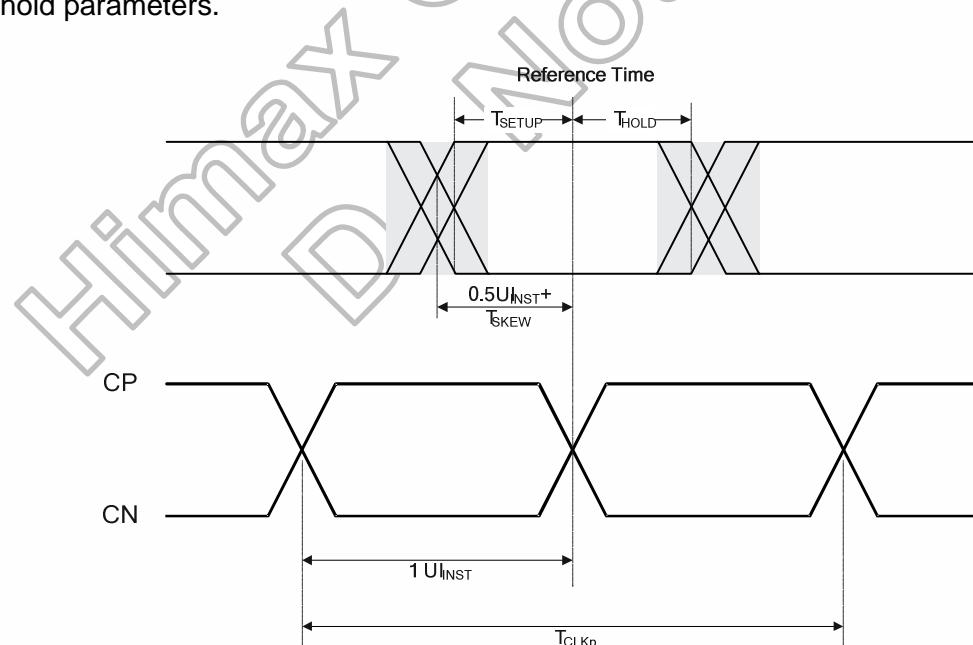
**Table 7.11: Reverse HS data transmission timing parameters**

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 7.9. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.



**Figure 7.6: Data to clock timing definitions**

### 7.3.2.8 Data-clock timing specifications

The Data-Clock timing specifications are shown in Table 7.12. Implementers shall specify a value  $UI_{INST,MIN}$  that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 7.12 are specified as a part of this value. The skew specification,  $T_{SKEW[TX]}$ , is the allowed deviation of the data launch time to the ideal  $\frac{1}{2}UI_{INST}$  displaced quadrature clock edge. The setup and hold times,  $T_{SETUP[RX]}$  and  $T_{HOLD[RX]}$ , respectively, describe the timing relationships between the data and clock signals.  $T_{SETUP[RX]}$  is the minimum time that data shall be present before a rising or falling clock edge and  $T_{HOLD[RX]}$  is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave  $0.4*UI_{INST}$ , i.e.  $\pm 0.2*UI_{INST}$  for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [Receiver]	$T_{SETUP[RX]}$	0.15	-	-	$UI_{INST}$	(1)
Clock to Data Hold Time [Receiver]	$T_{HOLD[RX]}$	0.15	-	-	$UI_{INST}$	(1)

**Note:** (1) Total setup and hold window for receiver of  $0.3*UI_{INST}$ .

**Table 7.12: Data to clock timing specifications**

### 7.3.3 Timings for DSI video mode

#### 7.3.3.1 Vertical timings

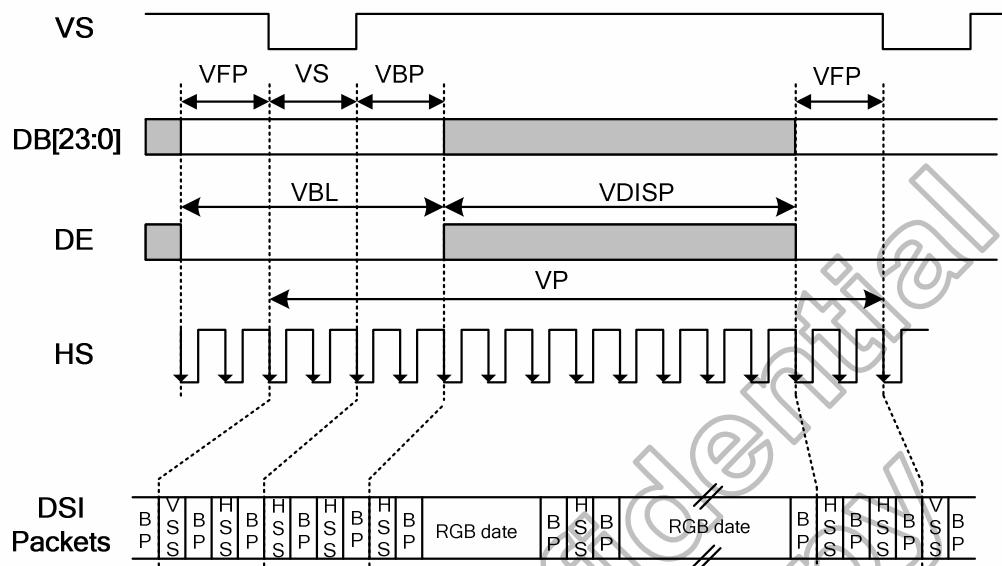


Figure 7.7: Vertical timings for DSI I/F

Resolution=800x1280(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, TA=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	1286	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display.

Table 7.13: Vertical timings for DSI I/F

### 7.3.3.2 Horizontal timings

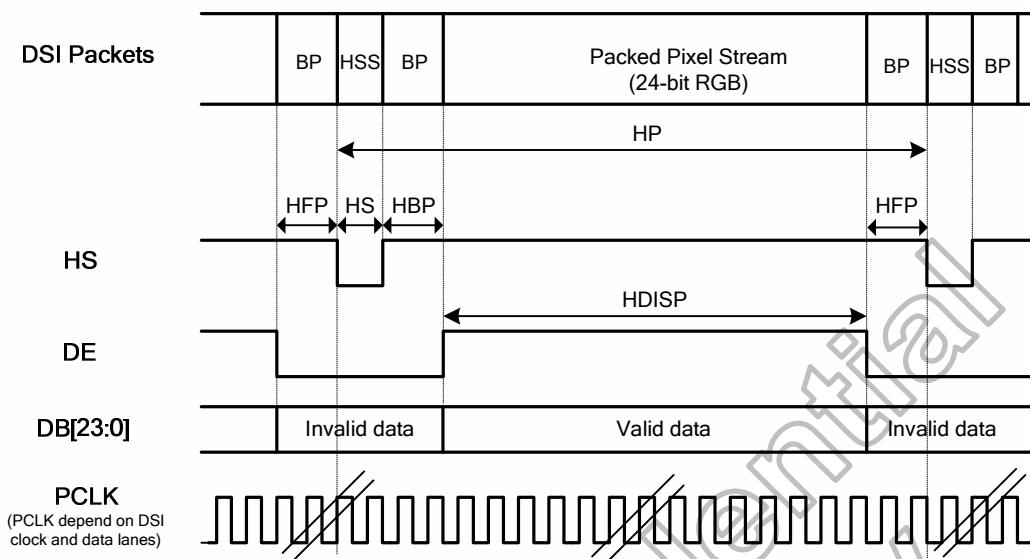


Figure 7.8: Horizontal timing for DSI video mode I/F

Resolution=800x1280 (VSSA=0V, VDD1=1.8V, VDD2=VDD3=VCC=2.8V, TA=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	0.2	-	-	μs
Horizontal back porch	HBP	-	1.0	-	-	μs
Horizontal front porch	HFP	-	1.0	-	-	μs
Horizontal data start point	-	HS+HBP	1.2	-	-	μs
Horizontal blanking period	HBLK	HS+HBP+HFP	2.2	-	-	μs
Horizontal active area	HDISP	-	-	800	-	DCK

Table 7.14: Horizontal timings for DSI video mode I/F

## 8. Ordering Information

Part No.	Package
HX8394-D <u>PDxxx</u>	PD: mean COG xxx: mean chip thickness ( $\mu\text{m}$ ), (default: 250 $\mu\text{m}$ )

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