Department of Electrical and Computer Engineering

The University of Texas at Austin

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Problem Set 4 Solution
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1. The number of occurances of value x, in the input vector V0,V1,...,Vn-1

2. a) Single processor system - using Horner's rule

   $(((((ax + b)x + c)x + d)x + e)x + f)x + g$

   Number of operations = 12 (6 multiplies & 6 adds)

   Number of time-steps = 12

   b) Using 4 processors: time steps = 5, operations = 15.

   One way of doing this is:

Step 1	$x * x$	$b * x$	$d * x$	$f * x$
Step 2	$x^2 * x^2$	$a * x^2$	$dx + e$	$bx + c$
Step 3	$ax^2 * x^4$	$(bx + c) * x^4$	$(dx + e) * x^2$	$fx + g$
Step 4	$ax^6 + bx^5 + cx^4$	$dx^3 + ex^2 + fx + g$		
Step 5	$ax^6 + bx^5 + cx^4 + dx^3 + ex^2 + fx + g$			

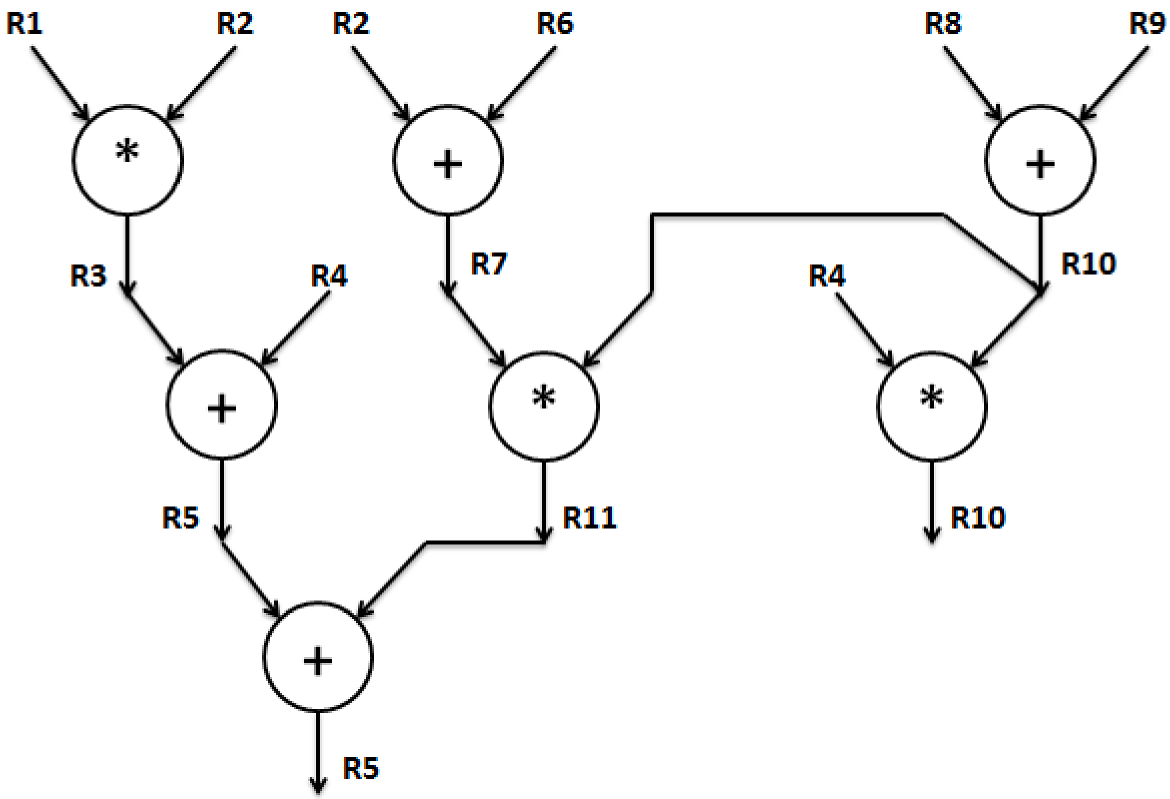
   An intuitive proof for why it can't be done in less than 5 time steps:

   Lets assume it takes x time steps. In the xth time step, only one operation can be performed (either an add or a multiply) to get the final result. In the (x-1)th time step, at the most two operations can be performed, one each to get each of the operands for the operation in step x. In the (x-2)nd time step & other below, possibly 4 units of work can be found. If x = 4, then theres no way to compute all the operands such that only 3 operations are left to be performed after 2 time steps.

   c) Speedup = $T_1 / T_p = 12/5 = 2.4$

3. T1 should be the time to solve the problem, using **the fastest** sequential algorithm and implementation.

4. The Solution:



5. The table is shown below:

		k = 2	k = 4	k = 8	k = 64
Number of switches in each level	n/k	n/2	n/4	n/8	n/64
Number of levels (= latency)	$\log_k n$	$\log_2 n$	$\log_4 n$	$\log_8 n$	$\log_{64} n$
Cost	$k^2 * n/k * \log_k n = nk\log_k n$	$2n\log_2 n$	$4n\log_4 n$	$8n\log_8 n$	$64n\log_{64} n$

Reasonable choice depends on whether lower cost, latency, or contention is desired.

For n=64, Using k=64 yields the lowest latency, and k=2 or k=4 yields the lowest cost. If we would like low latency we would choose k to be 64. If we would like lowest cost, we would choose k to be 2 or 4. If we would like to minimize contention, we would choose k to be 64.

Another approach could be to minimize the cost-latency product, in which case we would choose k=8 for n=64.

6. Initial state of directory for cache line A: 0000
After processor 1 reads A: 1000
After processor 2 writes to A: 0101
After processor 3 reads A: 0110