The data path in our design consists of three main parts. The MuxOut memory, the adder and logic, and the memory b. The MuxOut memory holds the values that are output to the LEDs and visible to the user. Values in this memory are selected by a mux to supply to the adder and logic based upon the counter address. The counter comes from the FSM and changes value every clock A. On the clock B, the readData signal selects the resulting cell value from the logic to supply to the memory B based upon the counter also. The writeData signal latches the value to the memory B. Every cell of MuxOut is cycled through. At the end of all the cells, the dataPath latches the values from memory B to MuxOut which displays on the LEDs. If the FSM is in input mode, the loadData signal is asserted instead. The DataIn bit comes from the switches that specify a starting configuration. The DataIn is only one bit so an external mux needs to accept a counter address to cycle through the switches in a similar way that the MuxOut memory is cycled through.