

Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2025

COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog Assignment 5

August 20, 2025

Instructions: Please make an individual submission of this assignment. You must demonstrate your working design to a TA for evaluation. Submit a single zipped folder named `VerilogAssignment5_<Your_Roll_No>.zip` containing all well-commented source files. Ensure each source file includes a header with your name and roll number.

Design of a 4-bit Parallel-load Linear Feedback Shift Register (LFSR)

About the Design:

The objective is to design a synchronous sequential circuit using four D flip-flops, which when loaded by a non-zero initial vector (called seed), cycles through all the 15 non-zero binary vectors before returning to the initial vector (the seed). Thus this can be used as a modulo-15 counter. The only combinational blocks required are XOR gates. This forms a very useful structure, commonly known as a Linear Feedback Shift Register (LFSR), and has extensive use in digital circuits, communication theory, etc.

Details of the Circuit:

The design is a synchronous sequential circuit using four D flip-flops connected as shown in Figure 1. The flip-flops can be initialized with a seed by using four multiplexers as shown. When the select line of the multiplexer `sel` is made 0, the bits of the seed vector are passed to the D inputs of the flip-flops. For each of the three flip-flops on the right, when `sel = 1`, the output of the DFF to its left is applied to the input. For the left-most DFF, the bit to be shifted in when the `sel = 1`, is computed by XORing the outputs of the two DFFs on the right as shown. The wire names are mentioned in the diagram to help in your design. Also note that DFFs will have an asynchronous reset input `rst`. For the purpose of demonstration on the FPGA board, you need to use a very slow clock (frequency ~ 1 Hz); therefore, the input clock is to be divided as required.

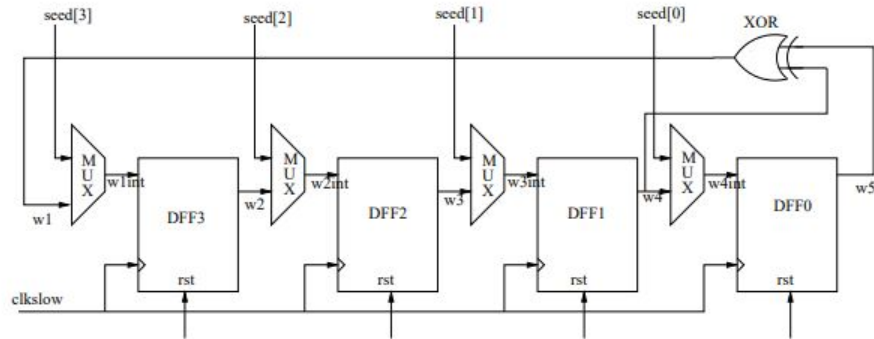


Figure 1: Schematic diagram of the 4-bit LFSR

The Assignment:

For the design of the LFSR and to demonstrate its working, proceed with the following steps.

1. Design the circuit using Verilog in a modular fashion. Your design should have a top-level module which instantiates separate sub-modules for:
 - (a) D flip-flops (DFF)
 - (b) Multiplexers (MUX)
 - (c) Clock-Divider (CLKDiv)

The inputs of the design are: (i) 4-bit `seed`, (ii) `rst`, (iii) `sel`, and (iv) `clk` (generated internally in the board and later divided by your CLKDiv module). The output will be a 4-bit state of the flip-flops, denoted by `state[3:0] = {w2, w3, w4, w5}`.

2. Write an **XDC file** for the design, ensuring that the 4-bit `seed`, `rst`, and `sel` inputs are provided from the switches and buttons on your Nexys4 DDR board. The output `state` must be visualised in the LEDs of your board.
3. Download the design's bit file onto the FPGA board and demonstrate the evolution of the LFSR using the slow clock. Load the LFSR by the non-zero seed **1111**, and verify that it comes back to the same state after 15 clock ticks. The state transitions of the LFSR will be as follows: 1111 → 0111 → 0011 → 0001 → 1000 → 0100 → 0010 → 1001 → 1100 → 0110 → 1011 → 0101 → 1010 → 1101 → 1110 → 1111.