// Assignment 6

// Group 2

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Question 1:

Using BRAM for the S-Box saves a lot of LUT resources, since BRAM is made for storing lookup tables efficiently.

It also improves performance and power compared to implementing the whole S-Box with LUTs. This reduces routing congestion and improves area scaling for larger tables.

The tradeoff is BRAM resource consumption and the need to handle the BRAM's read latency (we insert two wait states in the FSM).

Question 2

The summarised data is as follows

Resources	**Used**	**Available**	**Util in %**		
LUT	**59**	**63400**	**.09**		
FlipFlop	**37**	**126800**	**.03**		
BRAM	**2**	**135**	**1.48**		
IO	**34**	**210**	**16.19**		

For detailed report please refer to "detailed_utilization_report.txt"

Question 3

The critical path is through the S-Box lookup in the datapath, since that's the longest combinational delay before the output is registered.

We Find it from max Delay Path in the TIMING REPORTS

Max Delay Paths

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Slack (MET) : 5.168ns (required time - arrival time)

Source: s_box_inst/sbox_inst_1/U0/inst_blk_mem_gen/gnbram.gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[0].ram.r/prim_init.ram/DEVICE_7SERIES.NO_BMM_INFO.SP.WIDE_PRIM18.ram/CLKARDCLK

(rising edge-triggered cell RAMB18E1 clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: state_reg_reg[7]/D

(rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys_clk_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 4.797ns (logic 2.702ns (56.327%) route 2.095ns (43.672%))

Logic Levels: 2 (LUT6=2)

Clock Path Skew: -0.076ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.945ns = (14.945 - 10.000)

Source Clock Delay (SCD): 5.280ns

Clock Pessimism Removal (CPR): 0.259ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns