Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2025

COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog Assignment 4

August 19, 2025

Instructions: *Please make an individual submission of this assignment. You must demonstrate your working design to a TA for evaluation. Submit a single zipped folder named* `VerilogAssignment4_<Your_Roll_No>.zip` *containing all well-commented source files. Ensure each source file includes a header with your name and roll number.*

Question

Design a 4-bit binary counter that automatically cycles up or down at a visible rate (approximately 2 Hz). The counting direction is controlled by a switch. The entire design must be clocked by the FPGA board's internal high-frequency clock, necessitating the use of a clock divider to slow down the visual output.

[**Note on Persistence of Human eyes:** The FPGA's 100 MHz clock is too fast for the human eye to see changes on the LEDs. This is due to visual persistence: our eyes can only process about 20 images per second before they begin to blur together. Therefore, you must divide the clock to slow the counter's changes to a visible rate. This same principle is fundamental to how digital video systems work.]

I/O Specification

Inputs

- `clk`: The 100 MHz internal clock of the FPGA board.
- `reset`: An asynchronous reset signal. When asserted, it should clear the counter to `4'b0000`.
- `direction`: A single-bit input from a board switch. If the value is `1`, the counter counts up. If it is `0`, the counter counts down.

Outputs

- `count_out[3:0]`: The 4-bit output of the counter. This should be connected to four LEDs for display.
- `mode_led`: A single-bit output connected to a separate LED. This LED should be ON when the counter is in "up" mode (`direction = 1`) and OFF when in "down" mode (`direction = 0`).

Design Requirements

1. **Clock Divider Module:** Design a Verilog module that takes the 100 MHz system clock and generates a slow clock signal with a frequency of approximately 2 Hz.
2. **Structural Adder/Subtractor Module:**
   - You must design a 4-bit adder/subtractor module using a **structural** Verilog description. This means you will first design a full-adder module, and then instantiate it four times to build the 4-bit adder/subtractor.
   - The module should take the 4-bit counter value and the `direction` signal as inputs and output the result of adding or subtracting 1.
   - Draw the architecture for your structural 4-bit adder/subtractor, showing the full-adder instances and any other required logic gates.
3. **Top-Level Counter Module:** Design the main counter module which contains the 4-bit register for the count value.
   - This module must **instantiate** your structural adder/subtractor module to calculate the next count value.
   - The register logic in this module should be clocked by the slow clock signal generated by your clock divider.
4. **FPGA Prototyping and Submission:**
   - **Target Board:** Synthesize and implement your design on the **Digilent Nexys A7-100T (formerly Nexys4 DDR)** FPGA board.
   - **Connections:** Use a board switch for the `direction` input, a push-button for the `reset`, and connect all outputs to the LEDs.
   - **Submission:** Submit all Verilog source files, your architecture diagram for the adder/-subtractor, and a short video of your working prototype.