SONY

Power supply system management & Audio IC

CXD5247GF

Description

The combination of CXD5247and CXD5602 for high performance wearable applications realizes ideal power supply management with low power consumption.

In addition, CXD5247 also realizes audio input/output functions for the CXD5602 System.

Features

Power management block

◆Low power consumption (RTC block IQ=3 μA typ.)

◆Voltage step down type PFM control DC-DC converter (3ch)

◆LDO (5ch)

◆RTC (32.768 kHz clock output)

◆I2C serial interface

◆GPO (8ch)

◆Load switch : 1.8V(4ch)

◆USB charge function

◆Analog front-end for battery power level detection

Audio block

◆Original data format for CXD5602

◆Amplifier for analog microphone + A/D converter

- ◆Number of channels : 4ch
- ◆PGA setting : 0dB to 21dB, 0.5dB increments
- ◆SNR : 90dB(typ.)
- ◆THD+N : -80dB(typ.)
- ◆Input referred noise : 10uVrms

◆S-master BTL Speaker Driver

- ◆Speaker impedance : 8 Ω
- ◆THD+N : 54dB
- ◆Noise level : 10uVrms(typ.)
- ◆POP noise reduction function

◆Other functions

- ◆Supported crystals : 24.576MHz/49.152MHz
- ◆GPO(1ch)

Package

XFBGA 156pin

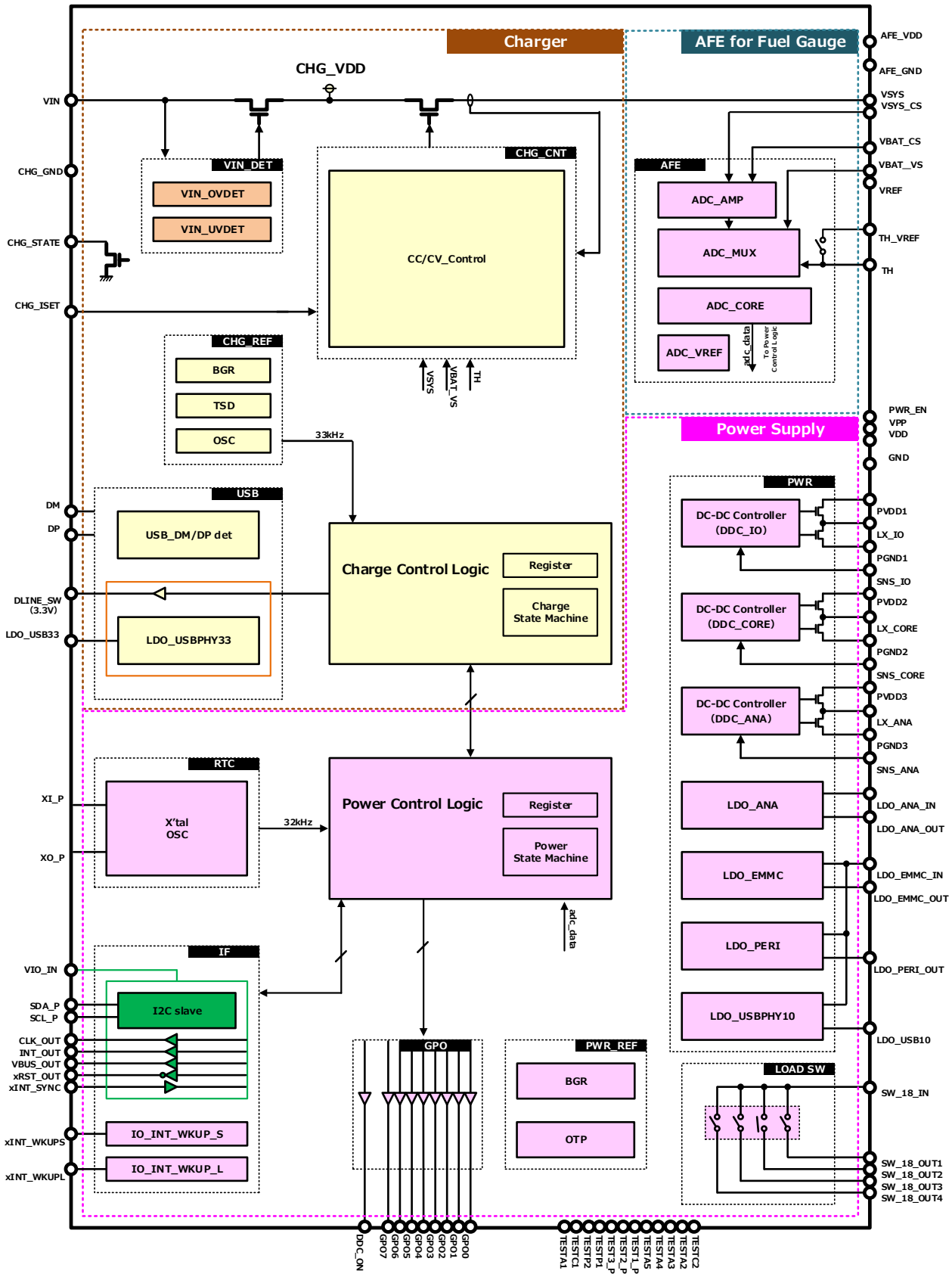
Structure

CMOS Si monolithic IC

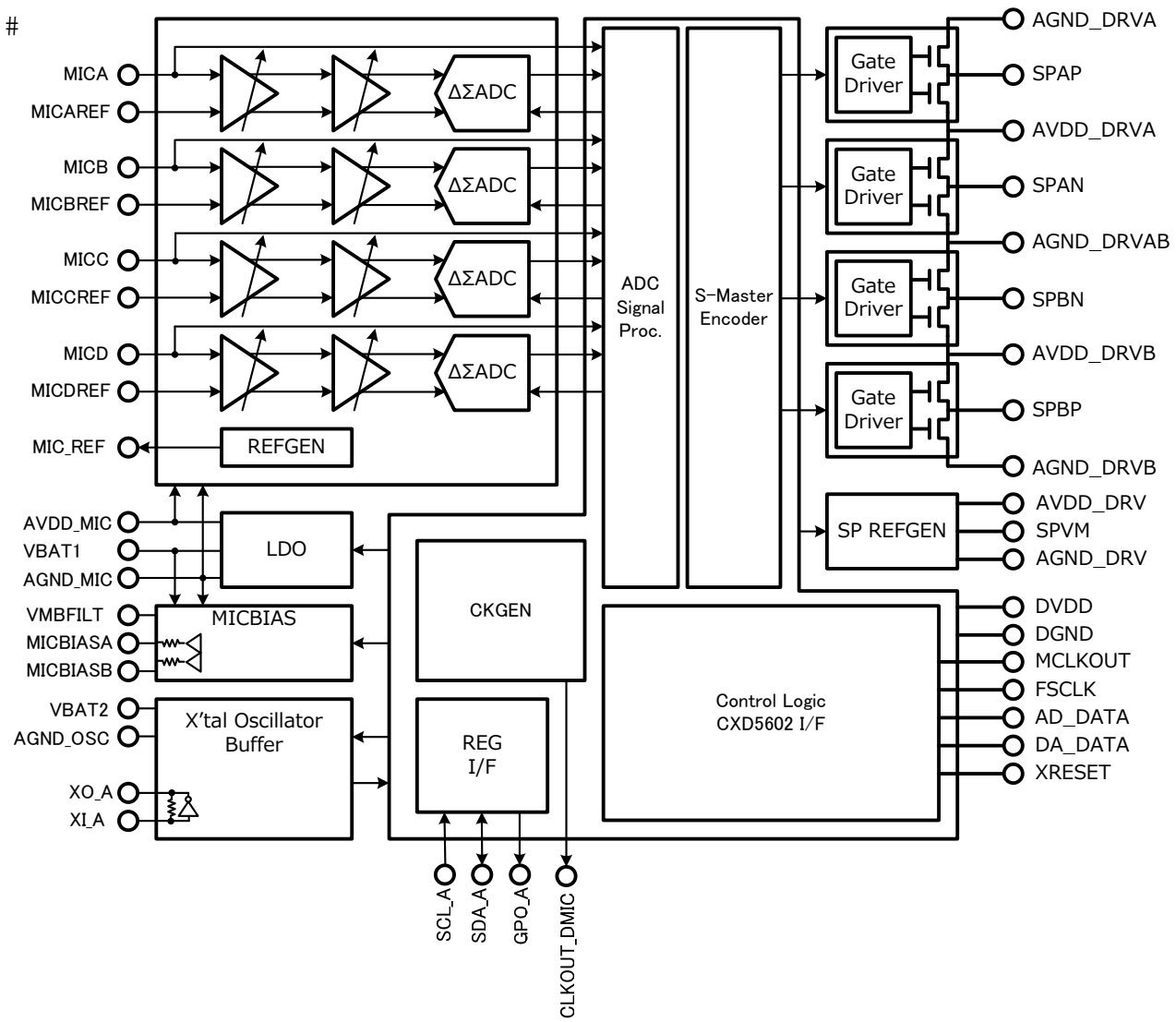
Contents

Block Diagram

◆Power management block

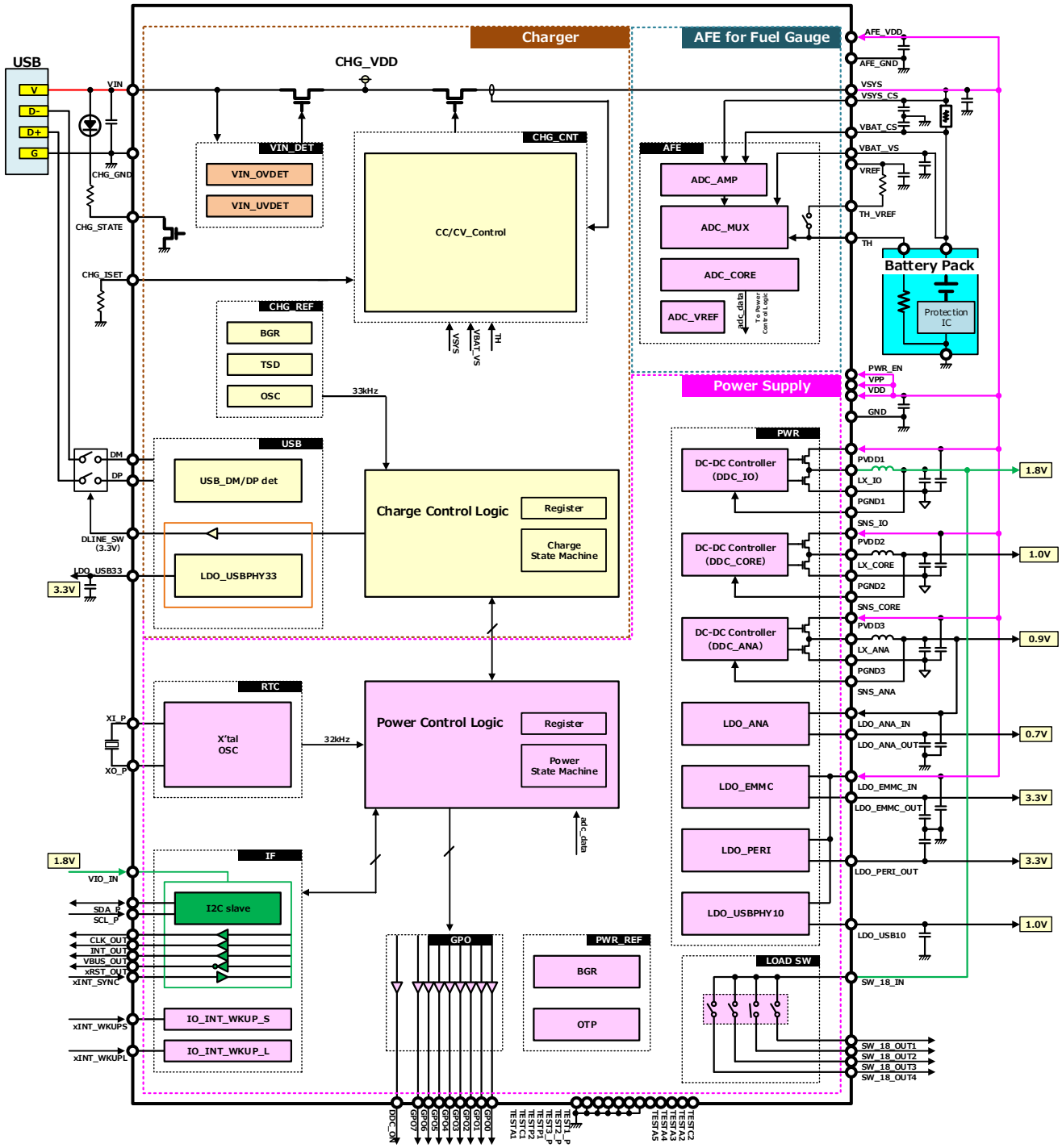


◆Audio Block


#
MICA
MICAREF
MICB
MICBREF
MICC
MICCREF
MICD
MICDREF
MIC_REF
REFGEN
ΔΣADC
ΔΣADC
ΔΣADC
ΔΣADC
ADC Signal Proc.
S-Master Encoder
Gate Driver
Gate Driver
Gate Driver
Gate Driver
AGND_DRVA
SPAP
AVDD_DRVA
SPAN
AGND_DRVAB
SPBN
AVDD_DRVB
SPBP
AGND_DRVB
SP REFGEN
AVDD_DRV
SPVM
AGND_DRV
AVDD_MIC
VBAT1
AGND_MIC
LDO
VMBFILT
MICBIASA
MICBIASB
MICBIAS
CKGEN
VBAT2
AGND_OSC
X'tal Oscillator Buffer
XO_A
XI_A
REG I/F
Control Logic CXD5602 I/F
DVDD
DGND
MCLKOUT
FSCLK
AD_DATA
DA_DATA
XRESET
SCL_A
SDA_A
GPO_A
CLKOUT_DMIC

Application Circuit

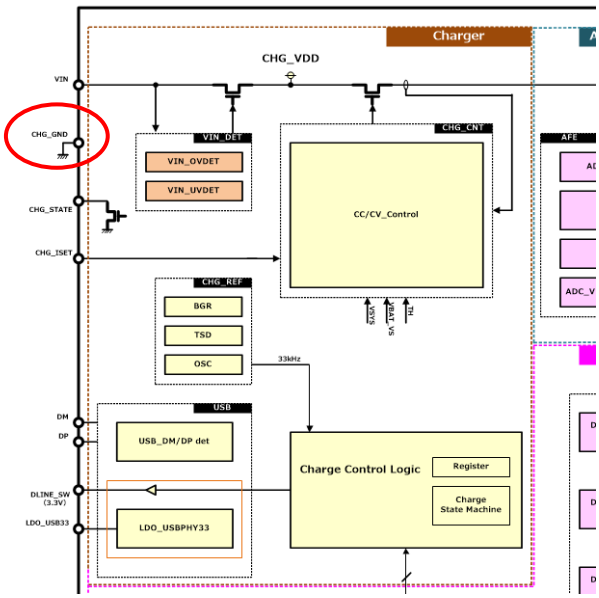
◆Power management block



Power management block (Case : Nonuse of charge function)

Open-pin : VIN, CHG_STATE, CHG_ISET, DP, DM, DLINE_SW, LDO_USB33

Connect-pin: CHG_GND to GND

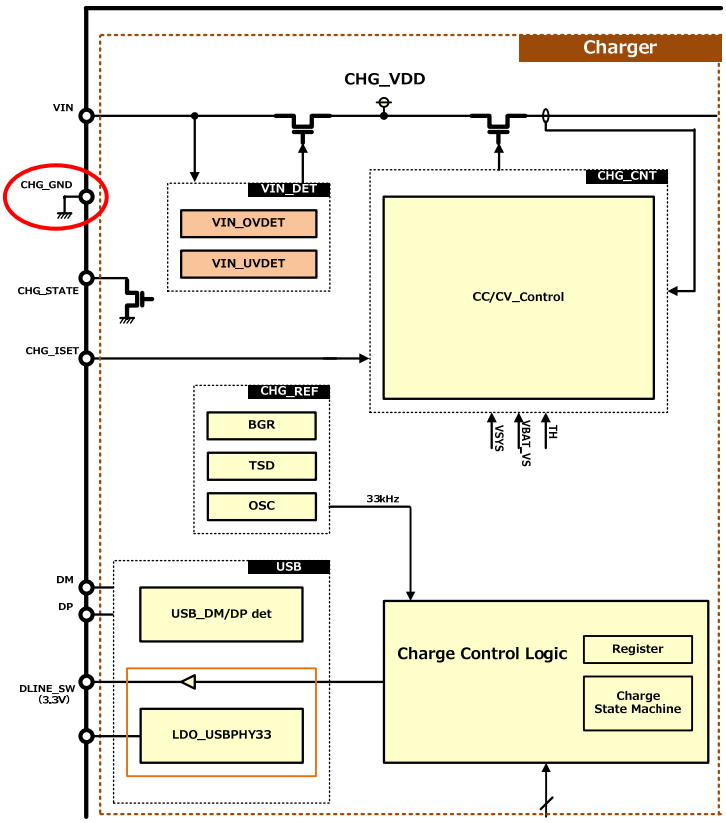


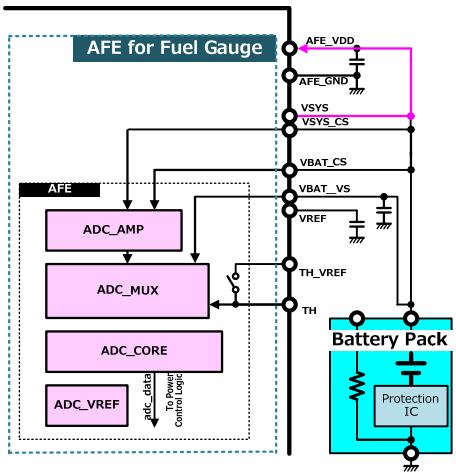
Power management block (Case : Nonuse of charge function and fuel gauge function)

Open-pin : VIN, CHG_STATE, CHG_ISET, DP, DM, DLINE_SW, LDO_USB33,TH_VREF, TH

Connect-pin: VSYS, VSYS_CS, VBAT_CS, VBAT_VS, AFE_VDD (VDD), CHG_GND to GND

External-part: VREF - 0.22uF, VBAT_VS - 1uF

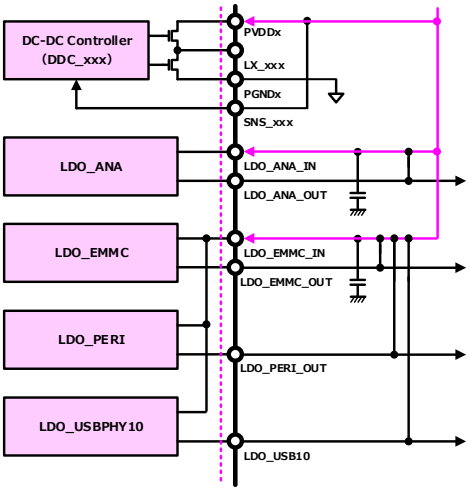




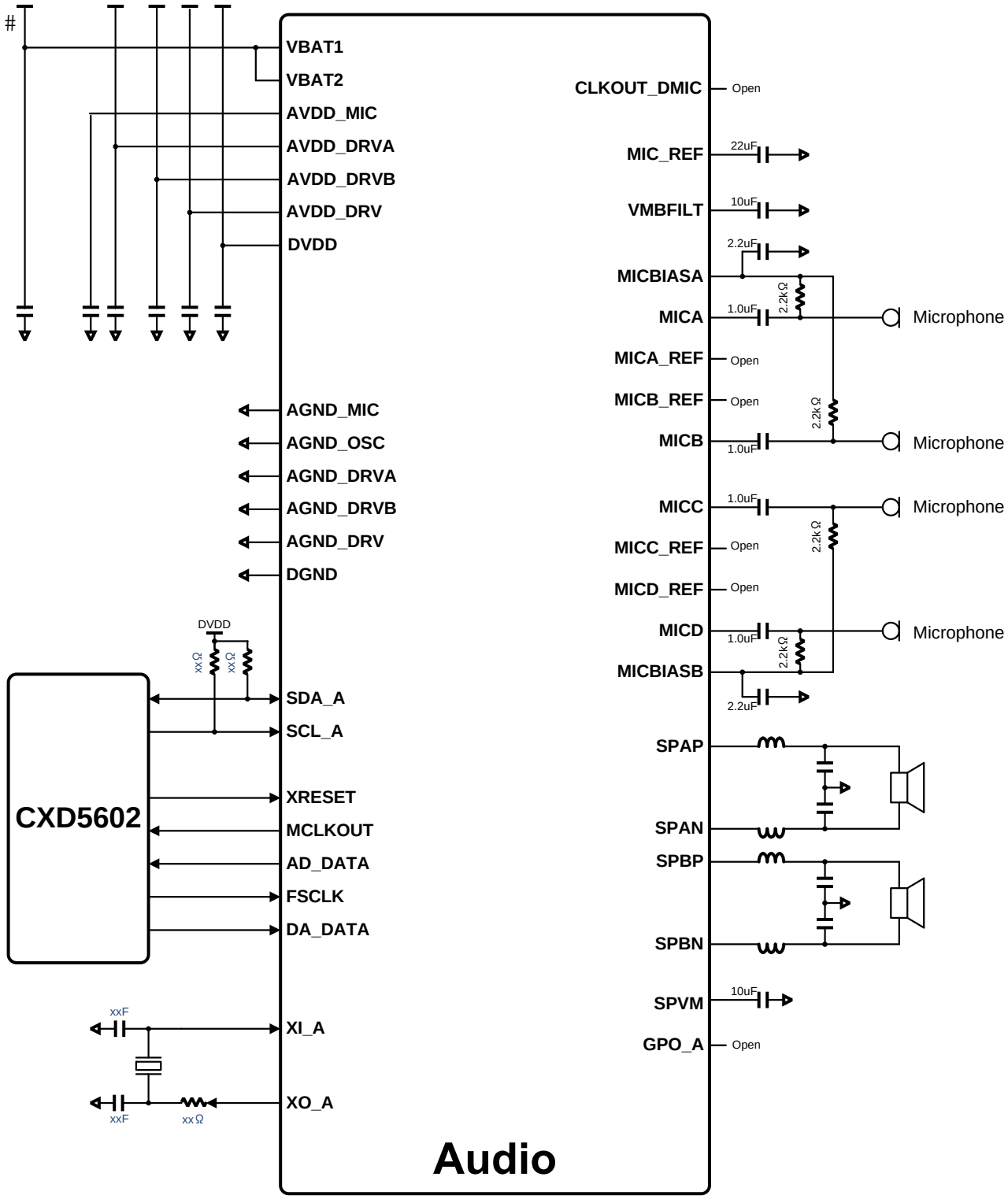
Power management block (Case : Nonuse of power supply)

Open-pin : LX_xxx

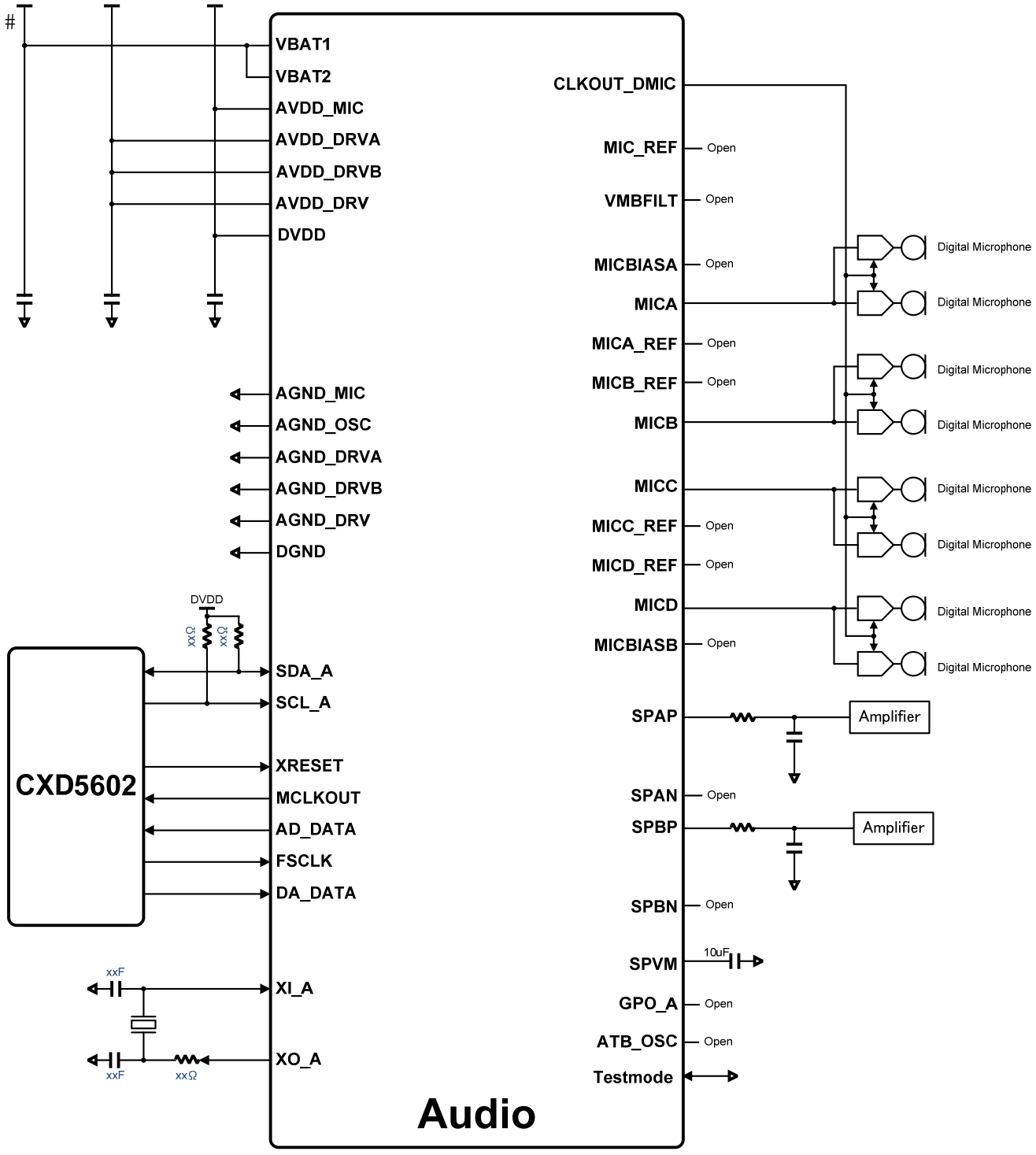
Connect-pin : SNS_xxx to PVDD (VDD), LDO_EMMC_OUT(or PERI_OUT or USB10) to LDO_EMMC_IN



◆**Audio block (Case1：Speaker BTL Drive / 4ch Analog MIC)**



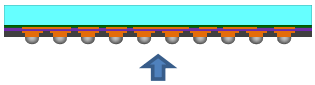
◆Audio block (Cace2：External Speaker Amp / 8ch Digtal MIC)



Pin Configuration

	A	B	C	D	E	F	G	H	J	K	L	M
1	VIN2	VIN4	VSYS2	VSYS4	VREF	AFE_GND	LDO_EMMC_OUT	LDO_EMMC_IN	LDO_PERI_OUT	LDO_USB10	GND1	XI_P
2	VIN1	VIN3	VSYS1	VSYS3	TH_VREF	AFE_VDD	N.C.	N.C.	GND	GND	GND	XO_P
3	DP	CHG_GND1	CHG_GND2	VBAT_VS	TH	N.C.	N.C.	GND	GPO7	GPO6	GPO5	GPO4
4	LDO_USB33	CHG_ISET	DM	CHG_STATE	VBAT_CS	VSYS_CS	N.C.	N.C.	GPO3	GPO2	GPO1	VDD1
5	PVDD2	PVDD2_S	DLINE_SW	GND	N.C.	N.C.	N.C.	N.C.	GPO0	N.C.	GND	LDO_ANA_IN
6	LX_CORE	N.C.	SNS_CORE	N.C.	N.C.	N.C.	GND2	N.C.	xRST_OUT	SNS_ANA	VPP	LDO_ANA_OUT
7	PGND2	PGND2_S	GND3	DDC_ON	GND	DA_DATA	N.C.	N.C.	SDA_P	xINT_SYNC	PGND3_S	PGND3
8	PVDD1	PVDD1_S	PWR_EN	xINT_WKUPL	MCLK_OUT	SW_18_OUT2	SW_18_OUT3	N.C.	SCL_P	CLK_OUT	N.C.	LX_ANA
9	LX_IO	N.C.	VDD2	xINT_WKUPS	SW_18_OUT1	SW_18_IN1	SW_18_IN2	SW_18_OUT4	GND4	VBUS_OUT	PVDD3_S	PVDD3
10	PGND1	PGND1_S	SNS_IO	SDA_A	GPO_A	CLKOUT_DMIC	MIC_REF	AGND_MIC	MICDREF	INT_OUT	VIO_IN	GND5
11	XRESET	FSCLK	AD_DATA	SCL_A	GND	MICA	MICB	AVDD_MIC	MICD	MIC_BIASB	VMBFILT	SPVM
12	XI_A	AGND_OSC	N.C.	DVDD	DGND	MICAREF	MICBREF	MICC	MICCREF	MIC_BIASA	VBAT1	AVDD_DRV
13	XO_A	VBAT2	AGND_DRVA	SPAP	AVDD_DRVA	SPAN	AGND_DRVAB	SPBN	AVDD_DRVB	SPBP	AGND_DRVB	AGND_DRV

Audio Power



BOTTOM VIEW

Pin Table

No.	Ball #	Ball Name	Power Supply	Type	Description
1	A1	VIN2 (=VIN1)	CHG_GND	Power Supply	Power Supply for USB
2	A2	VIN1	CHG_GND	Power Supply	Power Supply for USB
3	A3	DP	VIN,CHG_GND	Analog	USB bus, D + input
4	A4	LDO_USB33	VIN,CHG_GND	Analog	USB Power Supply LDO 3.3V output
5	A5	PVDD2	PGND2	Power Supply	Power Supply for DDC_core
6	A6	LX_CORE	—	Analog	Switching output for DDC_core
7	A7	PGND2	—	Power Supply	Ground for DDC_core
8	A8	PVDD1	PGND1	Power Supply	Power Supply for DDC_IO
9	A9	LX_IO	—	Analog	Switching output for DDC_IO
10	A10	PGND1	—	Power Supply	Ground for DDC_IO
11	A11	XRESET	DVDD,DGND	Digital INPUT	System Reset
12	A12	XI_A	VBAT2,AGND_OSC	Analog	Crystal Oscillator Input
13	A13	XO_A	VBAT2,AGND_OSC	Analog	Crystal Oscillator Output
14	B1	VIN4 (=VIN1)	CHG_GND	Power Supply	Power Supply for USB
15	B2	VIN3 (=VIN1)	CHG_GND	Power Supply	Power Supply for USB
16	B3	CHG_GND1	—	Power Supply	Ground for Chager
17	B4	CHG_ISET	VIN,CHG_GND	Analog	Charge current setting input
18	B5	PVDD2_S (=PVDD2)	PGND2	Power Supply	Power Supply for DDC_core
19	B6	N.C.	—	—	—
20	B7	PGND2_S (=PGND2)	—	Power Supply	Ground for DDC_core
21	B8	PVDD1_S (=PVDD1)	PGND1	Power Supply	Power Supply for DDC_IO
22	B9	N.C.	—	—	—
23	B10	PGND1_S (=PGND1)	—	Power Supply	Ground for DDC_IO
24	B11	FSCLK	DVDD,DGND	Digital INPUT	Serial Data Frame Clock
25	B12	AGND_OSC	—	Power Supply	Ground for Oscillator
26	B13	VBAT2	AGND_OSC	Power Supply	Power Supply from Battery
27	C1	VSYS2 (=VSYS1)	CHG_GND	Power Supply	Power Supply for SYTEM
28	C2	VSYS1	CHG_GND	Power Supply	Power Supply for SYTEM
29	C3	CHG_GND2 (=CHG_GND1)	—	Power Supply	Ground for Chager
30	C4	DM	VIN,CHG_GND	Analog	USB bus, D - input
31	C5	DLINE_SW	VIN,CHG_GND	Digital OUTPUT	USB bus connection signal
32	C6	SNS_CORE	VDD,GND	Analog	Feedback input for DDC_CORE

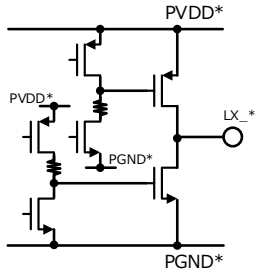
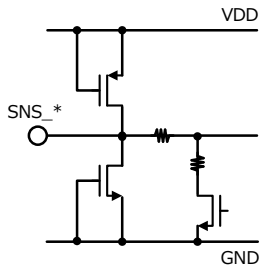
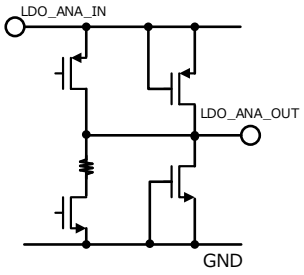
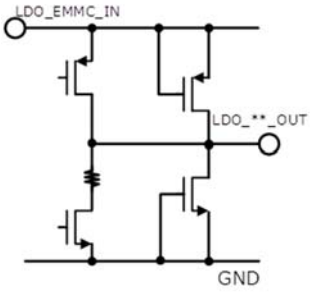
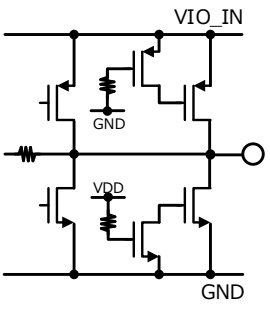
No.	Ball #	Ball Name	Power Supply	Type	Description
33	C7	GND3 (=GND)	—	Power Supply	Ground for PM
34	C8	PWR_EN	VDD,GND	Digital INPUT	Enable input
35	C9	VDD2 (=VDD)	GND	Power Supply	Power Supply for PM
36	C10	SNS_IO	VDD,GND	Analog	Feedback input for DDC_IO
37	C11	AD_DATA	DVDD,DGND	Digital OUTPUT	ADC Serial Data Output
38	C12	N.C.	—	—	Test output (ATB_OSC)
39	C13	AGND_DRVA	—	Power Supply	Ground for Ach Speaker Driver
40	D1	VSYS4 (=VSYS1)	CHG_GND	Power Supply	Power Supply for SYTEM
41	D2	VSYS3 (=VSYS1)	CHG_GND	Power Supply	Power Supply for SYTEM
42	D3	VBAT_VS	CHG_GND	Analog	Battery voltage sense input
43	D4	CHG_STATE	VIN,CHG_GND	Digital OUTPUT	Charge status output
44	D5	GND	—	—	Test input (TESTC1)
45	D6	N.C.	—	—	—
46	D7	DDC_ON	VDD,GND	Digital OUTPUT	DDC_CORE start-up output
47	D8	xINT_WKUPL	VDD,GND	Digital INPUT	Long time interrupt input
48	D9	xINT_WKUPS	VDD,GND	Digital INPUT	Short time interrupt input
49	D10	SDA_A	DVDD,DGND	Digital OUTPUT	I2C Serial Control Data
50	D11	SCL_A	DVDD,DGND	Digital INPUT	I2C Serial Control Port Clock
51	D12	DVDD	DVDD,DGND	Power Supply	Power Supply for 1.8V Digital Domain
52	D13	SPAP	AVDD_DRVA,AGND_DRVA	Analog	Positive Speaker Output of Ach
53	E1	VREF	AFE_VDD,AFE_GND	Analog	VREF output
54	E2	TH_VREF	AFE_VDD,AFE_GND	Analog	Thermistor monitor input
55	E3	TH	AFE_VDD,AFE_GND	Analog	Thermistor input
56	E4	VBAT_CS	CHG_GND	Analog	Battery current sense input
57	E5	N.C.	—	—	Test output (TESTC2)
58	E6	N.C.	—	—	—
59	E7	GND	—	—	Test input (TESTP1)
60	E8	MCLKOUT	DVDD,DGND	Digital OUTPUT	Master Clock Output
61	E9	SW_18_OUT1	SW_18_IN,GND	Analog	Load switch output (for USB)
62	E10	GPO_A	DVDD,DGND	Digital OUTPUT	General Purpose Output
63	E11	GND	—	—	Test input (TESTMODE)
64	E12	DGND (=GND)	—	Power Supply	Ground for 1.8V Digital Domain
65	E13	AVDD_DRVA	AGND_DRVA	Power Supply	Power Supply for Ach Speaker Driver
66	F1	AFE_GND	—	Power Supply	Ground for AFE
67	F2	AFE_VDD	AFE_GND	Power Supply	Power Supply for AFE
68	F3	N.C.	—	—	Test output (TESTA5)

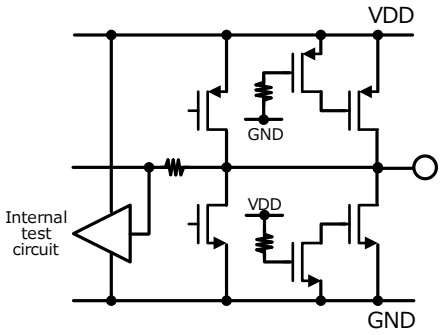
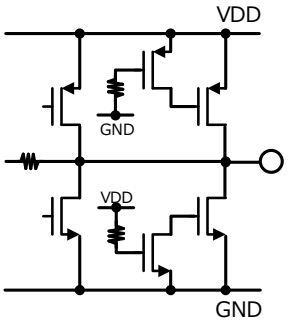
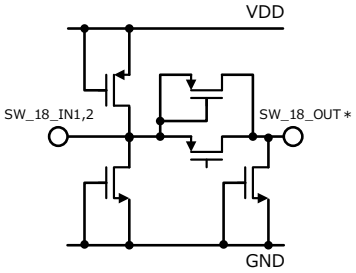
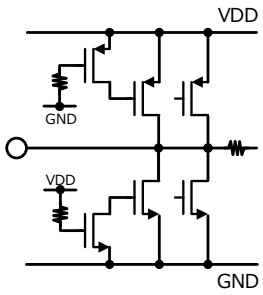
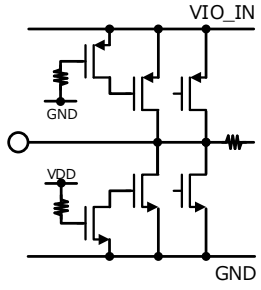
No.	Ball #	Ball Name	Power Supply	Type	Description
69	F4	VSYS_CS	VSYS,CHG_GND	Analog	VSYS current sense input
70	F5	N.C.	—	—	—
71	F6	N.C.	—	—	—
72	F7	DA_DATA	DVDD,DGND	Digital INPUT	DAC Serial Data Input
73	F8	SW_18_OUT2	SW_18_IN,GND	Analog	Load switch output
74	F9	SW_18_IN1	VDD,GND	Analog	Load switch input
75	F10	CLKOUT_DMIC	DVDD,DGND	Digital OUTPUT	Clock Output for Digital Microphone
76	F11	MICA	AVDD_MIC,AGND_MIC	Analog	Microphone Input
77	F12	MICAREF	AVDD_MIC,AGND_MIC	Analog	Reference terminal for Microphone Input
78	F13	SPAN	AVDD_DRVA,AGND_DRVA	Analog	Negative Speaker Output of Ach
79	G1	LDO_EMMC_OUT	LDO_EMMC_IN,GND	Analog	Power supply LDO output for EMMC
80	G2	N.C.	—	—	Test output (TESTA2)
81	G3	N.C.	—	—	Test output (TESTA4)
82	G4	N.C.	—	—	—
83	G5	N.C.	—	—	—
84	G6	GND2 (=GND)	—	Power Supply	Ground for PM
85	G7	N.C.	—	—	—
86	G8	SW_18_OUT3	SW_18_IN,GND	Analog	Load switch output
87	G9	SW_18_IN2 (=SW_18_IN1)	VDD,GND	Analog	Load switch input
88	G10	MIC_REF	AVDD_MIC,AGND_MIC	Analog	Common Reference for MIC ADC
89	G11	MICB	AVDD_MIC,AGND_MIC	Analog	Microphone Input
90	G12	MICBREF	AVDD_MIC,AGND_MIC	Analog	Reference terminal for Microphone Input
91	G13	AGND_DRVAB	—	Power Supply	Ground for Ach/Bch Speaker Driver
92	H1	LDO_EMMC_IN	GND	Analog	Power supply LDO input for EMMC
93	H2	N.C.	—	—	Test output (TESTA3)
94	H3	GND	—	—	Test input (TESTA1)
95	H4	N.C.	—	—	—
96	H5	N.C.	—	—	—
97	H6	N.C.	—	—	—
98	H7	N.C.	—	—	—
99	H8	N.C.	—	—	—
100	H9	SW_18_OUT4	SW_18_IN,GND	Analog	Load switch output
101	H10	AGND_MIC	—	Power Supply	Ground for MIC Input and MIC bias
102	H11	AVDD_MIC	AGND_MIC	Power Supply	Power Supply for Microphone Input
103	H12	MICC	AVDD_MIC,AGND_MIC	Analog	Microphone Input
104	H13	SPBN	AVDD_DRVB,AGND_DRVB	Analog	Negative Speaker Output of Bch

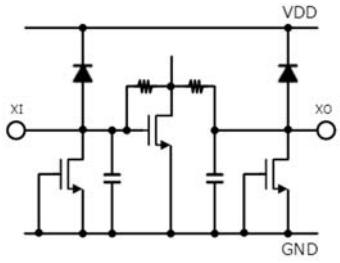
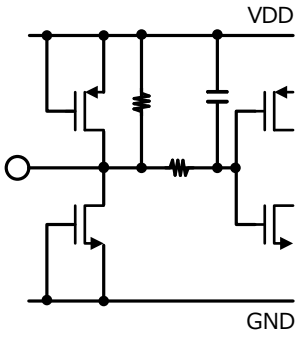
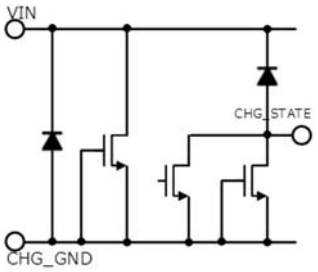
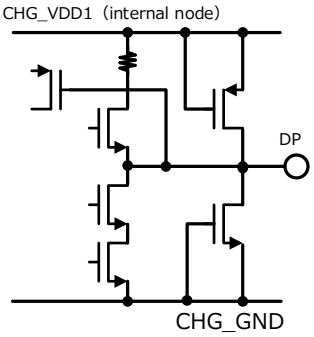
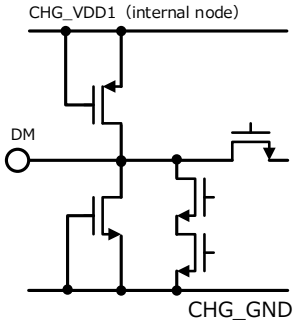
No.	Ball #	Ball Name	Power Supply	Type	Description
105	J1	LDO_PERI_OUT	LDO_EMMC_IN,GND	Analog	Power supply LDO output for peripheral equipment
106	J2	GND	—	—	Test input (TEST1_P)
107	J3	GPO7	VDD,GND	Digital OUTPUT	General-purpose output
108	J4	GPO3	VDD,GND	Digital OUTPUT	General-purpose output
109	J5	GPO0	VDD,GND	Digital OUTPUT	General-purpose output
110	J6	xRST_OUT	VIO_IN,GND	Digital OUTPUT	Reset output
111	J7	SDA_P	VIO_IN,GND	Digital INPUT	Serial data input
112	J8	SCL_P	VIO_IN,GND	Digital INPUT	Serial clock input
113	J9	GND4 (=GND)	—	Power Supply	Ground for PM
114	J10	MICDREF	AVDD_MIC,AGND_MIC	Analog	Reference terminal for Microphone Input
115	J11	MICD	AVDD_MIC,AGND_MIC	Analog	Microphone Input
116	J12	MICCREF	AVDD_MIC,AGND_MIC	Analog	Reference terminal for Microphone Input
117	J13	AVDD_DRVB	AGND_DRVB	Power Supply	Power Supply for Bch Speaker Driver
118	K1	LDO_USB10	LDO_EMMC_IN,GND	Analog	Power supply LDO output for USB
119	K2	GND	—	—	Test input (TEST2_P)
120	K3	GPO6	VDD,GND	Digital OUTPUT	General-purpose output
121	K4	GPO2	VDD,GND	Digital OUTPUT	General-purpose output
122	K5	N.C.	—	—	—
123	K6	SNS_ANA	VDD,GND	Analog	Feedback input for DDC_ANA
124	K7	xINT_SYNC	VIO_IN,GND	Digital INPUT	Interrupt input for time synchronization
125	K8	CLK_OUT	VIO_IN,GND	Digital OUTPUT	Clock output
126	K9	VBUS_OUT	VIO_IN,GND	Digital OUTPUT	USB connection detection output
127	K10	INT_OUT	VIO_IN,GND	Digital OUTPUT	Interrupt output
128	K11	MICBIASB	VBAT1,AGND_MIC	Analog	Microphone Bias
129	K12	MICBIASA	VBAT1,AGND_MIC	Analog	Microphone Bias
130	K13	SPBP	AVDD_DRVB,AGND_DRVB	Analog	Positive Speaker Output of Bch
131	L1	GND1 (=GND)	—	Power Supply	Ground for PM
132	L2	GND	—	—	Test input (TEST3_P)
133	L3	GPO5	VDD,GND	Digital OUTPUT	General-purpose output
134	L4	GPO1	VDD,GND	Digital OUTPUT	General-purpose output
135	L5	GND	—	—	Test input (TESTP2)
136	L6	VPP	GND	Analog	Power supply for OTP write
137	L7	PGND3_S (=PGND3)	—	Power Supply	Ground for DDC_ANA
138	L8	N.C.	—	—	—
139	L9	PVDD3_S (=PVDD3)	PGND1	Power Supply	Power Supply for DDC_ANA

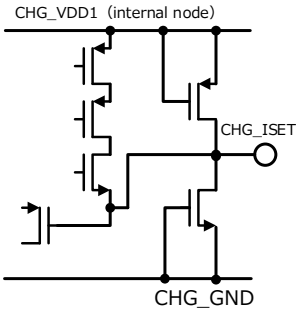
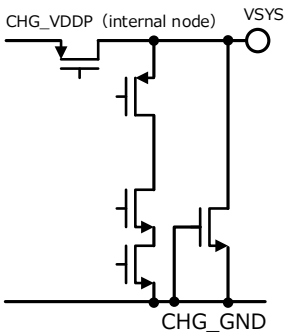
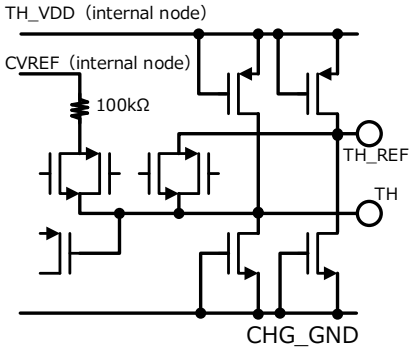
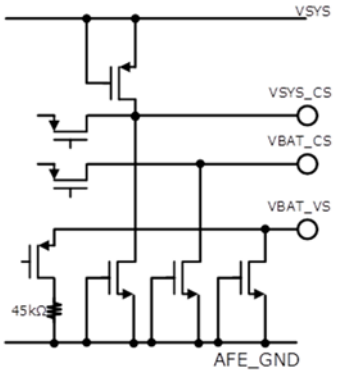
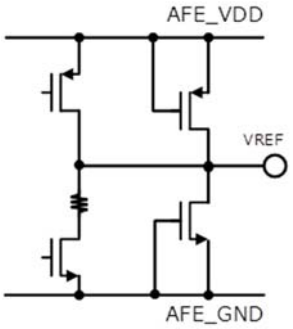
No.	Ball #	Ball Name	Power Supply	Type	Description
140	L10	VIO_IN	GND	Power Supply	Power Supply for IO
141	L11	VMBFILT	VBAT1,AGND_MIC	Analog	Bias voltage of Microphone Bias
142	L12	VBAT1	VBAT1,AGND_MIC	Power Supply	Power Supply from Battery
143	L13	AGND_DRVB	—	Power Supply	Ground for Bch Speaker Driver
144	M1	XI_P	VDD,GND	Analog	Crystal input
145	M2	XO_P	VDD,GND	Analog	Crystal output
146	M3	GPO4	VDD,GND	Digital OUTPUT	General-purpose output
147	M4	VDD1 (=VDD)	GND	Power Supply	Power Supply for PM
148	M5	LDO_ANA_IN	GND	Analog	Power supply LDO input for Analog Core
149	M6	LDO_ANA_OUT	LDO_ANA_IN,GND	Analog	Power supply LDO output for Analog Core
150	M7	PGND3	—	Power Supply	Ground for DDC_ANA
151	M8	LX_ANA	—	Analog	Switching output for DDC_ANA
152	M9	PVDD3	PGND1	Power Supply	Power Supply for DDC_ANA
153	M10	GND5 (=GND)	—	Power Supply	Ground for Digital
154	M11	SPVM	AVDD_DRV,AGND_DRV	Analog	Reference for Speaker Driver
155	M12	AVDD_DRV	AGND_DRV	Power Supply	Power Supply for Driver Analog circuits
156	M13	AGND_DRV	—	Power Supply	Ground for Driver Analog circuits

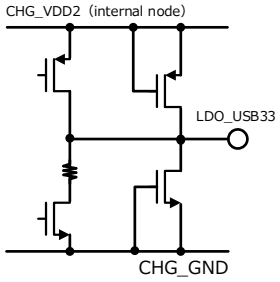
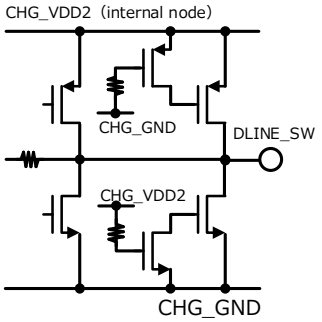
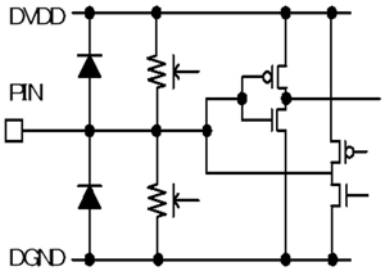
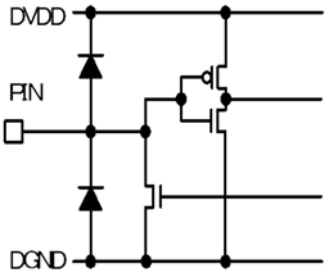
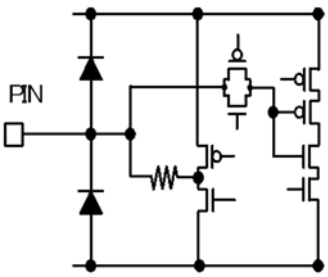
Pin Description

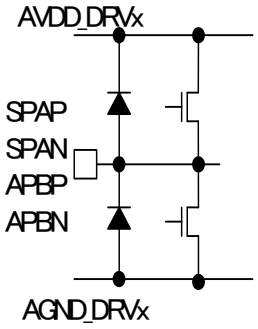
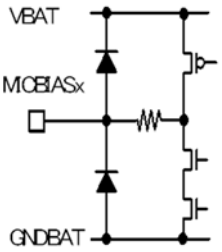
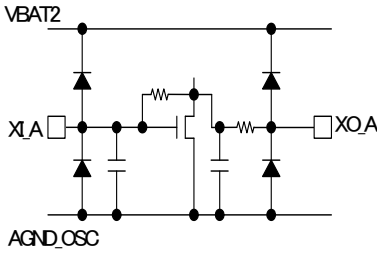
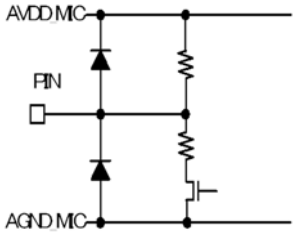
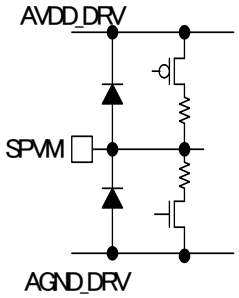
Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
A9,B9 A6,B6 M8,L8	LX_IO LX_CORE LX_ANA	O	PVDD1～PGND1 PVDD2～PGND2 PVDD3～PGND3	
C10 C6 K6	SNS_IO SNS_CORE SNS_ANA	I	1.8V 1.0V 0.9V	
M5 M6	LDO_ANA_IN LDO_ANA_OUT	I O	VDD～GND 3.3V	
H1 G1 J1 K1	LDO_EMMC_IN LDO_EMMC_OUT LDO_PERI_OUT LDO_USB10	I O O O	VDD～GND 3.3V 3.3V 1.0V	
K10 K8 J6 K9	INT_OUT CLK_OUT xRST_OUT VBUS_OUT	O	GND/VIO_IN	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
J5 L4 K4 J4 M3 L3 K3 J3	GPO0 GPO1 GPO2 GPO3 GPO4 GPO5 GPO6 GPO7	O	GND/VDD	 Caution Be sure to pull up or pull down the GPO pin.
D7	DDC_ON	O	GND/VDD	
F9 G9 E9 F8 G8 H9	SW_18_IN1 SW_18_IN2 SW_18_OUT1 SW_18_OUT2 SW_18_OUT3 SW_18_OUT4	I I O O O O	1.8V～GND 1.8V～GND SW_18_IN1,2 SW_18_IN1,2 SW_18_IN1,2 SW_18_IN1,2	
C8	PWR_EN	I	VDD～GND	
J7 J8 K7	SDA_P SCL_P xINT_SYNC	I/O I I	VIO_IN～GND VIO_IN～GND VIO_IN～GND	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
M1 M2	XI_P XO_P	I O	VDD～GND VDD～GND	
D9 D8	xINT_WKUPS xINT_WKUPL	I I	VDD～GND VDD～GND	
D4	CHG_STATE	O	VIN～CHG_GND	
A3	DP	O	0.6V	
C4	DM	I	0～0.6V	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
B4	CHG_ISET	O	0～1.3V	
C1 C2 C3 C4	VSYS	O	0～4.2V	
E2 E3	TH_REF TH	I I	0.6V 0.6V	
F4 E4 D3	VSYS_CS VBAT_CS VBAT_VS	I I I	0～4.2V 0～4.2V 0～4.2V	
E1	VREF	O	2.0V	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
A4	LDO_USB33	O	3.3V	
C5	DLINE_SW	O	0V/ 3.3V	
F10 C11 F7 B11 E8 A11 E10	CLKOUT_DMC, AD_DATA, DA_DATA, FSCLK, MCLKOUT, XRESET, GPO_A	O O I I O I O	0V/1.8V	
D10 D11	SDA_A SCL_A	I/O I	0V/1.8V	
F11 G11 H12 J11	MICA MICB MICC MICD	I	0.9V±0.225V	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
D13 F13 K13 H13	SPAP SPAN SPBP SPBN	O	0V/3.3V	
K12 K11 L11	MICBIASA MICBIASB VMBFILT	O	2V	
A12 A13	XI_A XO_A	I O	0V/1.8V	
F12 G12 J12 J10 G10	MICAREF MICBREF MICCREF MICDREF MIC_REF	OI	0.9V	
M11	SPVM	O	1.65V	

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Maximum input voltage (Power)	V_{IN_MAX}	16.0	V	VIN*, CHG_STATE
Power supply (Power)	V_{VDD_MAX}	7.0	V	VSYS*,VDD*,PVDD*,AFE_VDD,VIO_IN
Power supply (Audio)	V_{BAT_MAX}	5.5	V	VBAT*,AVDD_DRV*
	V_{DVDD_MAX}	2.0	V	DVDD,AVDD_MIC
I/O pin voltage 1 (Power)	V_{IO1}	-0.3～VDD+0.3	V	Except for maximum input voltage, Power Supply, I/O pin voltage 2~4, and output pins
I/O pin voltage 2 (Power)	V_{IO2}	-0.3～VIO_IN+0.3	V	xRST_OUT, CLK_OUT, INT_OUT, SDA_P, SCL_P, VBUS_OUT
I/O pin voltage 3 (Audio)	V_{IO3}	-0.3～DBAT*+0.3	V	SPAP,SPAN,SPBP,SPBN,MICBIASA,MICBIASB, VMBFILT,XI_A,XO_A,SPVM
I/O pin voltage 4 (Audio)	V_{IO4}	-0.3～DVDD+0.3	V	SDA_A,SCL_A,XRESET,MCLKOUT,AD_DATA, FSCLK,DA_DATA,,CLKOUT_DMIC,GPO_A, MIC_REF,,MICA,MICB,MICC,MICD,MICAREF, MICBREF,MICCREF,MICDREF,
Maximum junction temperature	T_{j_max}	+ 125	°C	
Storage temperature	T_{stg}	-65 ~ +150	°C	

Recommended Operating Conditions

Item	Symbol	Rating	Unit	Remarks
Ambient operating temperature	Ta	-25 ~ +85	℃	
Supply voltage range 1	VIN	4.5 ~ 5.5	V	VIN*
Supply voltage range 2	VSYS	2.5 ~ 4.4	V	VSYS*,VDD*, PVDD*, AFE_VDD
Supply voltage range 3	VIO_IN	1.62 ～ 1.98	V	VIO_IN
Supply voltage range 4	DVDD	1.62 ～ 1.98	V	DVDD,AVDD_MIC
Supply voltage range 5	AVDD_DRV	3.0 ～ 3.6	V	AVDD_DRV*
Supply voltage range 6	VBAT	2.5 ～ 5.5	V	VBAT*
DC-DC converter output inductor	Lo1	2.2	µH	DDC_IO, DDC_CORE VLS2010ET-2R2M(TDK)
	Lo2	10	µH	DDC_ANA VLS2010ET-100M(TDK)
DC-DC converter output capacitance	Co_DDC1	22*2 parallel connection	µF	DDC_IO, DDC_CORE AMK107BBJ226MA-T (Taiyo Yuden Co., Ltd.)
	Co_DDC2	22	µF	DDC_ANA AMK107BBJ226MA-T(Taiyo Yuden Co., Ltd.)
LDO output capacitance	Co_LDO1	1	µF	LDO_USB33, LDO_USB10, LDO_PERI_OUT
	Co_LDO2	10	µF	LDO_EMMC_OUT
	Co_LDO3	22	µF	LDO_ANA_OUT
VREF output capacitance	Co_VREF	0.22	µF	VREF
VBAT capacitance	Co_VBAT	1	µF	VBAT
VSYS output capacitance	Co_VSYS	1	µF	VSYS
VSYS line total capacitance	C_VSYSALL	10~100	µF	Total including the VDD and PVDD line input capacitance (effective capacitance)
Crystal oscillation frequency	f_{XT}	32.768	kHz	NX3215SA(NDK), TFX-04(RIVER ELETEC) The capacity in the CHIP is 9.5pF (Typ). The CL level of the crystal assumes a thing of 5.0-6.0pF. 32768 Hz crystal is allowed 55kohm max ESR.
Current sense resistor	Rimon	100	mohm	Set as Ichgmax*Rimon≒50mV
Lithium ion battery capacity	Li-ion_cap	~500	mAh	
Rapid charge current	Ichg_set	100~500	mA	Riset=100~20kohm
Thermistor resistance B constant		4250	K	NCP15WF104F03RC (Murata Manufacturing Co., Ltd.)

Electrical Characteristics

◆Power supply Block

(Unless otherwise specified: Ta = 27 °C, VDD = PVDD1 = PVDD2 =PWR_EN = 3.6 V, VIO_IN = SW_IN = 1.8 V)

Power supply input (VDD, VIO_IN)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Power consumption in VDD operating state	I_{VDD1}	Power ON state, No Switching		60		μA
Power consumption in VDD stop state	I_{VDD2}	PWR_EN = 0V			1	μA
Power consumption in VDD Deep Sleep state	I_{VDD3}	VDD=3.6, Deep Sleep state , VIO_IN=OPEN		2	5	μA
Power consumption in VIO_IN operating state	I_{VIO1}	I2C operation state		3		uA
Power consumption in VIO_IN stop state	I_{VIO2}	I2C stop state (SDA_P and SCL_P pulled up)			0.1	uA
UVLO detection voltage	V_{UVLO_L}		2.40	2.45	2.50	V
UVLO cancel voltage	V_{UVLO_H}		2.50	2.55	2.60	V
UVLO hysteresis width	$\triangle V_{UVLO}$	$\triangle V_{UVLO} = V_{UVLO\_H} - V_{UVLO\_L}$	-	100	-	mV

RTC (XI_P, XO_P)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Crystal oscillation frequency	f_{XT}			32.768		kHz
CLK_OUT output Duty	X_{duty}	* Design guarantee item	10		90	%

LOAD SW (SW_18_IN, SW_18_OUT1-4)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
ON resistor 1 (exclusively for USB-PHY)	R_{ON_SW}	I_{SW} = 50mA; SW_18_IN = 1.75V, SW_18_OUT1	-	0.8	1	Ω
ON resistor 2	R_{ON_SW}	I_{SW} = 50mA; SW_18_IN = 1.75V, SW_18_OUT2~4	-	0.8	1	Ω

IF-IN (PWR_EN, xINT_WKUP_S, xINT_WKUP_L, xINT_SYNC, SCL_P, SDA_P)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PWR_EN pin H level input voltage	V_{IPE_H}		VDD − 0.3	-	-	V
PWR_EN pin L level input voltage	V_{IPE_L}		-	-	0.3	V
xINT_WKUP pin H level input voltage	$V_{IxINT\_WKUP\_H}$		VDD − 0.3	-	-	V
xINT_WKUP pin L level input voltage	$V_{IxINT\_WKUP\_L}$		-	-	0.3	V
xINT_SYNC pin H level input voltage	$V_{IxINT\_SYNC\_H}$		VIO_IN − 0.3	-	-	V
xINT_SYNC pin L level input voltage	$V_{IxINT\_SYNC\_L}$		-	-	0.3	V
SCL_P pin H level input voltage	$V_{ISCL\_P\_H}$		VIO_IN − 0.3	-	-	V
SCL_P pin L level input voltage	$V_{ISCL\_P\_L}$		-	-	0.3	V
SDA_P pin H level input voltage	$V_{ISDA\_P\_H}$		VIO_IN − 0.3	-	-	V
SDA_P pin L level input voltage	$V_{ISDA\_P\_L}$		-	-	0.3	V

IF-OUT (CLK_OUT, INT_OUT, xRST_OUT, VBUS_OUT, GPO0-7, DDC_ON)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
CLK_OUT pin H level output voltage	$V_{OCLK\_OUT\_H}$	I_{OUT} =-2mA	VIO_IN – 0.2V	-	-	V
CLK_OUT pin L level output voltage	$V_{OCLK\_OUT\_L}$	I_{IN} =+2mA	-	-	0.2	V
INT_OUT pin H level output voltage	$V_{OINT\_OUT\_H}$	I_{OUT} =-2mA	VIO_IN – 0.2V	-	-	V
INT_OUT pin L level output voltage	$V_{OINT\_OUT\_L}$	I_{IN} =+2mA	-	-	0.2	V
xRST_OUT pin H level output voltage	$V_{OxRST\_OUT\_H}$	I_{OUT} =-2mA	VIO_IN – 0.2V	-	-	V
xRST_OUT pin L level output voltage	$V_{OxRST\_OUT\_L}$	I_{IN} =+2mA	-	-	0.2	V
VBUS_OUT pin H level output voltage	$V_{OVBUS\_OUT\_H}$	I_{OUT} =-2mA	VIO_IN – 0.2V	-	-	V
VBUS_OUT pin L level output voltage	$V_{OVBUS\_OUT\_L}$	I_{IN} =+2mA	-	-	0.2	V
GPO0~7 pin H level output voltage	V_{OGPO1_H}	I_{OUT} =-2mA	VDD – 0.2V	-	-	V
GPO0~7 pin L level output voltage	V_{OGPO1_L}	I_{IN} =+2mA	-	-	0.2	V
DDC_ON pin H level output voltage	$V_{DDC\_ON\_H}$	I_{OUT} =-2mA	VDD – 0.2V	-	-	V
DDC_ON pin L level output voltage	$V_{DDC\_ON\_L}$	I_{IN} =+2mA	-	-	0.2	V

DDC_IO

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Maximum output current*1	I_{DIO_MAX}		200			mA
Inductor peak current*1	I_{DIO_LP}				1000	mA
Output voltage*1	V_{DIO}	VDD=2.5~4.4V, Io=1~200mA	1.65	1.80	1.95	V
Output feedback voltage	V_{DIO_FB}		1.77	1.80	1.83	V
Maximum operating frequency*1	F_{DIO_FMAX}	Io = 0 mA, maximum frequency at start-up			1	MHz
Output start-up time*1	T_{DIO}			0.2	0.4	ms
Output ON resistor (H side)	R_{ONH_DIO}				0.3	ohm
Output ON resistor (L side)	R_{ONL_DIO}				0.15	ohm

*1 Design guarantee item when using the recommended parts

DDC_ANA

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Maximum output current*1	I_{DANA_MA}		6			mA
Inductor peak current*1	I_{DANA_LP}				150	mA
Output voltage*1	V_{DANA}	VDD=2.5~4.4V, Io=0~6mA, VO_D_ANA[5:0] = 0Ch	0.65	0.70	0.75	V
Output feedback voltage	V_{DANA_FB}	VO_D_ANA[5:0] = 0Ch	0.690	0.700	0.710	V
Maximum operating frequency*1	F_{DANA_FMAX}	Io=0mA, maximum frequency at start-up			2	MHz
Output start-up time*1	T_{DANA}			0.5	1	ms
Output ON resistor (H side)	R_{ONH_DANA}				2	ohm
Output ON resistor (L side)	R_{ONL_DANA}				1	ohm

*1 Design guarantee item when using the recommended parts

DDC_CORE

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Maximum output current*1	I_{DCORE_MA}		100			mA
Inductor peak current*1	I_{DCORE_LP}				500	mA
Output voltage 1*1	V_{DCORE1}	VDD=2.5~4.4V, Io=0~100mA, VO_D_CORE[5:0] = 0Ch	0.65	0.70	0.75	V
Output voltage 2*1	V_{DCORE2}	VDD=2.5~4.4V, Io=0~100mA, VO_D_ CORE [5:0] = 24h	0.90	1.00	1.10	V
Output feedback voltage	V_{DCORE_FB}	VO_D_ CORE [5:0] = 0Ch	0.69	0.70	0.71	V
Maximum operating frequency*1	F_{DCORE_FMAX}	Io = 0 mA, maximum frequency at start-up			2	MHz
Output start-up time*1	T_{DCORE}			0.4	1	ms
Output ON resistor (H side)	R_{ONH_DCORE}				0.8	ohm
Output ON resistor (L side)	R_{ONL_DCORE}				0.6	ohm

*1 Design guarantee item when using the recommended parts

LDO_EMMC

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PSRR LDO_IN	$PSRR_{LEMMC}$	1kHz~100KHzPeak（Io=0A, 100mA）		30		dB
Maximum output current	$I_{LEMMCmax}$		100			mA
Output voltage	V_{LEMMC}	Register setting: VO_L_EMMC[1:0] = 00h (Default)	3.15	3.3	3.45	V
Input stability	$V_{LEMMCivs}$	VDD= V_{LEMMC} +0.2~4.4V			10	mV
Output stability	$V_{LEMMCAls}$	Io=0~100mA			2	mV
Voltage difference between input and output	$V_{LEMMCIO}$	LDO_EMMC_IN = 3.0 V, Io = 100 mA, Vo = 3.3 V settings	2.8			V

LDO_PERI

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PSRR LDO_IN	$PSRR_{LPERI}$	1kHz~100KHzPeak（Io=0A, 10mA）		30		dB
Maximum output current	$I_{LPERImax}$		10			mA
Output voltage	V_{LPERI}	Register setting: VO_L_PERI[1:0] = 00h (Default)	3.15	3.3	3.45	V
Input stability	$V_{LPERIvs}$	VDD=2.5~4.4V			10	mV
Output stability	$V_{LPELIls}$	Io=0~10mA			2	mV
Voltage difference between input and output	$V_{LPELIIO}$	LDO_EMMC_IN=3.0V, Io=10mA, Vo=3.3V settings	2.8			V

LDO_ANA

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Input voltage range	V_{LANA_IN}		V_{LANA} +0.2		VDD	V
PSRR LDO_IN	$PSRR_{LANA1}$	10kHz～2MHzPeak（Io=0A, 100uA, 1mA, 6mA）		55		dB
PSRR VDD	$PSRR_{LANA2}$	10kHz～2MHzPeak（Io=0A, 100uA, 1mA, 6mA）		50		dB
Maximum output current	$I_{LANAmax}$		6			mA
Output voltage	V_{LANA}	Register setting: VO_L_ANA[5:0] = 0Ch (Default)	0.65	0.700	0.75	V
Input stability	$V_{LANAivs}$	VDD=2.5~4.4V			3	mV
Output stability	V_{LANAls}	Io=0~6mA			2	mV

1.0V output for USBPHY (LDO_USB10)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PSRR LDO_IN	$PSRR_{LVIN2}$	1kHz~100KHzPeak（Io=0A, 10mA）		30		dB
Maximum output current	$I_{USB10max}$	* Max. 50 mA due to overcurrent limiter	10		50	mA
Output voltage	V_{USB10}		0.95	1.00	1.05	V
Input stability	$V_{LUSB10ivs}$	VIN=2.5~5.5V			10	mV
Output stability	$V_{LUSB10ls}$	Io=0~10mA			2	mV

List of DC-DC converter and LDO output register settings

Setting voltage of each power supply and code Unit[V]

Address	DDC_ANA	DDC_CORE	LDO_ANA	LDO_EMMC	LDO_PERI
00h		0.55		3.3	3.3
01h		0.5625		3.2	3.2
02h		0.575		3.1	3.1
03h		0.5875		3.0	3.0
04h	0.6	0.6	0.6	2.9	2.9
05h	0.6125	0.6125	0.6	2.8	2.8
06h	0.625	0.625	0.625	2.7	2.7
07h	0.6375	0.6375	0.625	2.6	2.6
08h	0.65	0.65	0.65	2.5	2.5
09h	0.6625	0.6625	0.65	2.4	2.4
0Ah	0.675	0.675	0.675	2.3	2.3
0Bh	0.6875	0.6875	0.675	2.2	2.2
0Ch	0.7	0.7	0.7	2.1	2.1
0Dh	0.7125	0.7125	0.7	2.0	2.0
0Eh	0.725	0.725	0.725	1.9	1.9
0Fh	0.7375	0.7375	0.725	1.8	1.8
10h	0.75	0.75	0.75		
11h	0.7625	0.7625	0.75		
12h	0.775	0.775	0.775		
13h	0.7875	0.7875	0.775		
14h	0.8	0.8	0.8		
15h	0.8125	0.8125	0.8		
16h	0.825	0.825	0.825		
17h	0.8375	0.8375	0.825		
18h	0.85	0.85	0.85		
19h	0.8625	0.8625	0.85		
1Ah	0.875	0.875	0.875		
1Bh	0.8875	0.8875	0.875		
1Ch	0.9	0.9	0.9		
1Dh	0.9125	0.9125	0.9		
1Eh	0.925	0.925	0.925		
1Fh	0.9375	0.9375	0.925		
20h	0.95	0.95	0.95		
21h	0.9625	0.9625	0.95		
22h	0.975	0.975	0.975		
23h	0.9875	0.9875	0.975		
24h	1.0	1.0	1.0		

Unit[V]

Address	DDC_ANA	DDC_CORE
25h	1.0125	1.0125
26h	1.025	1.025
27h	1.0375	1.0375
28h	1.05	1.05
29h	1.0625	1.0625
2Ah	1.075	1.075
2Bh	1.0875	1.0875
2Ch	1.1	1.1
2Dh	1.1125	1.1125
2Eh	1.125	
2Fh	1.1375	
30h	1.15	
31h	1.1625	
32h	1.175	
33h	1.1875	
34h	1.2	
35h	1.2125	
36h	1.225	
37h	1.2375	
38h	1.25	
39h	1.2625	
3Ah	1.275	

* Blue cell values cannot be set (input).
* Yellow cell values are the default settings

◆Analog front-end block for battery power level detection

(Unless otherwise specified: Ta = 27 °C, VBAT = VSYS = VDD_AFE = 3.6 V)

Power supply input (AFE_VDD)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Supply voltage range	V_{DD}		2.5		4.4	V
Operating power consumption	I_{AVD_ACT}	At the time of measurement		100	200	μA
Current consumption when stopped	I_{AVD_SLP}				0.2	μA

Battery voltage, battery temperature measurement (VBAT_VS, TH)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Battery voltage measurement range		VBAT_VS voltage measurement	2.5		4.5	V
Battery voltage measurement resolution				1.1		mV/LSB
Battery voltage measurement accuracy			-4.4(-4)		+4.4(4)	mV(LSB)
Measurement cycle*2		Register：82h/83h ※Default 125ms	125ms		18.2h	
Battery temperature measurement range		TH voltage measurement	0		2.0	V
Battery temperature measurement resolution				0.5		mV/LSB
Battery temperature measurement accuracy			-1		+1	℃
Measurement cycle*2		Register：82h/83h ※Default 125ms	125ms		18.2h	

*2 Measurement is performed at a 7.8 ms cycle during charge.

Battery charge / discharge current measurement (VBT_CS, VSYS_CS)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Current measurement range		Between VSYS_CS and VBAT_CS	-50		50	mV
Current measurement resolution		Between VSYS_CS and VBAT_CS		30		uV/LSB
Current measurement accuracy		Between VSYS_CS and VBAT_CS =10mV	-5		+5	%
Current measurement offset		When VSYS_CS=VBAT_CS (0mA setting) output	-5	0	+5	LSB
Measurement cycle *2		Register：82h/83h ※Default 125ms	125ms		18.2h	

*2 Measurement is performed at a 7.8 ms cycle during charge.

Battery temperature detection and control (VREF, TH_REF)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Reference voltage	V_{ref}			2		V
Reference voltage SW_ON resistor	R_{ON_THREF}	I_{THSW} = 20uA	-	(10)	100	Ω

* Shared with the charge control block

◆Charge control block

(Unless otherwise specified: Ta = 27 °C, VIN = 5V, VBAT=3.6V)

Power path control, shared (VIN, VBT, VSYS)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
VIN detection L side	V_{vinl}	When the VIN voltage rises * 200 mV hysteresis	3.6	3.8	4.0	V
VIN detection H side	V_{vinh}	When the VIN voltage rises * 100 mV hysteresis	5.6	5.8	6.0	V
VSYS detection relative to VIN	V_{inbat}		VSYS -0.2	VSYS -0.1	VSYS	V
Battery discharge current 1	I_{dc1}	VIN=5V, VBAT=4.2V, when power supply block stopped, charge complete			2	uA
Battery discharge current 2	I_{dc2}	VIN=0V , VBAT=4.2V , when power supply block stopped			1	uA
Circuit current	I_{cc}	VIN=5V , when power supply block stopped ※VIN current			1	mA
Chip temperature control	T_{cc}	* Design guarantee item		100		℃
Thermal shutdown	T_{sd}	* Design guarantee item		150		℃

* The battery discharge current is measured at the VSYS pin.

Battery voltage detection and control (VBAT)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Precharge start voltage	$V_{pcstart}$	When the VBAT voltage rises	1.3	1.4	1.5	V
Weak battery judgment voltage	$V_{weakbat}$	When the VBAT voltage rises	3.3	3.4	3.5	V
		Resistor variable range 20mV-step	2.6	-	3.6	V
Rapid charge start voltage	$V_{qcstart}$	When the VBAT voltage rises	2.9	3.0	3.1	V
		Resistor variable range 200mV-step	2.6	-	3.2	V
Charge control voltage	V_{chg}	Ichg=10mA ※Ta=0~60℃	4.17	4.20	4.23	V
		Resistor variable range 50mV-step	4.0	-	4.4	V
Recharge start voltage	$V_{rcstart}$	During VBAT voltage step down	V_{chg}-0.45	V_{chg}-0.4	V_{chg}-0.35	V
		Resistor variable range 100mV-step	V_{chg}-0.4	-	V_{chg}-0.25	V
Charge complete voltage	V_{fv}	Function enable/disable is selected by the register. * Default: enable		$V_{rcstart}$+0.1		V

Charge current detection and control (CHG_ISET)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Rapid charge current	I_{chg}	Riset=33kohm , VBAT=3.6V	250	300	350	mA
Precharge current	I_{pchg}	Riset=33kohm , VBAT=2.2V, ※I_{chg}*0.2		60		mA
Initial charge current	I_{ppchg}	VBAT=1.0V	5	10	20	mA
Charge complete current	I_{fc}	When setting to 30mA	25	30	35	mA
		Resistor variable range10mA-step	10	-	50	mA

* The charge current can be varied by an external resistor. :Ichg=10000/Riset

Battery temperature detection and control (VREF, TH)

※The thermistor resistor for temperature measurement assumes the NCP15WF104F03RC

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Reference voltage for temperature detection	T_{ref}	Ro=200kohm		2		V
Battery connection detection	T_{thc}			T_{ref}*0.9		V
Temperature detection 1-1*3	T_{th1-1}	Hysteresis of 2.5°C on the temperature rise side relative to 0°C		0		℃
Temperature detection 1-2*4	T_{th1-1}		0.0		15.0	℃
Temperature detection 2*3	T_{th2}	Hysteresis of 2.5°C on the temperature rise side relative to 10°C		10		℃
Temperature detection 3*3	T_{th3}	Hysteresis of 2.5°C on the temperature rise side relative to 45°C		45		℃
Temperature detection 4-1*3	T_{th4-1}	Hysteresis of 2.5°C on the temperature rise side relative to 60°C		60		℃
Temperature detection 4-2*4	T_{th4-2}		45.0		60.0	℃

*3 Judged by the digital comparator output (set by 78h to 7Fh)

*4 Temperature detection 1-2 and 4-2 are when VBAT < $V_{qcstart}$ (before rapid charge, before HOST start-up).

3.3V output for USBPHY (LDO_USB33)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PSRR LDO_IN	$PSRR_{LVIN1}$	1kHz~100KHzPeak（Io=0A, 10mA）		-20		dB
Maximum output current	$I_{USB33max}$	* Max. 50 mA due to overcurrent limiter	10		50	mA
Output voltage	V_{USB33}		3.2	3.3	3.4	V
Input stability	$V_{LUSB33ivs}$	VIN=4.5~5.5V			10	mV
Output stability	$V_{LUSB33ls}$	Io=0~10mA			2	mV

USB detection (DP, DM, DLINE_SW)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
DP pin output voltage	V_{dp}	I_{dpo}=0~150uA	0.5	0.6	0.7	V
DP pin maximum source current	I_{dp}		150			uA
DM pin sink current	I_{dm}	V_{dpo}=0.6V	50		150	uA
Voltage detection	V_{dpm}		0.25		0.4	V
DLINE_SW pin H level output voltage	V_{ODL_H}	I_{OUT} =-2mA	V_{USB33} − 0.2V	-	-	V
DLINE_SW pin L level output voltage	V_{ODL_L}	I_{IN} =+2mA	-	-	0.2	V

Timers and setup times

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Initial charge timer	T_{ppc}		7	10	13	sec
Weak Battery timer	T_{wb}		24	34	44	min
Precharge timer	T_{pc}	Changeable to 120 min by the register	54	60	66	min
Rapid charge timer	T_{qc}	Changeable to 300 min by the register	540	600	660	min
Battery voltage setup time Battery temperature setup time	T_{bvd}	Setup by the 31 ms-clk matching 4 times Setup by the 31 ms-clk matching 4 times	3		4	Clk
Charge current setup time	T_{bcd}	Setup by the 250ms-clk matching 4 times * Changeable to x10 by the register	3		4	Clk

◆Audio block

MICs to serial output characteristics

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC = 1.8 V, DVDD = 1.8 V, VBAT = 3.7 V, GND_MIC =DGND = 0 V, OSCIN = 512•48 kHz, Input test signal is a 1 kHz sine wave, Measurement bandwidth is 20 Hz to 20 kHz)

Parameters	Symbol	Min	Typ	Max	Condition	Units
Input impedance	RMICIN		50			kΩ
DC voltage at MICx	VCM	-	AVDD_MIC/2	-		V
Full-scale input voltage	FSMIC	-	AVDD_MIC/2	-		Vpp
Signal to noise ratio	SNRMIC	-	90	-	A-weight, MICGAINx=0dB	dB
THD+N	THDMIC	-	-80	-	-6dBFS, MICGAINx=0dB	dB
Dynamic range	DRMIC	-	90	-	A-weight, MICGAINx=0dB	dB
Crosstalk	CTMIC	-	100	-	1kHz	dB
MICGAIN range	MICGAINx	0	-	15		dB
MICGAIN step	MICSTEPx	2.9	3	3.1		dB
PGAGAIN range	PGAGAINx	0	-	6		dB
PGAGAIN step	PGASTEPx	0.4	0.5	0.6		dB

serial input to SPOUTs characteristics (Loop OFF)

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC = 1.8 V, DVDD = 1.8 V, VBAT = 3.7 V, AGND_MIC = DGND = 0 V, OSCIN = 512•48 kHz, Input test signal is a 1 kHz sine wave, Measurement bandwidth is 20 Hz to 20 kHz, test load R_L = 8Ω, C_L = 150 pF for bridge tied an ear speaker load.)

Parameters	Symbol	Min	Typ	Max	Condition	Units
Power output per channel	PO	-	400	-	0dB FS input/Codec gain=24dB	mW
Total harmonic distortion + noise	THDSP	-	-60	-54	Input Amplitude=-6dBFS	dB
Output Noise	Vnoise	-	10	-	A-weight	uVrms

serial input to SPOUTs characteristics (Loop ON)

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC = 1.8 V, DVDD = 1.8 V, VBAT = 3.7 V, AGND_MIC = DGND = 0 V, OSCIN = 512•48 kHz, Input test signal is a 1 kHz sine wave, Measurement bandwidth is 20 Hz to 20 kHz, test load R_L = 8Ω, C_L = 150 pF for bridge tied an ear speaker load.)

Parameters	Symbol	Min	Typ	Max	Condition	Units
Power output per channel	PO	-	400	-	0dB FS input/Codec gain=24dB	mW
Total harmonic distortion + noise	THDSP	-	-66	-60	Input Amplitude=-6dBFS	dB
Output Noise	Vnoise	-	10	-	A-weight	uVrms

DC characteristics

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC = 1.8 V, DVDD = 1.8 V, VBAT = 3.7 V, AGND_MIC = DGND = 0 V, OSCIN = 512•48 kHz)

Parameters	Symbol	Min	Typ	Max	Condition	Units
MICx_BIAS						
	VO_{MICBS}	-	0	-	Low Output mode	V
		1.8	2.0	2.2		
		-	Hi-Z	-	Stand by mode	
Output current	IO_{MICBS}	-	-	2.0	low noise mode	mA
Output noise	NO_{MICBS}	-	-	5	low noise mode	μVrms
Output impedance	RO_{MICBS}	40	60	80	low noise mode	Ω
Output impedance	RO_{MICBS}	-	60	-	low power mode	Ω
		16k	20k	24k		
		80k	100k	120k		
LDO for MICIN						
LDOOUT voltage	VREG18	1.62	1.8	1.98		V

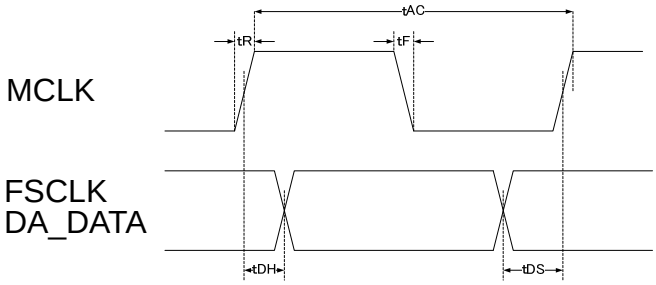
Crystal switching specification

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC =.8 V, DVDD = 1.8 V, VBAT = 3.7 V, AGND_MIC = DGND = 0 V)

Parameters	Symbol	Min	Typ	Max	Condition	Units
XI_A frequency	FREQ	-	24.576	-		MHz
		-	49.152	-		

Switching specifications and characteristics (serial audio interface form CXD5602)

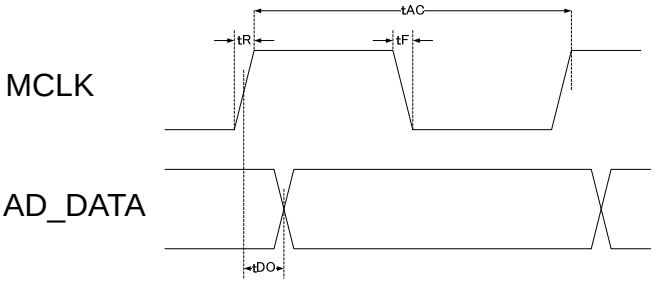
Parameters	Symbol	Min	Typ	Max	Condition	Units
Serial data input1 - FSCLK/DA_DATA						
MCLK clock frequency	-	-	24.576	-		MHz
MCLK clock duty cycle	-	40	50	60		%
MCLK clock period	tAC		40.69			ns
Rise time	tR			5.0		ns
Fall time	tF			5.0		ns
Setup time	tDS	5.0				ns
Hold time	tDH	0.0				ns



MCLK/FSCLK/DA_DATA timing

Switching specifications and characteristics (serial audio interface to CXD5602)

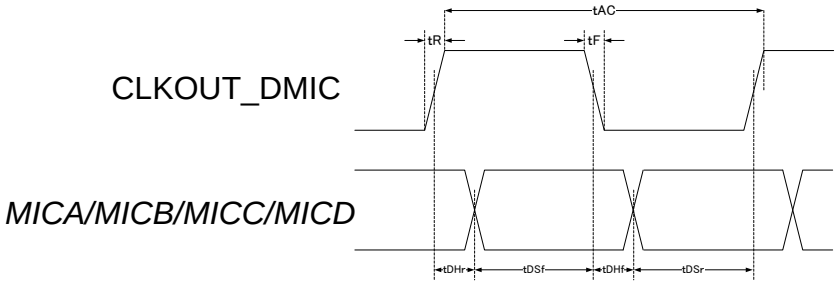
Parameters	Symbol	Min	Typ	Max	Condition	Units
Serial data output - MCLK/AD_DATA						
MCLK clock frequency	-	-	24.576	-		MHz
MCLK clock duty cycle	-	40	50	60		%
MCLK clock period	tAC		40.69			ns
Rise time	tR			5.0		ns
Fall time	tF			5.0		ns
Data Delay	tDO	3.0		15.0		ns



MCLK/AD_DATA timing

digital microphone interface

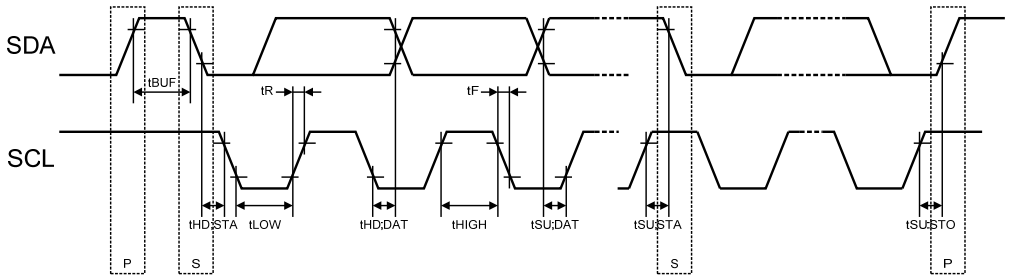
Parameters	Symbol	Min	Typ	Max	Condition	Units
Digital MIC input1 - DMCLK = 3.072 MHz						
CLKOUT_DMIC clock frequency	-	-	3.072	-		MHz
CLKOUT_DMIC clock duty cycle	-	40	50	60		%
CLKOUT_DMIC clock period	tAC		325.52			ns
Rise time	tR			5.0		ns
Fall time	tF			5.0		ns
Setup time	tDSr/tDSf	5.0				ns
Hold time	tDHf/tDHr	0.0				ns
Digital MIC input1 - DMCLK = 1.024 MHz (DDR input)						
CLKOUT_DMIC clock frequency	-	-	1.024	-		MHz
CLKOUT_DMIC clock duty cycle	-	40	50	60		%
CLKOUT_DMIC clock period	tAC		976.56			ns
Rise time	tR			5.0		ns
Fall time	tF			5.0		ns
Setup time	tDSr/tDSf	5.0				ns
Hold time	tDHf/tDHr	0.0				ns



DMCLK/DMIC timing

I2C bus switching specification

Parameters	Symbol	Min	Typ	Max	Condition	Units
Clock frequency	f_{SCL}	0	-	400		kHz
Data charge minimum waiting time	t_{BUF}	1.3	-	-		µs
Data transfer start waiting time	$t_{HD:STA}$	0.6	-	-		µs
Low level clock pulse width	t_{LOW}	1.3	-	-		µs
High level clock pulse width	t_{HIGH}	0.6	-	-		µs
Start setup waiting time	$t_{SU:STA}$	0.6	-	-		µs
Data hold time	$t_{HD:DATA}$	0	-	-		µs
Data setup time	$t_{SU:STA}$	100	-	-		ns
Rise time	t_R	-	-	300		ns
Fall time	t_F	-	-	300		ns
Stop setup waiting time	$t_{SU:STO}$	0.6	-	-		µs



I2C timing

digital input / output signal threshold level

Parameters	Symbol	Min	Typ	Max	Condition	Units
High-level output voltage	V_{OH}	DVDD - 0.2	-	-		V
Low-level output voltage	V_{OL}	-	-	0.2		V
High-level input voltage	V_{IH}	0.7 x DVDD	-	-		V
Low-level input voltage	V_{IL}	-	-	0.3 x DVDD		V

Power consumption (audio block)

The table below lists the current consumed by each Adonis internal power supply pin. This enables to calculate the overall power in accordance with the use case.

Block	Operating state	Pin	Min	Typ	Max	Conditon	Unit
Logic	When reset	DVDD		0.1	-		uA
	Analog Mic input SPOUT output				5	When Xtal 24.576MHz FSCLK/AD_DATA pin load 10 pF	mA
MICIN	Sleep	AVDD_MIC			10		uA
	1ch operation				3.6	Typ: approximately 2.5 mA	mA
	2ch operation				6.6	Typ: approximately 5 mA	mA
	4ch operation				12.6	Typ: approximately 10 mA	mA
	Digital MIC				1	When using Digital MIC	mA
Crystal buffer	Sleep	VBAT2		0.05	2	XRESET=Low	uA
	24.576MHz			1	1.5	SPOUT not used, oscillation stable	mA
	49.152MHz			1.2	1.8	SPOUT not used, oscillation stable	mA
	24.576MHz mono			1.1	1.65	SPOUT BTL mono, oscillation stable	mA
	24.576MHz Stereo			1.2	1.8	SPOUT BTL stereo, oscillation stable	mA
	49.152MHz mono			1.4	2.1	SPOUT BTL mono, oscillation stable	mA
	49.152MHz Stereo			1.6	2.4	SPOUT BTL stereo, oscillation stable	mA
MICBIAS	Sleep	VBAT1		0.05	1		uA
	MICBIAS 1ch			0.23	0.32	MICBIAS only operating	mA
	MICBIAS 2ch			0.16	0.24		mA
MICINLDO	Active			1.2	1.7	MICIN block current not included	mA
SPOUT	Sleep	AVDD_DRV*			0.1		uA
	Stereo 16fs			1.6		BTLstereo24.576MHz Max = about 3.6mA	mA
	Stereo 32fs			3.2		BTL stereo 49.152MHz Max= abount 5.34mA	mA
	Stereo 16fs Loop			8.6		BTLstereo24.576MHz, Loop ON Max= about 10.18mA	mA
	Stereo 32fs Loop			7.8		BTL stereo 49.152MHz, Loop ON Max= about 11.94mA	mA

Description of Functions

◆Power supply block

RTC

- Low power consumption IQ = 3 μA(typ.)
- Clock, start-up timer

Voltage step down type PFM control DC-DC converter

- Low power consumption IQ = 10μA (per channel)
- DDC_IO / Vout = 1.8 V/ Iomax = 200mA(min)
- DDC_ANA / Vout = 0.600 V～1.275 V, 25 mV-step / Iomax = 6 mA(min)
- DDC_CORE / Vout = 0.5500 V～1.1125 V, 12.5mV-step / Iomax = 100 mA(min)

LDO

- Low power consumption IQ = 6 μA (1ch per channel)
- LDO_ANA / Vout = 0.600 V～1.000 V, 25 mV-step / Iomax = 6 mA(min)
- LDO_EMMC / Vout = 1.8V～3.3V,100mV-step / Iomax = 100 mA(min)
- LDO_PERI / Vout = 1.8V～3.3V,100mV-step / Iomax = 10 mA(min)
- LDO_USB10 for USB-PHY / Vout = 1.0V/ Iomax = 10 mA(min)

External interface

- Load switch (4ch for 1.8 V)
- Communication (I2C serial interface, 32.768 kHz clock, reset, interrupt start-up control)
- GPO (8 systems, general-purpose switch drive, enable drive)
- USB detection (USB connection signal, Data line switch control signal)

◆Analog front-end block for battery power level detection

- On-chip 12-bit ADC (1ch: time sharing control) for battery power level detection and battery voltage, current and temperature measurement in the CXD5602 System

◆Charge control block

- Standalone type charge function
- Protective function
- Conformity to USB battery charging 1.2 (conformance as a system)
- USB detection (USB connection signal, Data line switch control signal)
- LDO_USB33 for USB-PHY / Vout =3.3V / Iomax = 10 mA(min)

◆Audio block

CXD5247 Audio is an analog audio I/O IC developed for the CXD5602 System. CXD5602 performs signal transfer using an original format. The two crystal types of 24.576 MHz and 49.152 MHz are supported as the clock source. The input systems include a ΔΣ ADC that supports four analog MIC inputs and an 8-channel digital MIC interface. The analog MIC input and digital MIC input pins are shared and used exclusively. The output system is a BTL configuration S-Master Speaker Driver (L/R) output. In addition, two systems of MIC bias circuits and a 1.8 V output LDO for MIC input are mounted.

Definition of fs

This specification defines fs as follows: **fs = 48 kHz**

Power Up constraint

CXD5247 Audio power-on (including reset signal assert) is subject to the restrictions noted in the table below.

(When external AVDD_MIC is supplied)

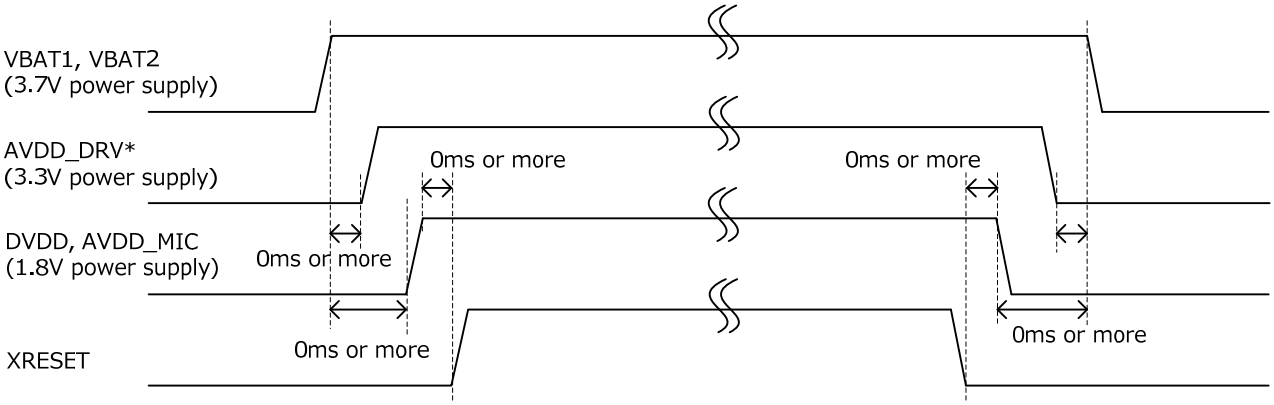
VBAT1/VBAT2	DVDD	AVDD_MIC	AVDD_DRV*	XRESET	Restrictions
OFF	OFF	OFF	OFF	0	**Allowed**
OFF	OFF	OFF	OFF	1	**Not Allowed**
OFF	OFF	OFF	ON	0	**Not Allowed**
OFF	OFF	OFF	ON	1	**Not Allowed**
OFF	OFF	ON	OFF	0	**Not Allowed**
OFF	OFF	ON	OFF	1	**Not Allowed**
OFF	OFF	ON	ON	0	**Not Allowed**
OFF	OFF	ON	ON	1	**Not Allowed**
OFF	ON	OFF	OFF	0	**Not Allowed**
OFF	ON	OFF	OFF	1	**Not Allowed**
OFF	ON	OFF	ON	0	**Not Allowed**
OFF	ON	OFF	ON	1	**Not Allowed**
OFF	ON	ON	OFF	0	**Not Allowed**
OFF	ON	ON	OFF	1	**Not Allowed**
OFF	ON	ON	ON	0	**Not Allowed**
OFF	ON	ON	ON	1	**Not Allowed**
ON	OFF	OFF	OFF	0	**Allowed**
ON	OFF	OFF	OFF	1	**Not Allowed**
ON	OFF	OFF	ON	0	**Allowed**
ON	OFF	OFF	ON	1	**Not Allowed**
ON	OFF	ON	OFF	0	**Allowed**
ON	OFF	ON	OFF	1	**Not Allowed**
ON	OFF	ON	ON	0	**Allowed**
ON	OFF	ON	ON	1	**Not Allowed**
ON	ON	OFF	OFF	0	**Allowed**
ON	ON	OFF	OFF	1	**Allowed**
ON	ON	OFF	ON	0	**Allowed**

ON	ON	OFF	ON	1	**Allowed**
ON	ON	ON	OFF	0	**Allowed**
ON	ON	ON	OFF	1	**Allowed**
ON	ON	ON	ON	0	**Allowed**
ON	ON	ON	ON	1	**Allowed**

Power Up/Reset assert sequence constraint

The CXD5247 Audio power-on sequence and reset cancel restrictions are shown below. Figure ? shows the timing sequence. (When external AVDD_MIC is applied)

- XRESET is canceled after VBAT1, VBAT2 and DVDD have risen.
- AVDD_DRV* should rise after VBAT1 and VBAT2 have risen.
- AVDD_DRV* also supports use cases when power supply is not turned on.



Power Up sequence

Supported crystals / clocks

This IC supports the following crystal frequencies.

Supported crystal frequencies

Symbol	Frequency	Description
XI_A XO_A	24.576MHz	Master clock, 512fs
	49.152MHz	Master clock, 1024 fs, Hi-Res operation

An external clock (0 V - 1.8 V square wave) can also be applied to the OSCIN pin.

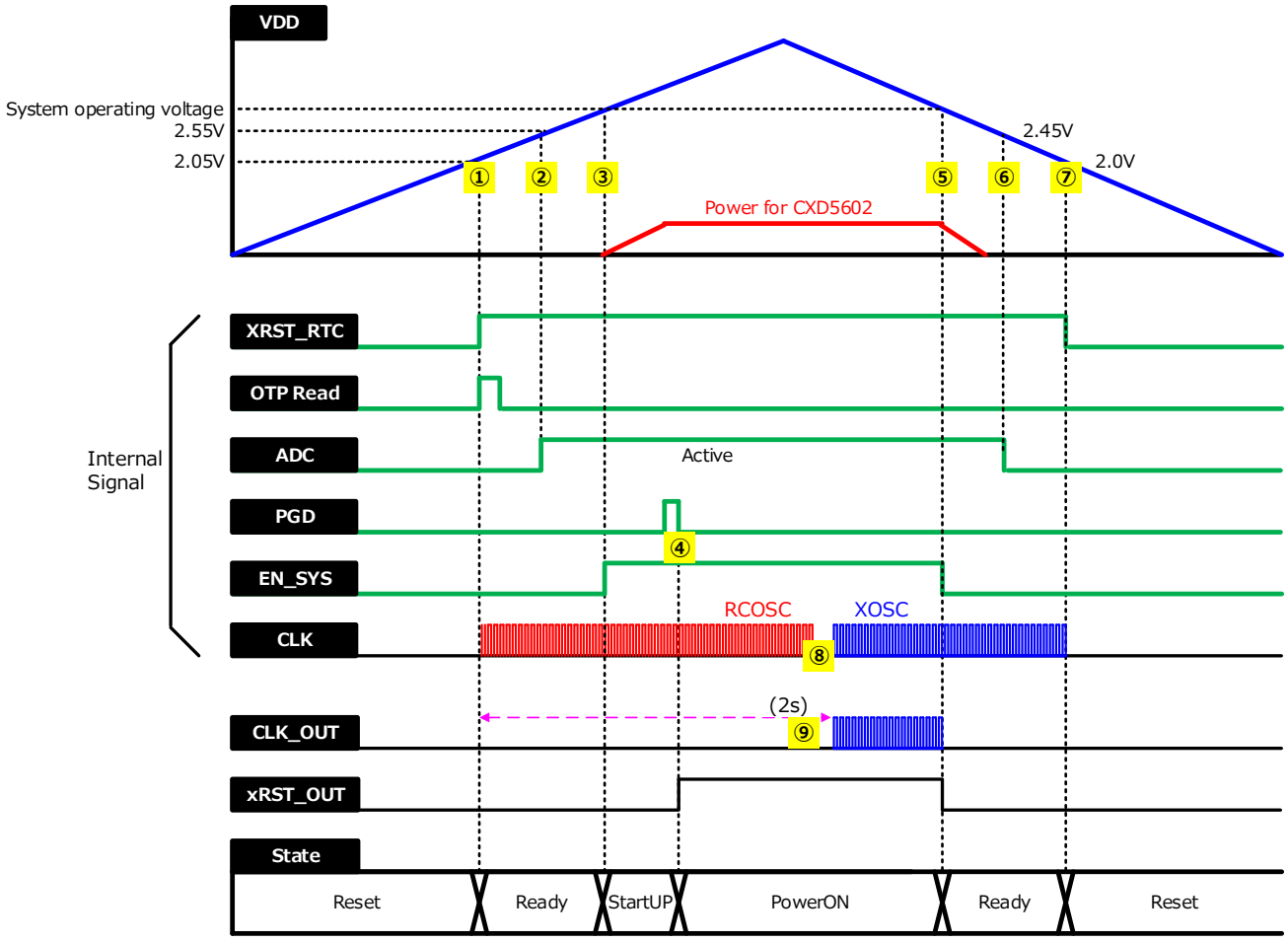
Frequency when applying an external clock

Symbol	Frequency	Description
XI_A	24.576MHz	Master clock, 512fs
	49.152MHz	Master clock, 1024fs Hi-Res operation

Description of Operation

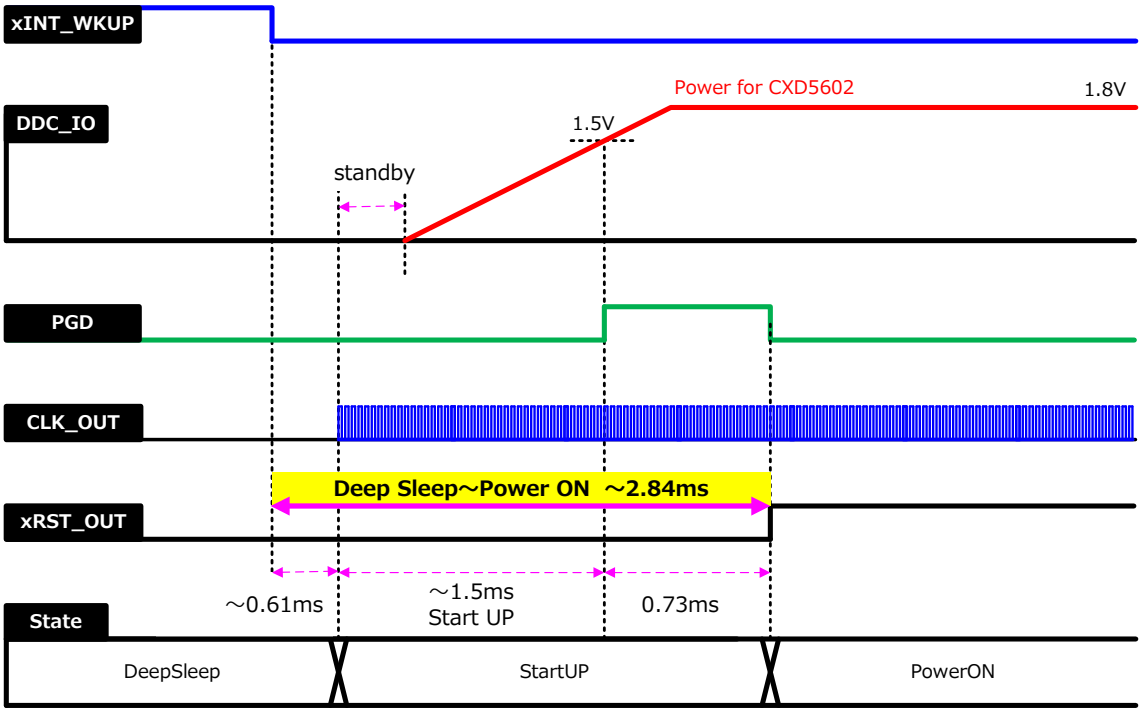
◆Power supply block operation sequence

Timing chart (Start UP to Stop)

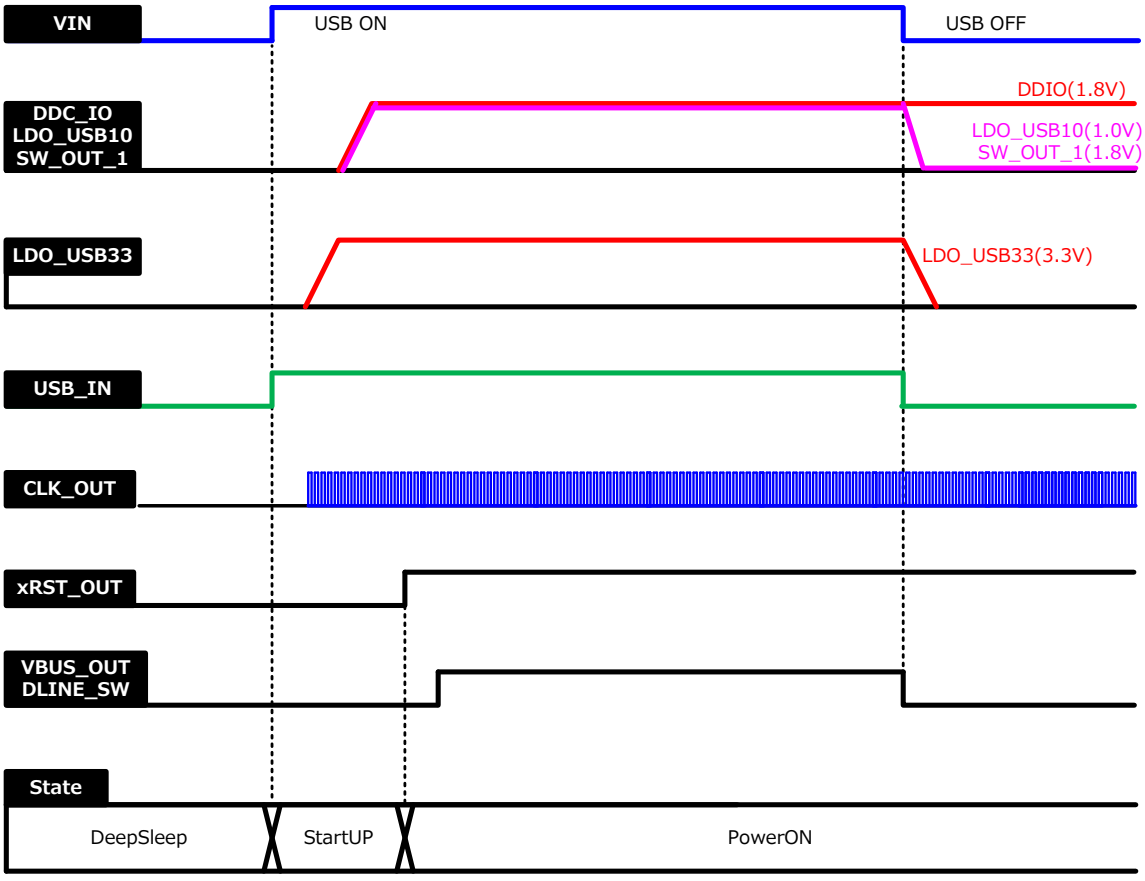


No.	Description	State
1	Detect 2.05 V and cancel the internal circuit reset state. * Read and reflect the OTP data for the analog circuits after reset cancel.	Reset→Ready
2	Detect 2.55 V and start ADC operation. (Only the battery voltage is measured in the Ready state.)	Ready
3	Detect the system operating voltage (3Ch: Def BDh) or more and start up the power supply block. This detection is performed by comparing the register setting value and the ADC data (digital comparator).	Ready→StartUP
4	Perform state transition by detecting the rise of the CXD5602 power supplies (4 systems: DDC_IO/ANA/CORE and LDO_ANA).	StartUP→PowerON
5	Detect the system operating voltage or less and stop power supply output (power supply block operation). * 4-bit (72 mV) hysteresis control is performed on the voltage step down side relative to the 3Ch setting value.	PowerON→Ready
6	Detect 2.45 V (100 mV hysteresis control relative to the rise 2.55 V) and stop ADC operation.	Ready
7	Detect 2.0 V (50 mV hysteresis control relative to the rise 2.05 V) and stop operation.	Ready→Reset
8	Operation uses the internal RC oscillation circuit (15 kHz) until the crystal oscillation circuit (XOSC) starts up. The transition from the RC oscillation circuit to the crystal oscillation circuit is performed automatically inside	–
9	Approximately 2 s (typ.) is required after reset cancel until the crystal oscillation circuit starts up and the clock is output to CXD5602 (output from the CLK_OUT pin).	–

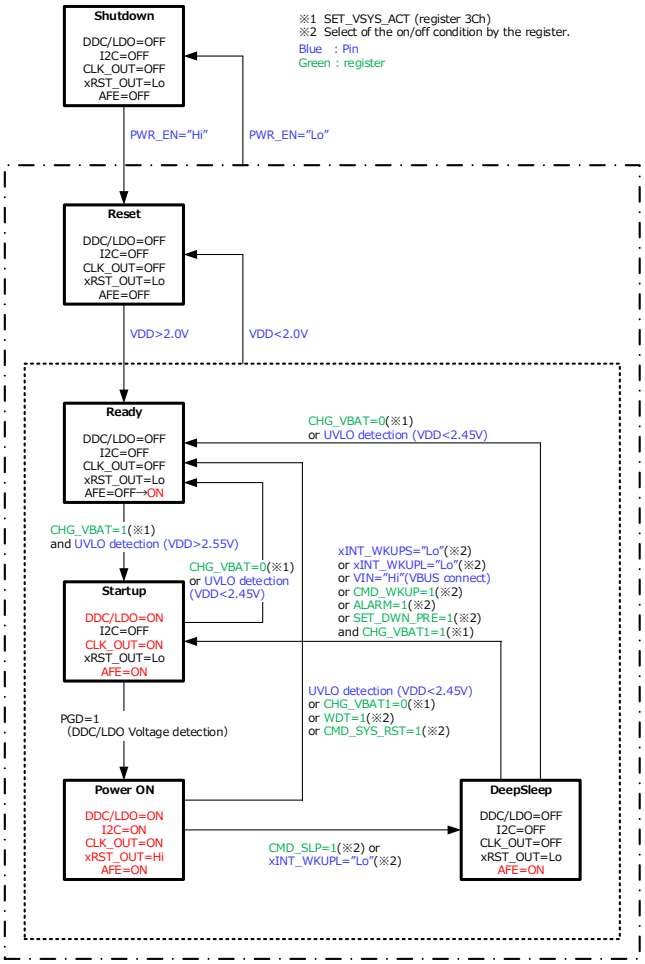
Deep Sleep（xINT_WKUP）～ Power ON



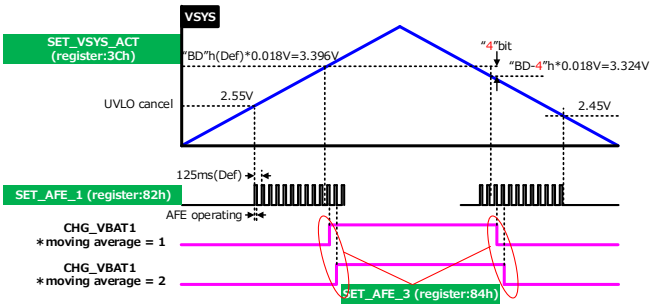
Deep Sleep ～ USB ON～ USB OFF



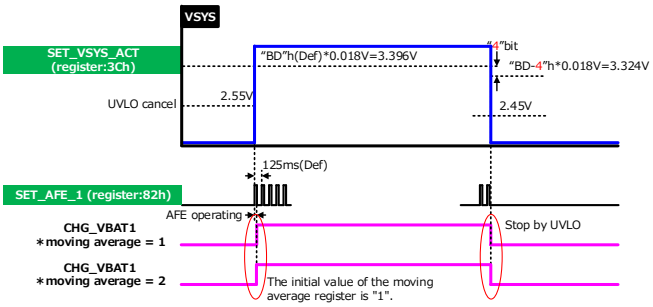
◆Power supply block state transition diagram



Timing chart of CHG_BAT1 (Case the voltage of VSYS rises slowly)

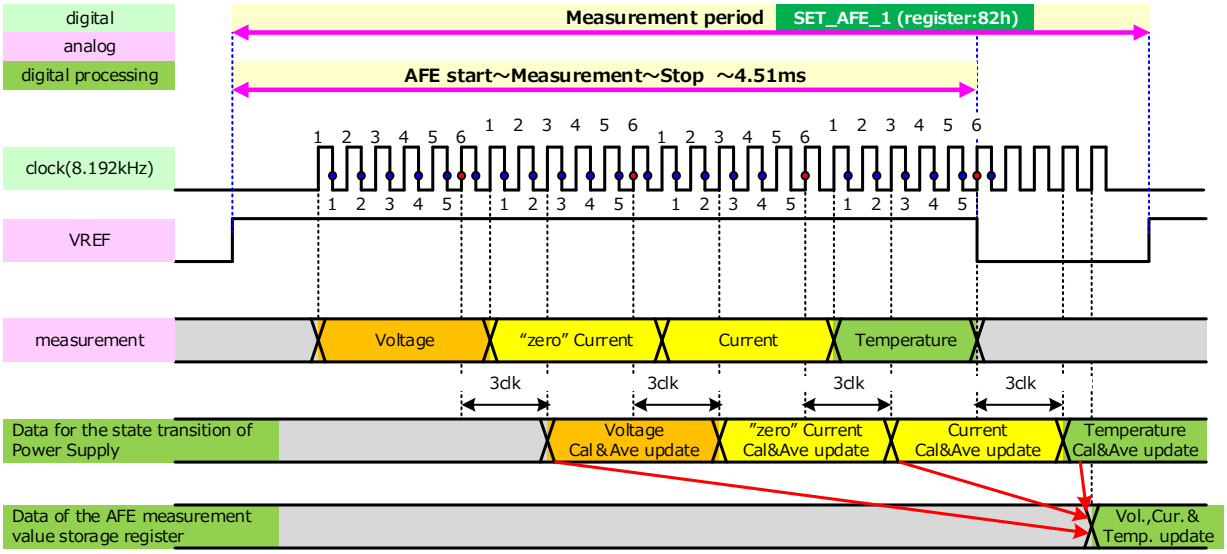


Timing chart of CHG_BAT1 (Case the voltage of VSYS rises quickly)

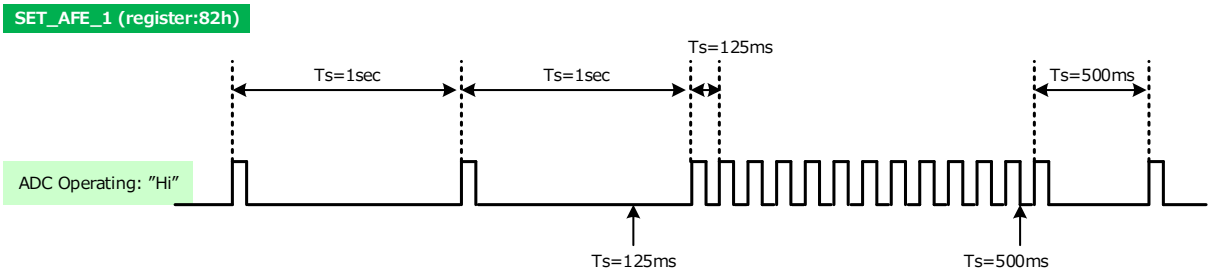


◆AFE block operation timing chart for battery power level detection

Timing chart of AFE operation



Timing chart (During the measurement cycle change)



Battery information measurement value read

The measurement data is reflected to the AFE measurement value storage register (registers 85h to 8Ah and 8Dh to 8Eh) by setting "1" in LRQ_AFE (register 8Bh). LRQ_AFED_STATE (register 8Ch) goes to "1" after the data is reflected.
The moving average values set by SET_AFE3 (register 84h[1:0]) are reflected to the storage registers.

- Battery voltage (DATA_AFEV1,2 register 85h,86h)

Battery voltage = Register value ×1.12mV Ex. : C85h×1.12mV=3.6V

- Battery charge/discharge current (DATA_AFEI1,2 register 87h,88h)

Battery charge/discharge current = (Register value - 800h) ÷ Current detection resistor ×0.02929 Ex. : (6ABh-800h) ÷0.1Ω×0.02929= - 100mA

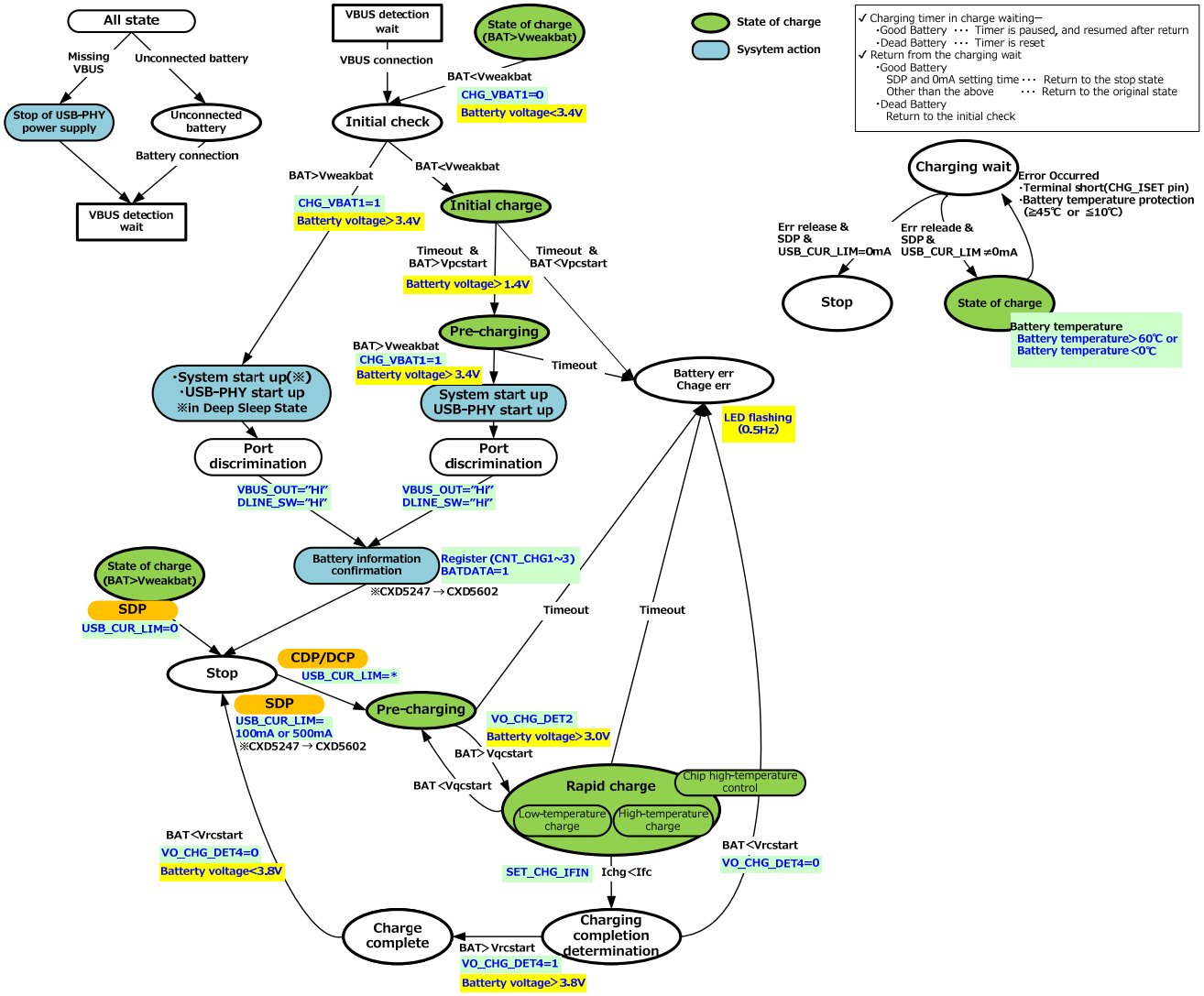
* "−" is the discharge direction and "+" is the charge direction.

- Battery temperature (DATA_AFET1,2 register 89h,8Ah)

Battery temperature (thermistor voltage) = Register value ×0.4883mV Ex.: 712h×0.4883mV=0.884V

* The temperature is determined according to the thermistor resistor (B constant) and the measurement value. When the B constant is B4250K, 0.884 V corresponds to a battery temperature of 30°C.

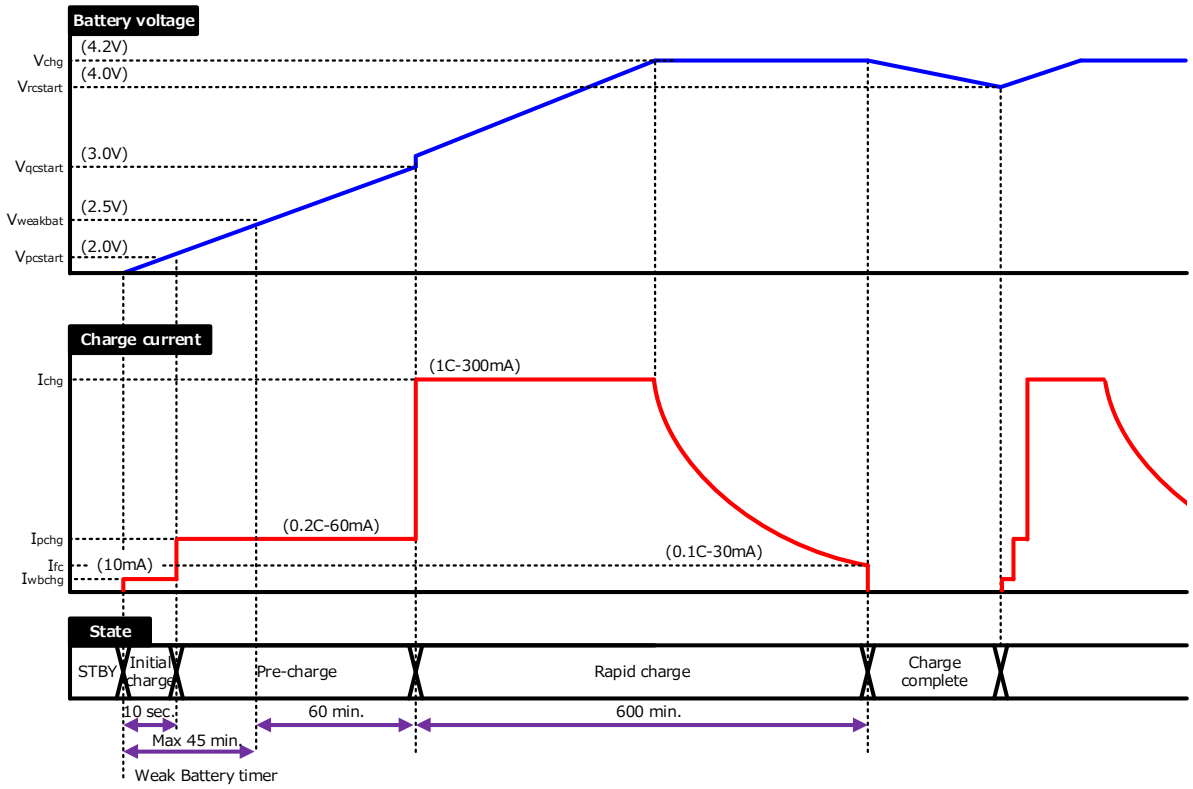
◆Charge control block state transition diagram



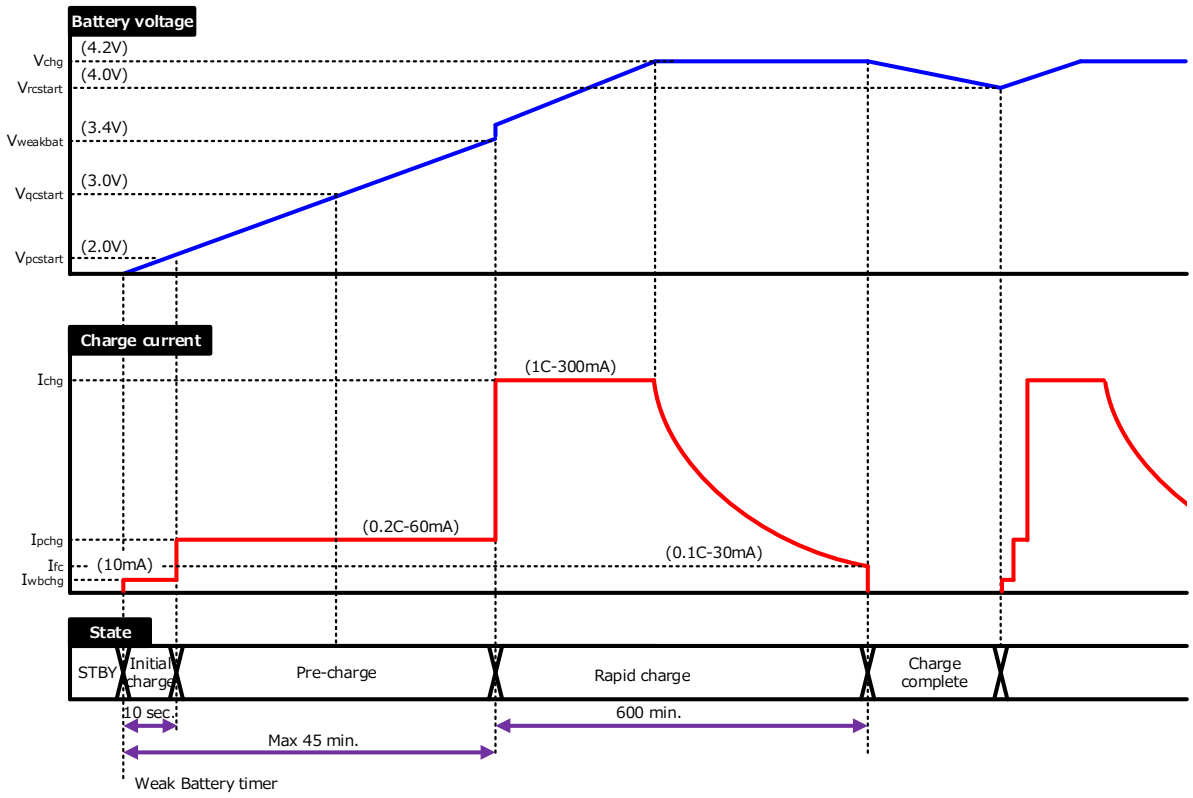
◆Charge control block operation timing

Charge timing chart

Vqcstart > Vweakbat



Vqcstart < Vweakbat



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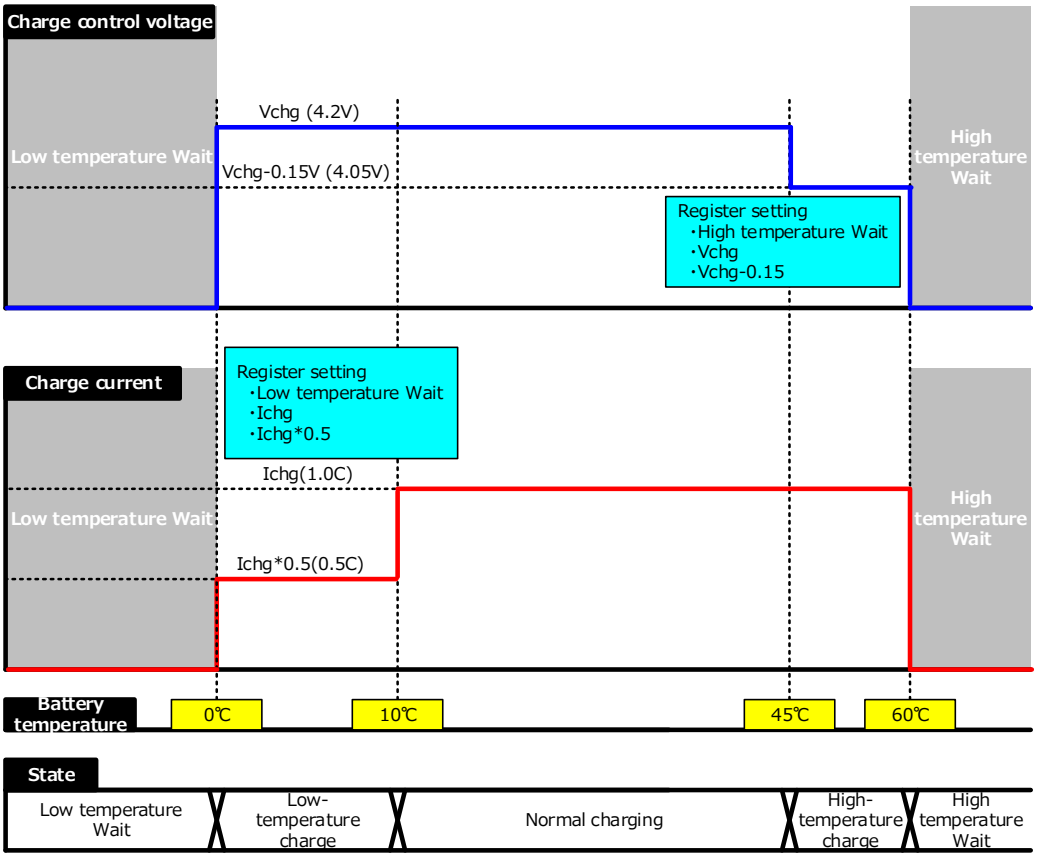
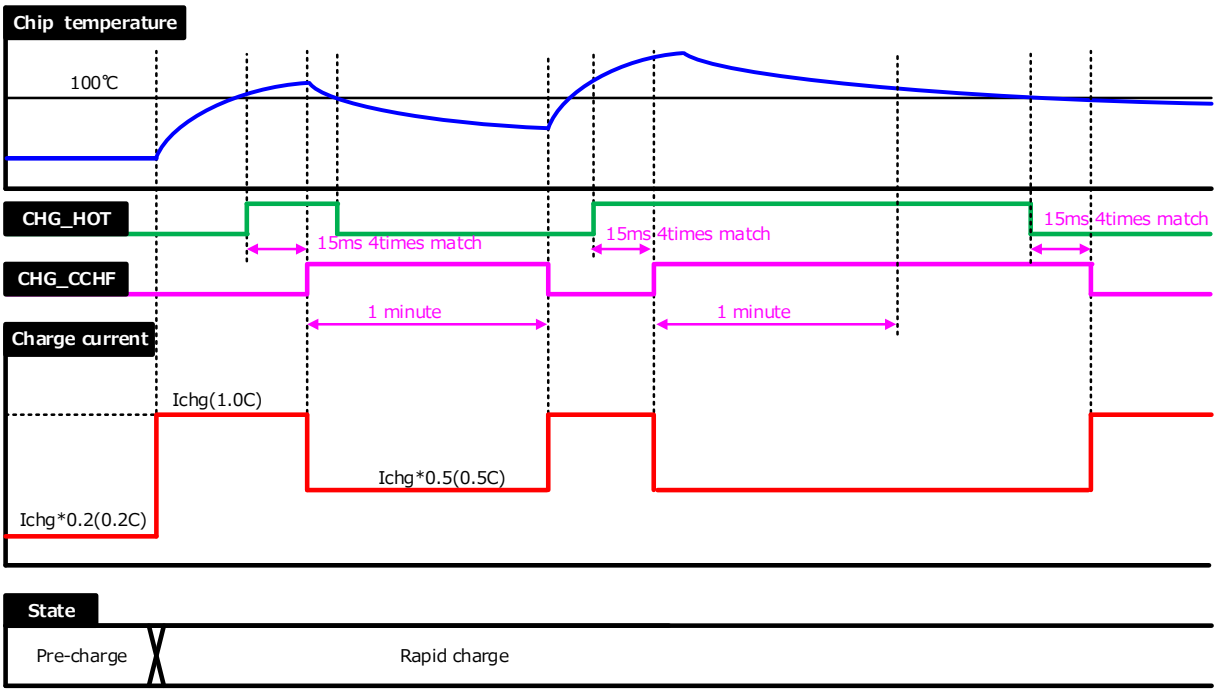
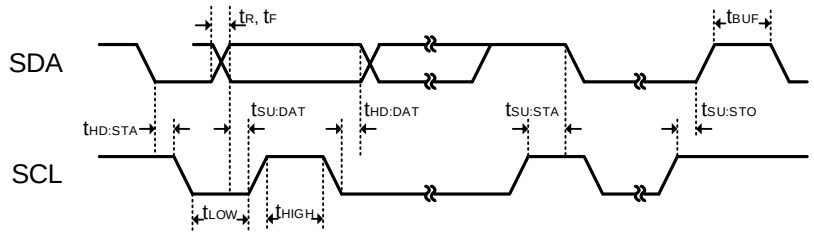


The control by the chip temperature in during Charge



◆Power block – I2C specifications

Symbol	Item	Min.	Max.	Unit
f_{SCL_P}	SCL_P clock frequency	0	400	kHz
$t_{HD:STA}$	Hold time (repeat) start condition (The first clock pulse is generated after this period.)	0.6	-	us
t_{LOW}	SCL_P clock Low period	1.3	-	us
t_{HIGH}	SCL_P clock High period	0.6	-	us
$t_{SU:STA}$	Repeat start condition setup time	0.6	-	us
$t_{HD:DAT}$	Data hold time	0	-	us
$t_{SU:DAT}$	Data setup time	100	-	ns
tr	SDA_P signal and SCL_P signal rise time	-	300	ns
tf	SDA_P signal and SCL_P signal fall time	-	300	ns
$t_{SU:STO}$	Stop condition setup time	0.6	-	us
t_{BUF}	Bus free time between Stop and Start conditions	1.3	-	us
Cb	Capacitance load of each bus line	-	400	pF



Write mode

S	Slave Address	W	A	Sub Address	A	Data	A	P

Read mode

S	Slave Address	W	A	Sub Address	A	SR	Slave Address	R	A	Data	N	P

symbol	description	bit
S	Start Condition	-
SR	Repeat Start Condition	-
P	Stop Condition	-
Slave Address	7'h2C	7
W	Write mode (Host→CXD5247)	1
R	Read mode(CXD5247→HOST)	1
A	ACK	1
N	NACK	1
Sub Address	Command Register	8
Data	Write/Read Data	8

◆Power register list

No.	Category	Address	Register name	Application
1	(Power supply block) Output control registers	10h	EN_CTRL1	D/D converter and LDO enable control
		11h	EN_CTRL2	
		12h	LOAD_SW_CTRL1	LOAD_SW enable control
		13h	GPO_CTRL1	GPO0～7 Output control
		14h	GPO_CTRL2	
		15h	VO_DDC_ANA	Sets the DDC_ANA output voltage
		16h	VO_DDC_CORE	Sets the DDC_CORE output voltage
		17h	VO_LDO_EMMC/PERI	Sets the LDO_EMMC/PERI output voltage
		18h	VO_LDO_ANA	Sets the LDO_ANA output voltage
2	(Power supply block) Power supply operating mode setting registers	20h	CONFIG_DDC_IO_1	Sets the DDC_IO operating mode
		21h	CONFIG_DDC_IO_2	
		22h	CONFIG_DDC_IO_3	
		23h	CONFIG_DDC_CORE_1	Sets the DDC_CORE operating mode
		24h	CONFIG_DDC_CORE_2	
		25h	CONFIG_DDC_CORE_3	
		26h	CONFIG_DDC_ANA_1	Sets the DDC_ANA operating mode
		27h	CONFIG_DDC_ANA_2	
		28h	CONFIG_DDC_ANA_3	
		29h	CONFIG_LDO	Sets the LDO operating mode
3	(Power supply block) Status control registers	30h	WKUP_STATUS	Stores the start-up factor
		31h	WKUP_STATUS_CLR	Clears the start-up factor_STATUS
		32h	WKUP_TRG	Stores the start-up factor output trigger
		33h	WKUP_TRG_CLR	Clears the start-up factor output trigger
		34h	INTO_STATUS	Stores the INT_OUT output trigger
		35h	INTO_STATUS_CLR	Clears the INT_OUT output trigger
		36h	VMIN_DDC_CORE	Holds the setting voltage before WDT issues
		37h	CMD_CTRL	Stores the I2C control command
		38h	CONFIG_INT_WKUP	Sets the xINT_WKUP condition
		39h	CONFIG_WDT	WDT setting
		3Ah	SET_DWN_PRE1	System operation lower limit voltage pre-notification voltage setting status
		3Bh	SET_DWN_PRE2	
		3Ch	SET_VSYS_ACT	Sets the system operating voltage
		3Dh	LRQ_SET_VSYS	Reflects the 3Ah to 3Ch settings
		3Eh	LRQ_VSYS_STATE	VSYS setting status

No.	Category	Address	Register name	Application
		3Fh	INT_SEL	Selects the INT_OUT output
4	(Power supply block) RTC control registers	40h	CURT_PRE_CNTR_1	Stores the current time
		41h	CURT_PRE_CNTR_2	
		42h	CURT_POST_CNTR_1	
		43h	CURT_POST_CNTR_2	
		44h	CURT_POST_CNTR_3	
		45h	CURT_POST_CNTR_4	
		46h	RRQ_TIME	Current time read request
4	(Power supply block) RTC control registers 1	47h	SET_PRE_CNTR_1	Stores the set time to the counter
		48h	SET_PRE_CNTR_2	
		49h	SET_POST_CNTR_1	
		4Ah	SET_POST_CNTR_2	
		4Bh	SET_POST_CNTR_3	
		4Ch	SET_POST_CNTR_4	
		4Dh	LRQ_TIME	Set time load request to the counter
		4Eh	LRQ_OFST	Reflects the offset time
		4Fh	WKUP_PRE_CNTR_1	Sets the WakeUp time (absolute time, relative time)
		50h	WKUP_PRE_CNTR_2	
		51h	WKUP_POST_CNTR_1	
		52h	WKUP_POST_CNTR_2	
		53h	WKUP_POST_CNTR_3	
		54h	WKUP_POST_CNTR_4	
		55h	LRQ_WU	Reflects the WakeUp time registers
		56h	CONFIG_WKUP	Condition settings of WakeUp
		57h	CNTR_STOP	Enable control of RTC counter
5	(Power supply block) RTC control registers 2	58h	ALM_PRE_CNTR_1	Sets the interrupt output alarm time (absolute time, relative time)
		59h	ALM_PRE_CNTR_2	
		5Ah	ALM_POST_CNTR_1	
		5Bh	ALM_POST_CNTR_2	
		5Ch	ALM_POST_CNTR_3	
		5Dh	ALM_POST_CNTR_4	
		5Eh	LRQ_ALM	Reflects the interrupt output alarm time setting registers
		5Fh	CONFIG_ALARM	Sets the alarm condition
		60h	RRQ_LRQ_STATUS	Time data status
6	(Power supply block) Information storage registers	61h	DATA_GPS1	Stores the GPS data
		62h	DATA_GPS2	
		63h	DATA_GPS3	

No.	Category	Address	Register name	Application
		64h	DATA_GPS4	
		65h	DATA_GPS5	
		66h	DATA_GPS6	
		67h	DATA_GPS7	
		68h	DATA_GPS8	
		69h	DATA_GPS9	
		6Ah	DATA_GPS10	
		6Bh	DATA_GPS11	
		6Ch	DATA_GPS12	
		6Dh	DATA_GPS13	
		6Eh	DATA_GPS14	
		6Fh	DATA_GPS15	
		70h	DATA_GPS16	
		71h	DATA_FREE1	Stores the information required by the software side
		72h	DATA_FREE2	
		73h	DATA_FREE3	
		74h	DATA_FREE4	
7	(Charge block) Control registers	75h	CNT_CHG1	Battery voltage judgment and control registers
		76h	CNT_CHG2	
		77h	CNT_CHG3	
		78h	SET_T60_1	Battery temperature control registers
		79h	SET_T60_2	
		7Ah	SET_T45_1	
		7Bh	SET_T45_2	
		7Ch	SET_T10_1	
		7Dh	SET_T10_2	
		7Eh	SET_T0_1	
		7Fh	SET_T0_2	
		80h	CNT_USB1	USB charge control registers
		81h	CNT_USB2	
8	(AFE block) Control registers	82h	SET_AFE1	AFE operation setting registers
		83h	SET_AFE2	
		84h	SET_AFE3	
		85h	DATA_AFEV_1	Stores the AFE measurement data
		86h	DATA_AFEV_2	
		87h	DATA_AFEI_1	
		88h	DATA_AFEI_2	

No.	Category	Address	Register name	Application
		89h	DATA_AFET_1	
		8Ah	DATA_AFET_2	
		8Bh	LRQ_AFE	Reflects the AFE measurement data to the registers
		8Ch	LRQ_AFED_STATE	AFE data status

* Note that addresses 8Dh and higher are assigned as test registers, and should not be used.

Output control registers

EN_CTRL1

Address	bit	Access	Name	Default	Description		Clear State
10h	7	R/W	-	0	Reserved		Ready&DeepSleep
	6	R/W	-	0	Reserved		Ready&DeepSleep
	5	R/W	EN_L_PERI1	1	LDO_PERI enable control	0:disable, 1:enable	Ready&DeepSleep
	4	R/W	EN_D_CORE1	1	DDC_CORE enable control	0:disable, 1:enable	Ready&DeepSleep
	3	R/W	EN_L_ANA1	1	LDO_ANA enable control	0:disable, 1:enable	Ready&DeepSleep
	2	R/W	EN_D_ANA1	1	DDC_ANA enable control	0:disable, 1:enable	Ready&DeepSleep
	1	R/W	EN_L_EMMC1	1	LDO_EMMC enable control	0:disable, 1:enable	Ready&DeepSleep
	0	R/W	EN_D_IO1	1	DDC_IO enable control	0:disable, 1:enable	Ready&DeepSleep

EN_CTRL2

Address	bit	Access	Name	Default	Description		Clear State
11h	0	R/W	EN_USBPHY	1	Power control for USB-PHY	0:disable, 1:enable	Ready&DeepSleep

* Effective at the time of USB connection. (LDO_USB33, LDO_USB10, SW_18_OUT1)

LOAD_SW_CTRL1

Address	bit	Access	Name	Default	Description		Clear State
12h	7	R/W	-	0	Reserved		Ready&DeepSleep
	6	R/W	-	0	Reserved		Ready&DeepSleep
	5	R/W	-	0	Reserved		Ready&DeepSleep
	4	R/W	EN_SW18_4	1	SW_18_OUT4 enable control	0:open, 1:short	Ready&DeepSleep
	3	R/W	EN_SW18_3	1	SW_18_OUT3 enable control	0:open, 1:short	Ready&DeepSleep
	2	R/W	EN_SW18_2	1	SW_18_OUT2 enable control	0:open, 1:short	Ready&DeepSleep
	1	R/W	-	1	Reserved		Ready&DeepSleep
	0	R/W	-	1	Reserved		Ready&DeepSleep

GPO_CTRL1

Address	bit	Access	Name	Default	Description		Clear State
13h	7	R/W	GPO[3]_EN	0	GPO3 output control	0:Hi-Z, 1:GPO[3] reflection	Reset
	6	R/W	GPO[2]_EN	0	GPO2 output control	0:Hi-Z, 1:GPO[2] reflection	Reset
	5	R/W	GPO[1]_EN	0	GPO1 output control	0:Hi-Z, 1:GPO[1] reflection	Reset
	4	R/W	GPO[0]_EN	0	GPO0 output control	0:Hi-Z, 1:GPO[0] reflection	Reset
	3	R/W	GPO[3]	0	GPO3 logic	0:Low output, 1:High output	Reset
	2	R/W	GPO[2]	0	GPO2 logic	0:Low output, 1:High output	Reset
	1	R/W	GPO[1]	0	GPO1 logic	0:Low output, 1:High output	Reset
	0	R/W	GPO[0]	0	GPO0 logic	0:Low output, 1:High output	Reset

GPO_CTRL2

Address	bit	Access	Name	Default	Description		Clear State
14h	7	R/W	GPO[7]_EN	0	GPO7 output control	0:Hi-Z, 1:GPO[7] reflection	Reset
	6	R/W	GPO[6]_EN	0	GPO6 output control	0:Hi-Z, 1:GPO[6] reflection	Reset
	5	R/W	GPO[5]_EN	0	GPO5 output control	0:Hi-Z, 1:GPO[5] reflection	Reset
	4	R/W	GPO[4]_EN	0	GPO4 output control	0:Hi-Z, 1:GPO[4] reflection	Reset
	3	R/W	GPO[7]	0	GPO7 logic	0:Low output, 1:High output	Reset
	2	R/W	GPO[6]	0	GPO6 logic	0:Low output, 1:High output	Reset
	1	R/W	GPO[5]	0	GPO5 logic	0:Low output, 1:High output	Reset
	0	R/W	GPO[4]	0	GPO4 logic	0:Low output, 1:High output	Reset

VO_DDC_ANA

Address	bit	Access	Name	Default	Description	Clear State
15h	5:0	R/W	VO_D_ANA[5:0]	1Ch	Output voltage setting register at PowerON. The setting voltage and the cord refer to table 1	Ready&DeepSleep

VO_DDC_CORE

Address	Bit	Access	Name	Default	Description	Clear State
16h	5:0	R/W	VO_D_CORE[5:0]	24h	Output voltage setting register at PowerON. The setting voltage and the cord refer to table 1	Ready&DeepSleep

VO_LDO_EMMC/PERI

Address	Bit	Access	Name	Default	Description	Clear State
17h	7:4	R/W	VO_L_PERI[3:0]	00h	Output voltage setting register at PowerON. The setting voltage and the cord refer to table 1	Ready&DeepSleep
	3:0	R/W	VO_L_EMMC[3:0]	00h	Output voltage setting register at PowerON. The setting voltage and the cord refer to table 1	Ready&DeepSleep

VO_LDO_ANA

Address	Bit	Access	Name	Default	Description	Clear State
18h	5:0	R/W	VO_L_ANA[5:0]	0Ch	Output voltage setting register at PowerON. The setting voltage and the cord refer to table 1	Ready&DeepSleep

Table.1

Setting voltage of each power supply and code Unit[V]

Address	DDC_ANA	DDC_CORE	LDO_ANA	LDO_EMMC	LDO_PERI
00h		0.55		3.3	3.3
01h		0.5625		3.2	3.2
02h		0.575		3.1	3.1
03h		0.5875		3.0	3.0
04h	0.6	0.6	0.6	2.9	2.9
05h	0.6125	0.6125	0.6	2.8	2.8
06h	0.625	0.625	0.625	2.7	2.7
07h	0.6375	0.6375	0.625	2.6	2.6
08h	0.65	0.65	0.65	2.5	2.5
09h	0.6625	0.6625	0.65	2.4	2.4
0Ah	0.675	0.675	0.675	2.3	2.3
0Bh	0.6875	0.6875	0.675	2.2	2.2
0Ch	0.7	0.7	0.7	2.1	2.1
0Dh	0.7125	0.7125	0.7	2.0	2.0
0Eh	0.725	0.725	0.725	1.9	1.9
0Fh	0.7375	0.7375	0.725	1.8	1.8
10h	0.75	0.75	0.75		
11h	0.7625	0.7625	0.75		
12h	0.775	0.775	0.775		
13h	0.7875	0.7875	0.775		
14h	0.8	0.8	0.8		
15h	0.8125	0.8125	0.8		
16h	0.825	0.825	0.825		
17h	0.8375	0.8375	0.825		
18h	0.85	0.85	0.85		
19h	0.8625	0.8625	0.85		
1Ah	0.875	0.875	0.875		
1Bh	0.8875	0.8875	0.875		
1Ch	0.9	0.9	0.9		
1Dh	0.9125	0.9125	0.9		
1Eh	0.925	0.925	0.925		
1Fh	0.9375	0.9375	0.925		
20h	0.95	0.95	0.95		
21h	0.9625	0.9625	0.95		
22h	0.975	0.975	0.975		
23h	0.9875	0.9875	0.975		
24h	1.0	1.0	1.0		

Unit[V]

Address	DDC_ANA	DDC_CORE
25h	1.0125	1.0125
26h	1.025	1.025
27h	1.0375	1.0375
28h	1.05	1.05
29h	1.0625	1.0625
2Ah	1.075	1.075
2Bh	1.0875	1.0875
2Ch	1.1	1.1
2Dh	1.1125	1.1125
2Eh	1.125	
2Fh	1.1375	
30h	1.15	
31h	1.1625	
32h	1.175	
33h	1.1875	
34h	1.2	
35h	1.2125	
36h	1.225	
37h	1.2375	
38h	1.25	
39h	1.2625	
3Ah	1.275	

* Blue cell values cannot be set (input).
* Yellow cell values are the default settings

Power supply operating mode setting registers

CONFIG_DDC_IO_1

Address	bit	Access	Name	Default	Description	Clear State
20h	5:4	R/W	PM_D_IO[1:0]	00b	Output setting register at disable 00b:10kohm, 01b:3.10kohm, 10b:Hi-z, 11b:3.6Mohm	Reset
	3:2	R/W	IOST_D_IO[1:0]	10b	Maximum output current setting at the time of start 00b:x0.5, 01b:x0.67, 10b:x1.0	Reset
	1:0	R/W	IOMAX_D_IO[1:0]	10b	Maximum output current setting 00b:x0.5, 01b:x0.67, 10b: x1.0	Reset

*PM_D_IO : Setting register to remove an electric charge from output capacity at the time of a power supply output stop

*IOST_D_IO : When the rush electric current which is at the time of a CXD5247GF start is a problem, please establish it. But, please pay attention to be connected with the starting time.

*IOMAX_D_IO : When there is fear of noise mainly, it's established. But, please pay attention to the maximum loading capacity's falling. (200mA to 100mA@x0.5)

CONFIG_DDC_IO_2

Address	bit	Access	Name	Default	Description	Clear State
21h	7	R/W	NDRVOFF_D_IO	0	Pre-driver OFF ability setting for output Low side-SW 0:x1.0, 1:x0.75	Reset
	6	R/W	PDRVOFF_D_IO	0	Pre-driver OFF ability setting for output High side-SW 0:x1.0, 1:x0.75	Reset
	5:4	R/W	NDRVON_D_IO[1:0]	10b	Pre-driver ON ability setting for output Low side-SW 00b:x0.5, 01b:x0.75, 10b:x1.0, 11b:x1.25	Reset
	3:2	R/W	PDRVON_D_IO[1:0]	10b	Pre-driver ON ability setting for output High side-SW 00b:x0.5, 01b:x0.75, 10b:x1.0, 11b:x1.25	Reset
	1:0	R/W	DT_D_IO[1:0]	10b	Output dead time setting 00b:5ns, 01b:10ns 10b:15ns, 11b:25ns	Reset

*21h[7:2] : When noise of a DDC is a problem, it's established (It's set as the minus side.) The effect can be expected by the order of the A [5:4] >= [3:2] >> [7] >= [6]. But, for the performance as the DDC to become the deterioration direction, a change judgment of pros and cons is recommended with a set evaluation result.

*DT_D_IO : This register is used to slight adjustment of the electric power change efficiency. When it's short, it'll be the way of the efficient good, but when it passes the optimum point, please be careful about deteriorating.

CONFIG_DDC_IO_3

Address	Bit	Access	Name	Default	Description	Clear State
22h	1:0	R/W	ZCD_D_IO[1:0]	10b	ZCD detection threshold value setting 00b:x0.88, 01b:x0.94, 10b:x1.0, 11b:x1.06	Reset

*ZCD_D_IO : This register is used to slight adjustment of the electric power change efficiency.

CONFIG_DDC_CORE_1

Address	bit	Access	Name	Default	Description	Clear State
23h	5:4	R/W	PM_D_CORE[1:0]	00b	Output setting register at disable 00b:10kohm, 01b:10kohm, 10b:Hi-z, 11b:220ohm	Reset
	3:2	R/W	IOST_D_CORE[1:0]	10b	Maximum output current setting at the time of start 00b:x0.5, 01b:x0.67, 10b:x1.0, 11b:Reserved	Reset
	1:0	R/W	IOMAX_D_CORE[1:0]	10b	Maximum output current setting 00b:x0.5, 01b:x0.67, 10b:x1.0, 11b:Reserved	Reset

*PM_D_CORE : Setting register to remove an electric charge from output capacity at the time of a power supply output stop

*The time of Power ON can also move only 11b in 23h [5:4]. When changing the DDC_CORE voltage, when also making them reach the setting voltage by a short time in untensioned, it's established. (1.0V→0.7V)

*IOST_D_CORE : When the rush electric current which is at the time of a CXD5247GF start is a problem, please establish it. But, please pay attention to be connected with the starting time.

*IOMAX_D_CORE : When there is fear of noise mainly, it's established. But, please pay attention to the maximum loading capacity's falling.(100mA to 50mA@x0.5)

CONFIG_DDC_ CORE _2

Address	bit	Access	Name	Default	Description	Clear State
24h	7	R/W	NDRVOFF_D_CORE	0	Pre-driver OFF ability setting for output Low side-SW 0:x1.0, 1:x0.75	Reset
	6	R/W	PDRVOFF_D_CORE	0	Pre-driver OFF ability setting for output High side-SW 0:x1.0, 1:x0.75	Reset
	5:4	R/W	NDRVON_D_CORE[1:0]	10b	Pre-driver ON ability setting for output Low side-SW 00b:x0.5, 01b:x0.75, 10b:x1.0, 11b:x1.25	Reset
	3:2	R/W	PDRVON_D_CORE[1:0]	10b	Pre-driver ON ability setting for output High side-SW 00b:x0.5, 01b:x0.75, 10b:x1.0, 11b:x1.25	Reset
	1:0	R/W	DT_D_CORE[1:0]	10b	Output dead time setting 00b:5ns, 01b:10ns 10b:15ns, 11b:25ns	Reset

*24h[7:2] : When noise of a DDC is a problem, it's established (It's set as the minus side.) The effect can be expected by the order of the A [5:4] >= [3:2] >> [7] >= [6]. But, for the performance as the DDC to become the deterioration direction, a change judgment of pros and cons is recommended with a set evaluation result.

*DT_D_IO : This register is used to slight adjustment of the electric power change efficiency. When it's short, it'll be the way of the efficient good, but when it passes the optimum point, please be careful about deteriorating.

CONFIG_DDC_ CORE _3

Address	bit	Access	Name	Default	Description	Clear State
25h	1:0	R/W	ZCD_D_CORE[1:0]	10b	ZCD detection threshold value setting 00b:x0.88, 01b:x0.94, 10b:x1.0, 11b:x1.06	Reset

*ZCD_D_CORE : This register is used to slight adjustment of the electric power change efficiency.

CONFIG_DDC_ANA_1

Address	bit	Access	Name	Default	Description	Clear State
26h	5:4	R/W	PM_D_ANA[1:0]	00b	Output setting register at disable 00b:10kohm, 01b:10kohm, 10b:Hi-z, 11b:3.6Mohm	Reset
	3:2	R/W	IOST_D_ANA[1:0]	10b	Maximum output current setting at the time of start 00b:x0.5, 01b:x0.67, 10b:x1.0, 11b:Reserved	Reset
	1:0	R/W	IOMAX_D_ANA[1:0]	10b	Maximum output current setting 00b:x0.5, 01b:x0.67, 10b:x1.0, 11b:Reserved	Reset

*PM_D_ANA : Setting register to remove an electric charge from output capacity at the time of a power supply output stop

*IOST_D_ANA : When the rush electric current which is at the time of a CXD5247GF start is a problem, please establish it. But, please pay attention to be connected with the starting time.

*IOMAX_D_ANA : When there is fear of noise mainly, it's established. But, please pay attention to the maximum loading capacity's falling.(10mA to 5mA@x0.5)

CONFIG_DDC_ ANA _2

Address	bit	Access	Name	Default	Description	Clear State
27h	7	R/W	NDRVOFF_D_ANA	0	Pre-driver OFF ability setting for output Low side-SW 0:x1.0, 1:x0.75	Reset
	6	R/W	PDRVOFF_D_ANA	0	Pre-driver OFF ability setting for output High side-SW 0:x1.0, 1:x0.75	Reset
	5:4	R/W	NDRVON_D_ANA[1:0]	10b	Pre-driver ON ability setting for output Low side-SW 00b:x0.5, 01b:x0.75, 10b:x1.0, 11b:x1.25	Reset
	3:2	R/W	PDRVON_D_ANA[1:0]	10b	Pre-driver ON ability setting for output High side-SW 00b:x0.5, 01b:x0.75, 10b:x1.0, 11b:x1.25	Reset
	1:0	R/W	DT_D_ANA[1:0]	10b	Output dead time setting 00b:5ns, 01b:10ns 10b:15ns, 11b:25ns	Reset

*27h[7:2] : When noise of a DDC is a problem, it's established (It's set as the minus side.) The effect can be expected by the order of the A [5:4] >= [3:2] >> [7] >= [6]. But, for the performance as the DDC to become the deterioration direction, a change judgment of pros and cons is recommended with a set evaluation result.

*DT_D_IO : This register is used to slight adjustment of the electric power change efficiency. When it's short, it'll be the way of the efficient good, but when it passes the optimum point, please be careful about deteriorating.

CONFIG_DDC_ ANA _3

Address	bit	Access	Name	Default	Description	Clear State
28h	1:0	R/W	ZCD_D_ANA[1:0]	10b	ZCD detection threshold value setting 00b:x0.88, 01b:x0.94, 10b:x1.0, 11b:x1.06	Reset

*ZCD_D_ANA : This register is used to slight adjustment of the electric power change efficiency.

CONFIG_LDO

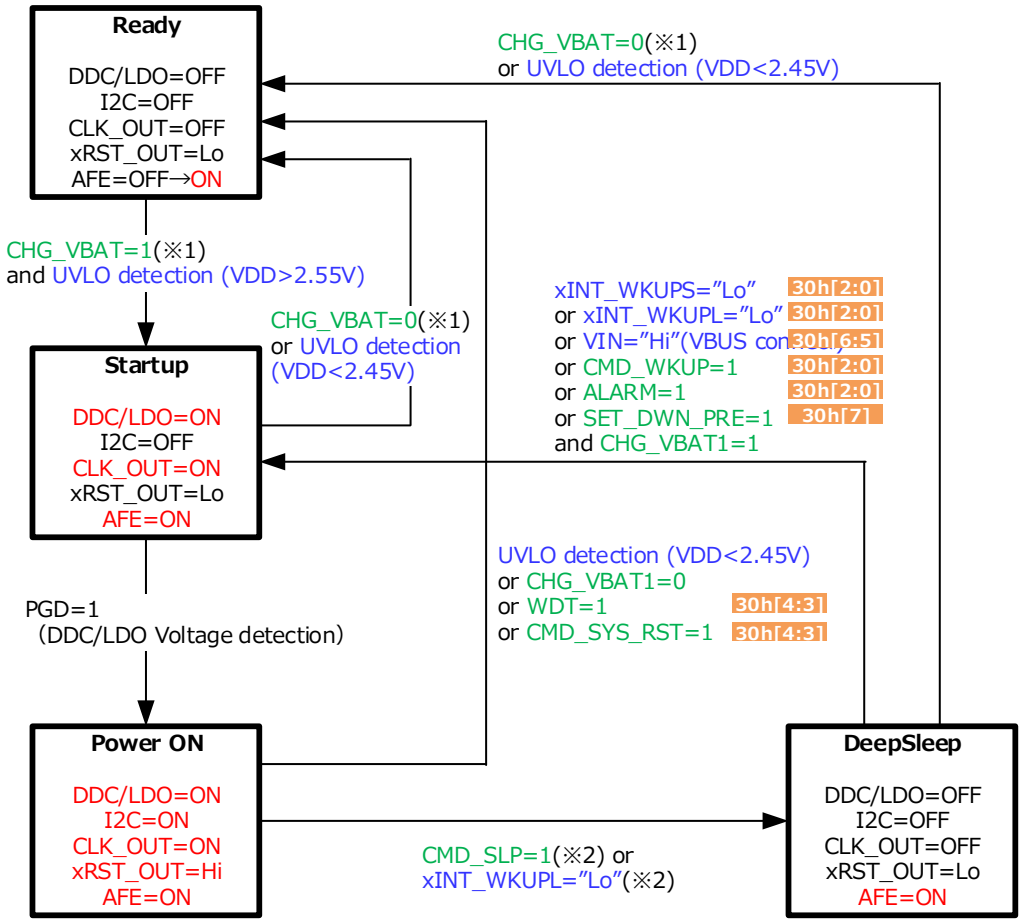
Address	bit	Access	Name	Default	Description	Clear State
29h	7:6	R/W	ZCONT_L_UPHY[1:0]	00b	LDO_USB10 00b:1Mohm, 01b:HiZ, 10b:1kohm,11b:1kohm LDO_USB33 00b:3.3Mohm, 01b:HiZ, 10b:1kohm,11b:1kohm	Reset
	5:4	R/W	ZCONT_L_PERI[1:0]	00b	LDO_PERI_OUT 00b:0.5Mohm, 01b:HiZ, 10b:1kohm,11b:1kohm	Reset
	3:2	R/W	ZCONT_L_ANA[1:0]	00b	LDO_ANA_OUT 00b:0.5Mohm, 01b:HiZ, 10b:1kohm,11b:1kohm	Reset
	1:0	R/W	ZCONT_L_EMMC[1:0]	00b	LDO_EMMC_OUT 00b:0.5Mohm, 01b:HiZ, 10b:1kohm,11b:1kohm	Reset

*ZCONT_L_* : Setting register to remove an electric charge from output capacity at the time of a power supply output stop

Status control registers

WKUP_STATUS (Return factor to “Power ON”)

Address	bit	Access	Name	Default	Description	Clear State
30h	7	R	VSYS_WKUP	0b	0:normal, 1:SET_DWN_PRE	Reset
	6:5	R	USB_WKUP[1:0]	00b	00b:normal, 01b:USB connect1(from Deep Sleep), 10b:USB connect2(from Dead Battery)	Reset
	4:3	R	RST_WKUP[1:0]	00b	00b:normal, 01b: CMD_SYS_RST, 10b:WDT	Reset
	2:0	R	NORMAL_WKUP[2:0]	000b	000b:normal, 001b:xINT_WKUPS pin “low”, 010b:xINT_WKUPL pin “low”, 011b:Alarm, 100b:CMD_WKUP, 101b:CMD_SLP[2:0]=001	Reset



WKUP_STATUS_CLR

Address	bit	Access	Name	Default	Description		Clear State
31h	3	R/W	VSYS_WKUP_CLR	0	Clear “VSYS_WKUP”	0:disable, 1:enable	Reset
	2	R/W	USB_WKUP_CLR	0	Clear “USB_WKUP[1:0]”	0:disable, 1:enable	Reset
	1	R/W	RST_WKUP_CLR	0	Clear “RST_WKUP[1:0]”	0:disable, 1:enable	Reset
	0	R/W	NORMAL_WKUP_CLR	0	Clear “NORMAL_WKUP[2:0]”	0:disable, 1:enable	Reset

*After having cleared “WKUP_STATU”, “0” is stored.

WKUP_TRG

Address	bit	Access	Name	Default	Description		Clear State
32h	6	R	TRG_VSYS_WKUP	0	SET_DWN_PRE signal	0:no signal, 1:signal	Reset
	5	R	TRG_USB2_WKUP	0	USB connect at Dead Battery	0:disconnect, 1:connect	Reset
	4	R	TRG_USB1_WKUP	0	USB connect at Good Battery	0:disconnect, 1:connect	Reset
	3	R	TRG_CMD_WKUP	0	CMD_WKUP signal	0:no signal, 1:signal	Reset
	2	R	TRG_ALARM_WKUP	0	Alarm signal	0:no signal, 1:signal	Reset
	1	R	TRG_INT_WKUPL	0	xINT_WKUPL pin	0:Hi , 1:Lo	Reset
	0	R	TRG_INT_WKUPS	0	xINT_WKUPS pin	0:Hi , 1:Lo	Reset

*Start factor maintenance register

WKUP_TRG_CLR

Address	bit	Access	Name	Default	Description		Clear State
33h	6	R/W	TRG_VSYS_WKUP_CLR	0	Clear “TRG_VSYS_WKUP”	0:disable, 1:enable	Reset
	5	R/W	TRG_USB2_WKUP_CLR	0	Clear “TRG_USB2_WKUP”	0:disable, 1:enable	Reset
	4	R/W	TRG_USB1_WKUP_CLR	0	Clear “TRG_USB1_WKUP”	0:disable, 1:enable	Reset
	3	R/W	TRG_CMD_WKUP_CLR	0	Clear “TRG_CMD_WKUP”	0:disable, 1:enable	Reset
	2	R/W	TRG_ALARM_WKUP_CLR	0	Clear “TRG_ALARM_WKUP”	0:disable, 1:enable	Reset
	1	R/W	TRG_INT_WKUPL_CLR	0	Clear “TRG_INT_WKUPL”	0:disable, 1:enable	Reset
	0	R/W	TRG_INT_WKUPS_CLR	0	Clear “TRG_INT_WKUPS”	0:disable, 1:enable	Reset

*After having cleared “WKUP_TRG”, “0” is stored.

INTO_STATUS

Address	bit	Access	Name	Default	Description		Clear State
34h	3	R	REG_VSYS_INTO	0	SET_DWN_PRE signal	0:no signal, 1:signal	Reset
	2	R	REG_WKUPL_INTO	0	xINT_WKUPL pin	0:Hi , 1:Lo	Reset
	1	R	REG_WKUPS_INTO	0	xINT_WKUPS pin	0:Hi , 1:Lo	Reset
	0	R	REG_ALARM_INTO	0	Alarm signal	0:no signal, 1:signal	Reset

* “INT_OUT pin output” factor maintenance register

INTO_STATUS_CLR

Address	bit	Access	Name	Default	Description		Clear State
35h	3	R/W	REG_VSYS_INTO_CLR	0	Clear “REG_VSYS_INTO”	0:disable, 1:enable	Reset
	2	R/W	REG_WKUPL_INTO_CLR	0	Clear “REG_WKUPL_INTO”	0:disable, 1:enable	Reset
	1	R/W	REG_WKUPS_INTO_CLR	0	Clear “REG_WKUPS_INTO”	0:disable, 1:enable	Reset
	0	R/W	REG_ALARM_INTO_CLR	0	Clear “REG_ALARM_INTO”	0:disable, 1:enable	Reset

*After having cleared “INTO_STATUS”, “0” is stored.

VMIN_DDC_CORE

Address	bit	Access	Name	Default	Description	Clear State
36h	5:0	R	VMIN_D_CORE[5:0]	24h	The setting voltage before the WDT effect is maintained to this register. The setting voltage and the cord refer to Table 1.	Reset

CMD_CTRL

Address	Bit	Access	Name	Default	Description		Clear State
37h	6	R/W	CMD_WDT_RST[1]	0	WDT enable command	0:disable, 1:enable	Reset
	5	R/W	CMD_WDT_RST[0]	0	WDT reset command	0:disable, 1:enable	Reset
	4	R/W	CMD_SYS_RST	0	System reset command	0:disable, 1:enable	Reset
	3	R/W	CMD_WKUP	0	Return to “Power ON” command	0:disable, 1:enable	Reset
	2	R/W	CMD_SLP[2]	1	Return to “Power ON” by xINT_WKUP pin.	0:disable, 1:enable	Reset
	1	R/W	CMD_SLP[1]	1	Return to “Power ON” by Alarm WakeUp.	0:disable, 1:enable	Reset
	0	R/W	CMD_SLP[0]	0	Sleep command	0:disable, 1:enable	Reset

*1 In CMD_SLP [0], “0” is stored by moving to "Start Up" state.

*2 When CMD_SLP [2:0]=001 is set, the state automatically moves from “Deep Sleep” to “Power ON”.

*3 In CMD_WKUP, “0” is stored by moving to "Start Up" state.

*4 In CMD_SYS_RST, “0” is stored by moving to “Ready” state.

*5 In CMD_WDT_RST [0], "0" is stored by "reset to WDT" or "clear of WKUP_TRG".

CONFIG_INT_WKUP

Address	bit	Access	Name	Default	Description		Clear State
38h	1	R/W	SET_xINT_WKUPL	0	State transition of “Deep Sleep” and “Start UP”	0:disable, 1:enable	Reset
	0	R/W	MODE_xINT_WKUPS	0	Kind of the trigger of "the xINT_WKUPS pin"	0:level, 1:edge	Reset

*SET_xINT_WKUPL : The transition to "Deep Sleep" is effective only in "Power ON", the transition to "Start UP" is effective only in "Deep Sleep".

* As for the transition time by " xINT_WKUPL pin", it is fixed for three seconds.

CONFIG_WDT

Address	bit	Access	Name	Default	Description	Clear State
39h	7:4	R/W	INTVL_WDT[3:0]	0000b	Time-up time setting is higher	Reset
	3:0	R/W	PREC_WDT[3:0]	0000b	Time-up time setting is lower	Reset

SET_DWN_PRE1

Address	bit	Access	Name	Default	Description	Clear State
3Ah	7:0	R/W	DWN_PRE_DET1[7:0]	00h	Voltage setting register to notify of before system movement lower limit voltage (the LSB side: 7 - 0bit)	Reset

SET_DWN_PRE2

Address	bit	Access	Name	Default	Description	Clear State
3Bh	1:0	R/W	DWN_PRE_DET2[1:0]	03h	Voltage setting register to notify of before system movement lower limit voltage (the LSB side: 1 - 0bit)	Reset

*Automatically returning it to a "Power ON" state by the battery voltage drop in "Deep Sleep" state and outside notice (INT_OUT pin) are possible by setting 3A/3Bh.

*Setting of the voltage 4.492mV×“3A/3Bh” Default 4.492mV×“0300h”=3.45V

SET_VSYS_ACT

Address	Bit	Access	Name	Default	Description	Clear State
3Ch	7:0	R/W	SET_VSYS_DET[7:0]	BDh	System movement lower limit voltage (18mV*Data)	Reset

*SET_VSYS_ACT links CHG_VBAT1(judgment of Good/Dead Battery)

*Setting of the voltage 18mV×“3Ch” Default : 18mV×“BDh”=3.396V

*The setting in 3C is a value at the time of the rises in voltage. The hysteresis is 4bit fixation.

Default: a value at the time of the voltage drop 3.396V-72mV(18mV*4bit)=3.324V

LRQ_SET_VSYS

Address	Bit	Access	Name	Default	Description		Clear State
3Dh	1	R/W	LRQ_DWN_PRE	0	Setting SET_DWN_PRE(3A,3Bh)	0:disable, 1:enable	Reset
	0	R/W	LRQ_VSYS_ACT	0	Setting SET_VSYS_ACT(3Ch)	0:disable, 1:enable	Reset

LRQ_VSYS_STATE

Address	Bit	Access	Name	Default	Description		Clear State
3Eh	1	R	LRQ_DWN_STATE	0	Status of LRQ_DWN_PRE	0: Setting non-completion, 1: Setting completion	Reset
	0	R	LRQ_VSYS_STATE	0	Status of LRQ_VSYS_ACT	0: Setting non-completion, 1: Setting completion	Reset

LRQ_SET_VSYS

Address	Bit	Access	Name	Default	Description		Clear State
3Fh	4	R/W	SEL_INT_OUT	0	Output mode select of the INT_OUT pin	0:CMOS, 1:Hiz	Ready
	3	R/W	INT_SEL[3]	1	SYS_DWN_PRE[9:0]	0:disable, 1:enable	Reset
	2	R/W	INT_SEL[2]	1	xINT_WKUPS pin	0:disable, 1:enable	Reset
	1	R/W	INT_SEL[1]	1	xINT_WKUPL pin	0:disable, 1:enable	Reset
	0	R/W	INT_SEL[0]	1	Alarm	0:disable, 1:enable	Reset

RTC control registers 1

CURT_PRE_CNTR_1

Address	bit	Access	Name	Default	Description	Clear State
40h	7:0	R/W	CURT_PRE_1[7:0]	00h	Stores a "pre-counter value" from the LSB side.(7-0bit)	Reset

CURT_PRE_CNTR_2

Address	bit	Access	Name	Default	Description	Clear State
41h	6:0	R/W	CURT_PRE_2[6:0]	00h	Stores a "pre-counter value" from the LSB side.(14-8bit)	Reset

CURT_POST_CNTR_1

Address	bit	Access	Name	Default	Description	Clear State
42h	7:0	R/W	CURT_POST_1[7:0]	00h	Stores a "post-counter value" from the LSB side.(7-0bit)	Reset

CURT_POST_CNTR_2

Address	bit	Access	Name	Default	Description	Clear State
43h	7:0	R/W	CURT_POST_2[7:0]	00h	Stores a "post-counter value" from the LSB side.(15-8bit)	Reset

CURT_POST_CNTR_3

Address	bit	Access	Name	Default	Description	Clear State
44h	7:0	R/W	CURT_POST_3[7:0]	00h	Stores a "post-counter value" from the LSB side.(23-16bit)	Reset

CURT_POST_CNTR_4

Address	bit	Access	Name	Default	Description	Clear State
45h	7:0	R/W	CURT_POST_4[7:0]	00h	Stores a "post-counter value" from the LSB side.(31-24bit)	Reset

RRQ_TIME

Address	bit	Access	Name	Default	Description		Clear State
46h	0	R/W	RRQ_TIME	0	Hold request of the present time register	0:disable, 1:enable	Reset

* After stored the present time to a present time register, "0" is stored

SET_PRE_CNTR_1

Address	bit	Access	Name	Default	Description	Clear State
47h	7:0	R/W	SET_PRE_1[7:0]	00h	Stores a set value to the pre-counter from the LSB side (7-0bit)	Reset

SET_PRE_CNTR_2

Address	bit	Access	Name	Default	Description	Clear State
48h	6:0	R/W	SET_PRE_2[6:0]	00h	Stores a set value to the pre-counter from the LSB side (14-8bit)	Reset

SET_POST_CNTR_1

Address	bit	Access	Name	Default	Description	Clear State
49h	7:0	R/W	SET_POST_1[7:0]	00h	Stores a set value to the post-counter from the LSB side (7-0bit)	Reset

SET _POST_CNTR_2

Address	bit	Access	Name	Default	Description	Clear State
4Ah	7:0	R/W	SET_POST_2[7:0]	00h	Stores a set value to the post-counter from the LSB side (15-8bit)	Reset

SET _POST_CNTR_3

Address	bit	Access	Name	Default	Description	Clear State
4Bh	7:0	R/W	SET_POST_3[7:0]	00h	Stores a set value to the post-counter from the LSB side (23-16bit)	Reset

SET _POST_CNTR_4

Address	bit	Access	Name	Default	Description	Clear State
4Ch	7:0	R/W	SET_POST_4[7:0]	00h	Stores a set value to the post-counter from the LSB side (31-24bit)	Reset

LRQ_TIME

Address	bit	Access	Name	Default	Description		Clear State
4Dh	0	R/W	LRQ_TIME	0	Road request to the present time register of the time road register	0:disable, 1:enable	Reset

*After loaded a time load register value to a present time register, "0" is stored

LRQ_OFST

Address	bit	Access	Name	Default	Description		Clear State
4Eh	0	R/W	LRQ_OFST	0	Let reflect offset time	0:disable, 1:enable	Reset

*After reflect offset time, "0" is stored

WKUP_PRE_CNTR_1

Address	bit	Access	Name	Default	Description	Clear State
4Fh	7:0	R/W	WKUP_PRE_1[7:0]	00h	Stores an offset time for time revision to a pre-counter from the LSB side.(7-0bit)	Reset

WKUP_PRE_CNTR_2

Address	bit	Access	Name	Default	Description	Clear State
50h	6:0	R/W	WKUP_PRE_2[6:0]	00h	Stores an offset time for time revision to a pre-counter from the LSB side.(14-8bit)	Reset

WKUP_POST_CNTR_1

Address	bit	Access	Name	Default	Description	Clear State
51h	7:0	R/W	WKUP_POST_1[7:0]	00h	Stores an offset time for time revision to a post-counter from the LSB side.(7-0bit)	Reset

WKUP _POST_CNTR_2

Address	bit	Access	Name	Default	Description	Clear State
52h	7:0	R/W	WKUP_POST_2[7:0]	00h	Stores an offset time for time revision to a post-counter from the LSB side.(15-8bit)	Reset

WKUP _POST_CNTR_3

Address	bit	Access	Name	Default	Description	Clear State
53h	7:0	R/W	WKUP_POST_3[7:0]	00h	Stores an offset time for time revision to a post-counter from the LSB side.(23-16bit)	Reset

WKUP _POST_CNTR_4

Address	bit	Access	Name	Default	Description	Clear State
54h	7:0	R/W	WKUP_POST_4[7:0]	00h	Stores an offset time for time revision to a post-counter from the LSB side.(31-24bit)	Reset

LRQ_WU

Address	bit	Access	Name	Default	Description		Clear State
55h	0	R/W	LRQ_WU	0	Let reflect WakeUp time register and WakeUp condition setting register.	0:disable, 1:enable	Reset

*After reflect WakeUp time register, "0" is stored

CONFIG_WKUP

Address	bit	Access	Name	Default	Description		Clear State
56h	1	R/W	CONFIG_WKUP[1]	0	Repetition select in case of the relative time	0:Not Repeat, 1:Repeat	Reset
	0	R/W	CONFIG_WKUP[0]	0	Select of the WakeUp time	0:absolute time, 1:relative time	Reset

*Reflected at after writing in 1 to LRQ_WU

CNTR_STOP

Address	bit	Access	Name	Default	Description		Clear State
57h	0	R/W	CNTR_STOP	1	Clock enable of the RTC counter	0:disable, 1:enable	Reset

RTC control registers 2

ALM_PRE_CNTR_1

Address	bit	Access	Name	Default	Description	Clear State
58h	7:0	R/W	ALM_PRE_1[7:0]	00h	Stores a pre-counter value from the LSB side.(7-0bit)	Reset

ALM_PRE_CNTR_2

Address	bit	Access	Name	Default	Description	Clear State
59h	6:0	R/W	ALM_PRE_2[6:0]	00h	Stores a pre-counter value from the LSB side.(14-8bit)	Reset

ALM_POST_CNTR_1

Address	bit	Access	Name	Default	Description	Clear State
5Ah	7:0	R/W	ALM_POST_1[7:0]	00h	Stores a post-counter value from the LSB side.(7-0bit)	Reset

ALM_POST_CNTR_2

Address	bit	Access	Name	Default	Description	Clear State
5Bh	7:0	R/W	ALM_POST_2[7:0]	00h	Stores a post-counter value from the LSB side.(15-8bit)	Reset

ALM_POST_CNTR_3

Address	bit	Access	Name	Default	Description	Clear State
5Ch	7:0	R/W	ALM_POST_3[7:0]	00h	Stores a post-counter value from the LSB side.(23-16bit)	Reset

ALM_POST_CNTR_4

Address	bit	Access	Name	Default	Description	Clear State
5Dh	7:0	R/W	ALM_POST_4[7:0]	00h	Stores a post-counter value from the LSB side.(31-24bit)	Reset

LRQ_ALM

Address	bit	Access	Name	Default	Description		Clear State
5Eh	0	R/W	LRQ_ALM	0	Let reflect the interrupt output Alarm time register and Alarm condition setting register.	0:disable, 1:enable	Reset

*After reflect Alarm time setting register, "0" is stored.

CONFIG_ALARM

Address	bit	Access	Name	Default	Description		Clear State
5Fh	1	R/W	CONFIG_ALM[1]	0	Repetition select in case of the relative time	0:Not Repeat, 1:Repeat	Reset
	0	R/W	CONFIG_ALM[0]	0	Select of the Alarm time	0:absolute time, 1:relative time	Reset

* Reflected at after writing in 1 to LRQ_ALM

RRQ_LRQ_STATUS

Address	bit	Access	Name	Default	Description		Clear State
60h	4	R	RRQ_TIME_STATE	0	Status of the present time hold setting	0:non-completion, 1:completion	Reset
	3	R	LRQ_TIME_STATE	0	Status of the present time setting	0:non-completion, 1:completion	Reset
	2	R	LRQ_OFST_STATE	0	Status of the offset reflection setting	0:non-completion, 1:completion	Reset
	1	R	LRQ_WU_STATE	0	Status of the WakeUp time setting	0:non-completion, 1:completion	Reset
	0	R	LRQ_ALM_STATE	0	Status of the Alarm time setting	0:non-completion, 1:completion	Reset

RTC control description

The RTC function is controlled using the 6. RTC control register and the 7. Interrupt control register. (Each register is described in detail hereafter.)

・Reading the current time

The current time can be acquired by setting "1" in RRQ_TIME using an I2C command, waiting approximately 8 ms, and then reading CURT_PRE_1, CURT_PRE_2, CURT_POST_1, CURT_POST_2, CURT_POST_3 and CURT_POST_4 using an I2C command.

・Reading the Deep Sleep transition time

The time when the IC transitioned from normal operation to the Deep Sleep state can be acquired by returning from the Deep Sleep state, and then reading CURT_PRE_1, CURT_PRE_2, CURT_POST_1, CURT_POST2, CURT_POST_3 and CURT_POST_4 using an I2C command.

・Loading the time (absolute time)

Set the preset time in SET_PRE_1, SET_PRE_2, SET_POST_1, SET_POST_2, SET_POST_3 and SET_POST_4 using an I2C command. However, note that SET_PRE_1[5:0] is not used.

- Loading the time by external interrupt

The time set in SET_PRE_1, SET_PRE_2, SET_POST_1, SET_POST_2, SET_POST_3 and SET_POST_4 is loaded to the RTC in 3.9 ms or more to 6 ms or less when an external interrupt is input in the state with "1" set in INT_LRQ_TIME using an I2C command.

* In order to prevent unanticipated operation, it is recommended to set bit 2 of address 50h to "0" (default: 1) before inputting the interrupt. (When this processing is not performed, bit 0 of address 43h must be set to "1" before transitioning to the Deep Sleep state.)

- Loading the time by issuing a load request using I2C

The time set in SET_PRE_1, SET_PRE_2, SET_POST_1, SET_POST_2, SET_POST_3, and SET_POST_4 is loaded to the RTC in 3.9 ms or more to 6 ms or less by setting "1" in LRQ_TIME using an I2C command.

・Loading the time (relative time)

Set the preset time in SET_PRE_1, SET_PRE_2, SET_POST_1, SET_POST_2, SET_POST_3, SET_POST_4 using an I2C command. However, note that SET_PRE_1[5:0] is not used. In this case, set the relative time from the current RTC time in two's complement format.

Example: To set +2 s

SET_PRE_1=00h, SET_PRE2=00h, SET_POST_1=02h, SET_POST_2=00h, SET_POST_3=00h, SET_POST_4=00h

Example: To set -1 s

SET_PRE_1=00h, SET_PRE2=00h, SET_POST_1=FFh, SET_POST_2=FFh, SET_POST3=FFh, SET_POST_4=FFh

The relative time set in SET_PRE_1, SET_PRE_2, SET_POST_1, SET_POST_2, SET_POST_3 and SET_POST_4 is added to the current RTC time in 3.9 ms or more to 6 ms or less by setting "1" in LRQ_OFST using an I2C command.

・**Setting the return time from Deep Sleep**

Set the time to return from the Deep Sleep state beforehand in WU_PRE_1, WU_PRE_2, WU_POST_1, WU_POST_2, WU_POST_3 and WU_POST_4 using an I2C command. However, note that WU_PRE_1[5:0] is not used. WU_PRE_1, WU_PRE_2, WU_POST_1, WU_POST_2, WU_POST_3, WU_POST_4, and CONFIG_WKUP[1:0] noted below are enabled in 3.9 ms or more to 6 ms or less by setting "1" in LRQ_WU using an I2C command.

- Setting the return time by the absolute time

Set CONFIG_WKUP[1] = 0 and CONFIG_WKUP[0] = 0 (default settings) using an I2C command. In this case the absolute time is set by WU_PRE_1, WU_PRE_2, WU_POST_1, WU_POST_2, WU_POST_3 and WU_POST_4.

- Setting the return time by the relative time (with repeat)

Set CONFIG_WKUP[1] = 1 and CONFIG_WKUP[0] = 1 using an I2C command. In this case the time to return from the Deep Sleep state is the relative time from the current time, and is set in two's complement format in WU_PRE_1, WU_PRE_2, WU_POST_1, WU_POST_2, WU_POST_3 and WU_POST_4. In addition, when the return time is reached, the time obtained by further adding the relative time is repeatedly set.

- Setting the return time by the relative time (without repeat)

Set CONFIG_WKUP[1] = 0 and CONFIG_WKUP[0] = 1 using an I2C command. In this case the time to return from the Deep Sleep state is the relative time from the current time, and is set in two's complement format in WU_PRE_1, WU_PRE_2, WU_POST_1, WU_POST_2, WU_POST_3 and WU_POST_4.

・**Stop**

RTC counter operation stops within 2 ms after "1" is set in CNTR_STOP using an I2C command.

Selecting the interrupt output signal

Two different types of interrupt output can be selected by setting INT_SEL using an I2C command. When other values are set, an interrupt signal is not output.

3'd0 : Outputs an interrupt signal for a 3.9 ms period starting 2 ms after the time designated below.
3'd1 : Outputs an interrupt signal in 2 ms or more to 4 ms or less when an external interrupt is input.

・**Setting the interrupt output time**

Set the time to output an interrupt signal beforehand in WU_PRE_1, WU_PRE_2, WU_POST_1, ALM_POST_2, ALM_POST_3 and ALM_POST_4 using an I2C command. However, note that ALM_PRE_1[5:0] is not used. ALM_PRE_1, ALM_PRE_2, ALM_POST_1, ALM_POST_2, ALM_POST_3, ALM_POST_4 and CONFIG_ALM[1:0] noted below are enabled in 3.9 ms or more to 6 ms or less by setting "1" in LRQ_ALM using an I2C command.

- Setting the interrupt output time by the absolute time

Set CONFIG_ALM[1] = 0 and CONFIG_ALM[0] = 0 (default settings) using an I2C command. In this case the absolute time is set by ALM_PRE_1, ALM_PRE_2, ALM_POST_1, ALM_POST_2, ALM_POST_3 and ALM_POST_4.

- Setting the interrupt output time by the relative time (with repeat)

Set CONFIG_ALM[1] = 1 and CONFIG_ALM[0] = 1 using an I2C command. In this case the time to output the interrupt signal is the relative time from the current time, and is set in two's complement format in ALM_PRE_1, ALM_PRE_2, ALM_POST_1, ALM_POST_2, ALM_POST_3 and ALM_POST_4. In addition, when the set time is reached, the time obtained by further adding the relative time is repeatedly set.

- Setting the interrupt output time by the relative time (without repeat)

Set CONFIG_ALM[1] = 0 and CONFIG_ALM[0] = 1 using an I2C command. In this case the time to output the interrupt signal is the relative time from the current time, and is set in two's complement format in ALM_PRE_1, ALM_PRE_2, ALM_POST_1, ALM_POST_2, ALM_POST_3 and ALM_POST_4.

Information storage registers

DATA_GPS_ 1~16

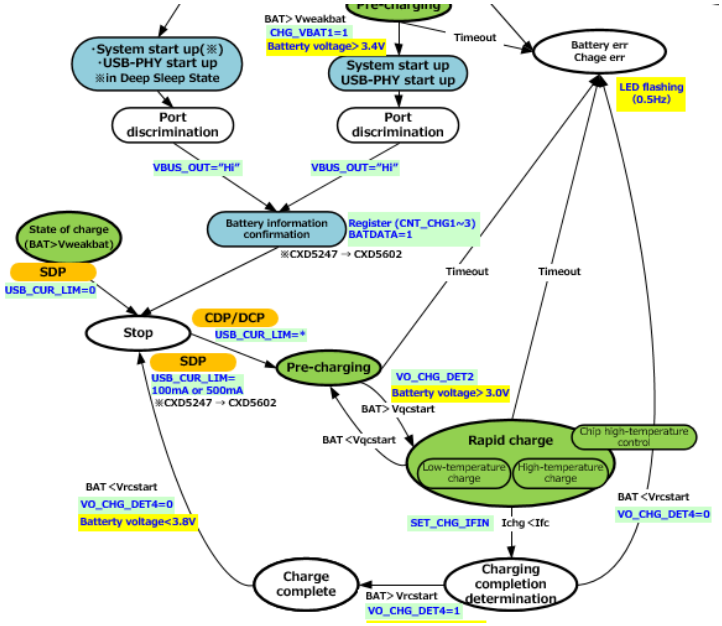
Address	bit	Access	Name	Default	Description	Clear State
61h	7:0	R/W	DATA_GPS1[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
62h	7:0	R/W	DATA_GPS2[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
63h	7:0	R/W	DATA_GPS3[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
64h	7:0	R/W	DATA_GPS4[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
65h	7:0	R/W	DATA_GPS5[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
66h	7:0	R/W	DATA_GPS6[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
67h	7:0	R/W	DATA_GPS7[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
68h	7:0	R/W	DATA_GPS8[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
69h	7:0	R/W	DATA_GPS9[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
6Ah	7:0	R/W	DATA_GPS10[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
6Bh	7:0	R/W	DATA_GPS11[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
6Ch	7:0	R/W	DATA_GPS12[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
6Dh	7:0	R/W	DATA_GPS13[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
6Eh	7:0	R/W	DATA_GPS14[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
6Fh	7:0	R/W	DATA_GPS15[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset
70h	7:0	R/W	DATA_GPS16[7:0]	0	Stores necessary information at the time of GPS Hot start	Reset

DATA_FREE_ 1~4

Address	bit	Access	Name	Default	Description	Clear State
71h	7:0	R/W	DATA_FREE1[7:0]	0	Stores necessary information for software side	Reset
72h	7:0	R/W	DATA_FREE2[7:0]	0	Stores necessary information for software side	Reset
73h	7:0	R/W	DATA_FREE3[7:0]	0	Stores necessary information for software side	Reset
74h	7:0	R/W	DATA_FREE4[7:0]	0	Stores necessary information for software side	Reset

Charge control registers

Please carry out the setting of data of 75h~7Fh in the condition of 77h[7]=0(SET_BATDATA=0).
The data of 75h~7Fh are reflected in “Stop” state



CNT_CHG 1

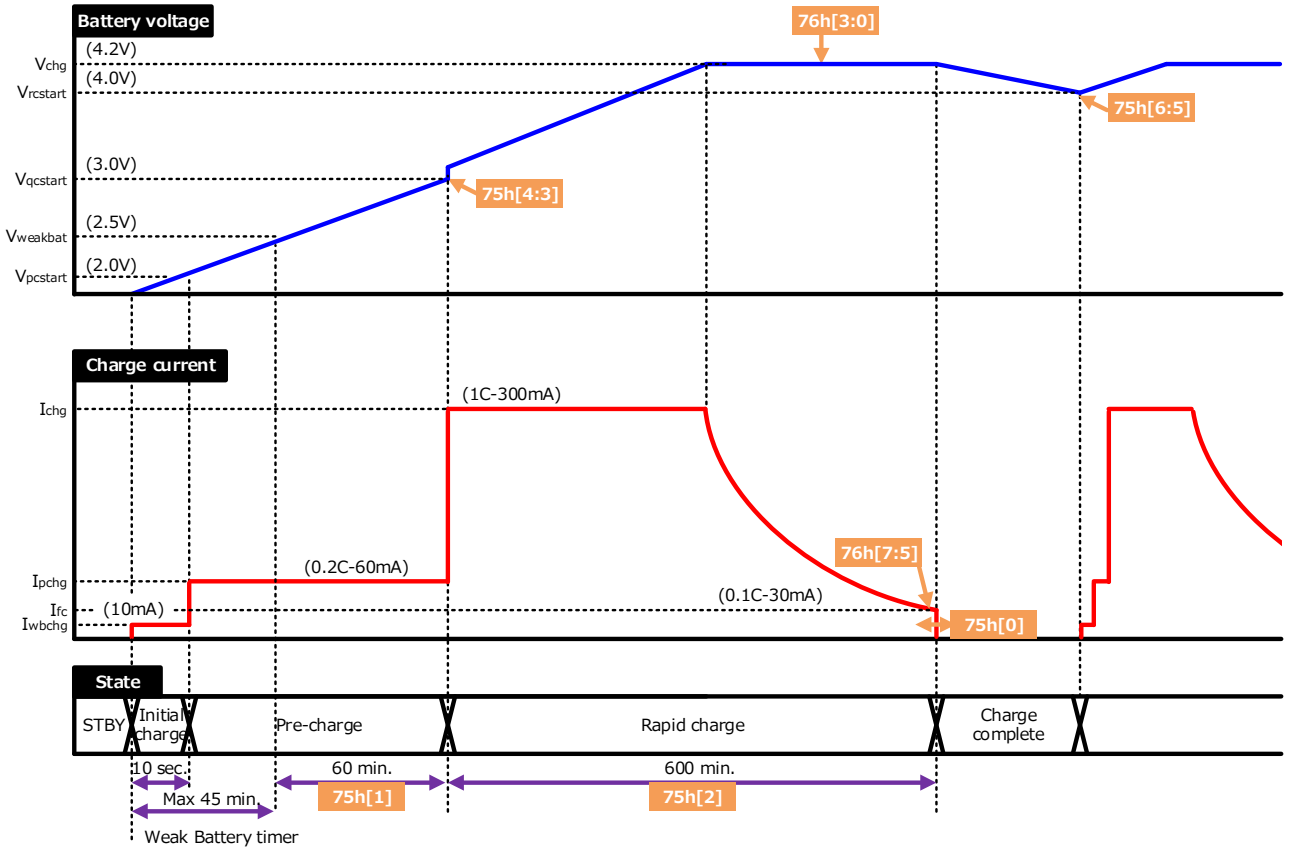
Address	bit	Access	Name	Default	Description		Clear State
75h	6:5	R/W	VO_CHG_DET4[1:0]	00b	Recharge start judgment voltage (for Vo_CHG_CNT3[4:0])	00b: -0.4V, 01b: -0.35V, 10b: -0.30V, 11b: -0.25V	Reset
	4:3	R/W	VO_CHG_DET2[1:0]	10b	Rapid charge start judgment voltage	00b:2.6V, 01b:2.8V, 10b:3.0V, 11b:3.2V	Reset
	2	R/W	SEL_CHG_TIME2	0	Rapid charge timer	0:600min, 1:300min	Reset
	1	R/W	SEL_CHG_TIME1	0	Pre-charge timer	0:60min, 1:120min	Reset
	0	R/W	SEL_CHG_TIME0	0	Charge completion current judgment time	0:4clk(250ms*4clk), 1:40clk(250ms*40clk)	Reset

*SEL_CHG_TIME0 links the VBUS loser detection time in the Rapid charge state.

CNT_CHG2

Address	bit	Access	Name	Default	Description		Clear State
76h	7:5	R/W	SET_CHG_IFIN	010b	Charge completion judgment current	000b: 50mA, 001b: 40mA, 010b: 30mA, 011b: 20mA, 100b: 10mA	Reset
	4	R/W	-	0	Reserved		Reset
	3:0	R/W	VO_CHG_CNT3[4:0]	0100b	Charge control voltage 4.0V~4.4V 50mVstep	0000b:4.00V, 0001b:4.05V, 0010b:4.10V, 0011b:4.15V, 0100b:4.20V, 0101b:4.25V, 0110b:4.30V, 0111b:4.35V, 1000b:4.40V, 1001b~1111b:4.20V	Reset

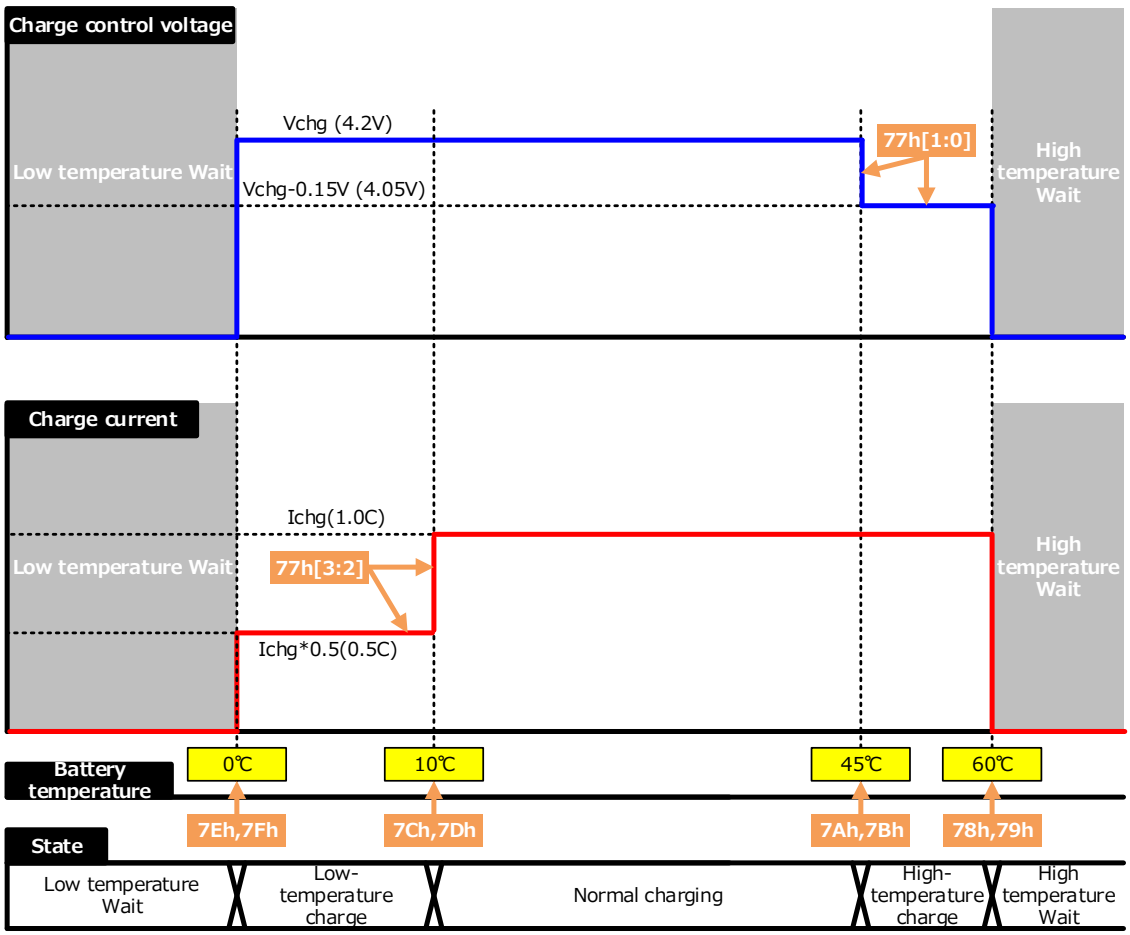
*SET_CHG_IFIN: Resistance between VSYS_CS-VBAT_CS in the case of 0.1ohm, in addition, it is effective only at Rapid charge.



CNT_CHG3

Address	bit	Access	Name	Default	Description		Clear State
77h	7	R/W	SET_BATDATA	0	Battery data input	0:non-entry, 1:entry	Reset
	3:2	R/W	SET_CHG_THL	00b	Low temperature charge setting (Rapid charge current)	00b: Charge 1C to 0deg 01b: Charge 1C to 10deg 10b: Charge 0.5C between 0deg and 10deg	Reset
	1:0	R/W	SET_CHG_THH	00b	High temperature charge setting *Vo_CHG_CNT3[4:0]=4.2V	00b: 4.2V to 60deg 01b: 4.2V to 45deg 10b: 4.05V between 45deg and 60deg	Reset

*When "0" is storing in SET_BATDATA, the charge is not started (at Good battery).



SET_T60_1

Address	bit	Access	Name	Default	Description	Clear State
78h	7:0	R/W	SET_T60_1[7:0]	E8h	Stores battery temperature 60 degrees from the LSB side(7-0bit)	Reset

SET_T60_2

Address	bit	Access	Name	Default	Description	Clear State
79h	4:0	R/W	SET_T60_2[3:0]	2h	Stores battery temperature 60 degrees from the LSB side(11-8bit)	Reset

SET_T45_1

Address	bit	Access	Name	Default	Description	Clear State
7Ah	7:0	R/W	SET_T45_1[7:0]	A4h	Stores battery temperature 45 degrees from the LSB side(7-0bit)	Reset

SET_T45_2

Address	bit	Access	Name	Default	Description	Clear State
7Bh	4:0	R/W	SET_T45_2[3:0]	4h	Stores battery temperature 45 degrees from the LSB side(11-8bit)	Reset

SET_T10_1

Address	bit	Access	Name	Default	Description	Clear State
7Ch	7:0	R/W	SET_T10_1[7:0]	D5h	Stores battery temperature 10 degrees from the LSB side(7-0bit)	Reset

SET_T10_2

Address	bit	Access	Name	Default	Description	Clear State
7Dh	4:0	R/W	SET_T10_2[3:0]	Ah	Stores battery temperature 10 degrees from the LSB side(11-8bit)	Reset

SET_T0_1

Address	bit	Access	Name	Default	Description	Clear State
7Eh	7:0	R/W	SET_T0_1[7:0]	07h	Stores battery temperature 0 degrees from the LSB side(7-0bit)	Reset

SET_T0_2

Address	bit	Access	Name	Default	Description	Clear State
7Fh	4:0	R/W	SET_T0_2[3:0]	Ch	Stores battery temperature 0 degrees from the LSB side(11-8bit)	Reset

R[kohm]	Temperature[deg]	Ratio	DEC	HEX	
4397.12	-40	97.8%	4005	FA4	
3088.6	-35	96.9%	3968	F7F	
2197.23	-30	95.6%	3918	F4D	
1581.88	-25	94.1%	3852	F0C	
1151.04	-20	92.0%	3769	EB8	
846.579	-15	89.4%	3663	E4F	
628.988	-10	86.3%	3534	DCE	
471.632	-5	82.5%	3379	D33	
357.012	0	78.1%	3200	C7F	SET_T0: detection side
	2.5	75.6%	3098	C19	SET_T0: cancellation side
272.5	5	73.2%	2996	BB4	
209.71	10	67.7%	2773	AD5	SET_T10: detection side
	12.5	64.8%	2655	A5E	SET_T10: cancellation side
162.651	15	61.9%	2536	9E8	
127.08	20	56.0%	2292	8F4	
100	25	50.0%	2048	7FF	
79.222	30	44.2%	1810	712	
63.167	35	38.7%	1586	631	
50.677	40	33.6%	1378	561	
	42.5	31.3%	1283	503	SET_T45: cancellation side
40.904	45	29.0%	1189	4A4	SET_T45: detection side
33.195	50	24.9%	1021	3FC	
27.091	55	21.3%	873	369	
	57.5	19.7%	809	328	SET_T60: cancellation side
22.224	60	18.2%	745	2E8	SET_T60: detection side
18.323	65	15.5%	634	27A	
15.184	70	13.2%	540	21B	
12.635	75	11.2%	459	1CB	
10.566	80	9.6%	391	187	
8.873	85	8.1%	334	14D	
7.481	90	7.0%	285	11D	
6.337	95	6.0%	244	F4	
5.384	100	5.1%	209	D1	
4.594	105	4.4%	180	B3	
3.934	110	3.8%	155	9B	
3.38	115	3.3%	134	85	
2.916	120	2.8%	116	74	
2.522	125	2.5%	101	64	

Input value of TH terminal at using NCP15WF104F03RC

CNT_USB1

Address	bit	Access	Name	Default	Description		Clear State
80h	5:1	R/W	STATE_CHG	00h	Charge state storage register		Reset
	0	R/W	USB_PORT_TYPE	0	USB port classification	0:SDP, 1:DCP/CDP	Reset

*STATE_CHG reflects in “8Bh=1”

80h[5:1]	STATE
5'd0	P_S_INIT_RST
5'd1	P_S_INIT_WAIT
5'd2	P_S_INIT_CHK
5'd3	P_S_DBP_START
5'd4	P_S_DB_INICHARGE
5'd5	P_S_DB_PRECHARGE
5'd6	P_S_DCON_WAIT
5'd7	P_S_PD_START
5'd8	P_S_DM_COMPARE
5'd9	P_S_PD_END
5'd10	P_S_BAT_WAIT
5'd11	P_S_CHG_STOP
5'd12	P_S_GB_PRECHARGE
5'd13	P_S_GB_QCKCHARGE
5'd14	P_S_GB_LOWCHARGE
5'd15	P_S_GB_HIGHCHARGE
5'd16	P_S_CHG_JUDGE
5'd17	P_S_CHG_COMPLETE
5'd18	P_S_GB_CONWAIT
5'd19	P_S_GB_CPTEMPWAIT1
5'd20	P_S_GB_CPTEMPWAIT2
5'd21	P_S_GB_TEMPWAIT
5'd22	P_S_DB_TEMPWAIT
5'd23	P_S_DB_CONWAIT
5'd24	P_S_BAT_UNUSUAL
5'd25	P_S_BAT_DISCON

CNT_USB2

Address	bit	Access	Name	Default	Description		Clear State
81h	2	R/W	SET_CHGOFF	0	Forced charge reset signal	0:normal, 1:reset	Reset
	1:0	R/W	USB_CUR_LIM	00b	Charge current setting	00b:<2.5mA, 01b:<100mA, 10b:<500mA	Reset

* Charge and all the USB detection functions are initialized by “SET_CHGOFF=1”

AFE control registers

SET_AFE_1

Address	bit	Access	Name	Default	Description	Clear State
82h	5:0	R/W	SET_ACT_1[5:0]	00h	Measurement period “Ts” setting in Ready,StartUP,PowerON.	Reset

*The measurement period is cf. list shown below.

*As for the data of 82h~84h, setting is recommended in 84h[3:2]=00b (measurement stop).

*After a measurement period changed, a measurement is carried out immediately.

SET_AFE_2

Address	bit	Access	Name	Default	Description	Clear State
83h	5:0	R/W	SET_ACT_1[5:0]	0Ch	Measurement period “Ts” setting in Deep Sleep.	Reset

*The measurement period is cf. list shown below

HEX	DEC	Ts	
0	0	125	ms
1	1	250	ms
2	2	500	ms
3	3	1	sec
4	4	2	sec
5	5	4	sec
6	6	8	sec
7	7	16	sec
8	8	32	sec
9	9	1.067	min
A	10	2.133	min
B	11	4.267	min
C	12	8.533	min
D	13	17.067	min
E	14	34.133	min
F	15	1.138	h
10	16	2.276	h
11	17	4.551	h
12	18	9.102	h
13	19	18.204	h

SET_AFE3

Address	bit	Access	Name	Default	Description		Clear State
84h	3:2	R/W	SET_ACT_4	01b	Movement measurement mode	00b:Mesurement stop, 01b: repetition measurement, 02b:once measurement	Reset
	1:0	R/W	SET_ACT_3[1:0]	00b	Moving average number of times	00b:one time, 01b:two times, 10b:four times	Reset

*SET_ACT_3 is 00b after 02b note movement

*SET_ACT_3 is applied to 3C register, 85~8A,8D,8E register

DATA_AFE* of 85h~8Ah is taken in in 8Bh= "1"

DATA_AFEV_1

Address	bit	Access	Name	Default	Description	Clear State
85h	7:0	R	DATA_AFEV_1[7:0]	00h	Stores the battery voltage from the LSB side (7-0bit)	Reset

DATA_AFEV_2

Address	bit	Access	Name	Default	Description	Clear State
86h	3:0	R	DATA_AFEV_2[3:0]	00h	Stores the battery voltage from the LSB side (11-8bit)	Reset

DATA_AFEI_1

Address	bit	Access	Name	Default	Description	Clear State
87h	7:0	R	DATA_AFEI_1[7:0]	00h	Stores the battery current from the LSB side (7-0bit)	Reset

DATA_AFEI_2

Address	bit	Access	Name	Default	Description	Clear State
88h	3:0	R	DATA_AFEI_2[3:0]	00h	Stores the battery current from the LSB side (11-8bit)	Reset

DATA_AFET_1

Address	bit	Access	Name	Default	Description	Clear State
89h	7:0	R	DATA_AFET_1[7:0]	00h	Stores the battery temperature from the LSB side (7-0bit)	Reset

DATA_AFET_2

Address	bit	Access	Name	Default	Description	Clear State
8Ah	3:0	R	DATA_AFET_2[3:0]	00h	Stores the battery temperature from the LSB side (11-8bit)	Reset

LRQ_AFE

Address	bit	Access	Name	Default	Description		Clear State
8Bh	0	R/W	LRQ_AFED	0	Reflect AFE register	0:disable, 1:enable	Reset

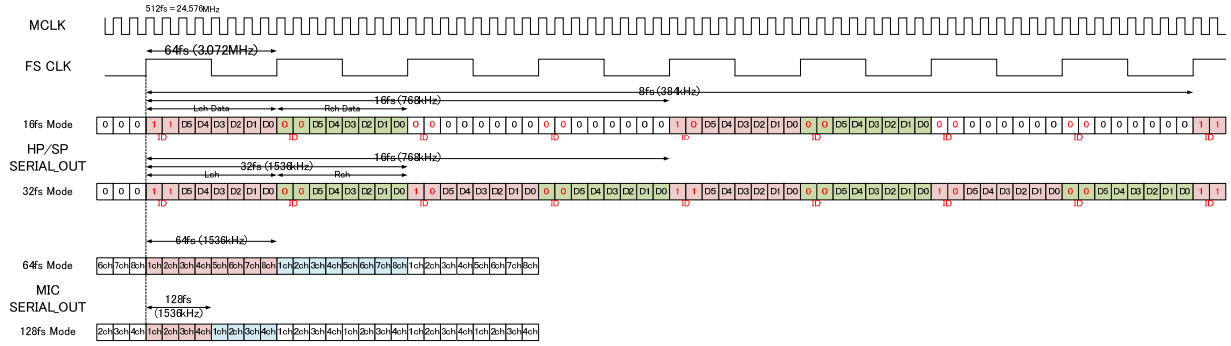
*After reflect DATA_AFE register, "0" is stored.

LRQ_STATUS

Address	bit	Access	Name	Default	Description		Clear State
8Ch	0	R	LRQ_AFED_STATE	0	Status of AFE data	0: Setting non-completion, 1: Setting completion	Reset

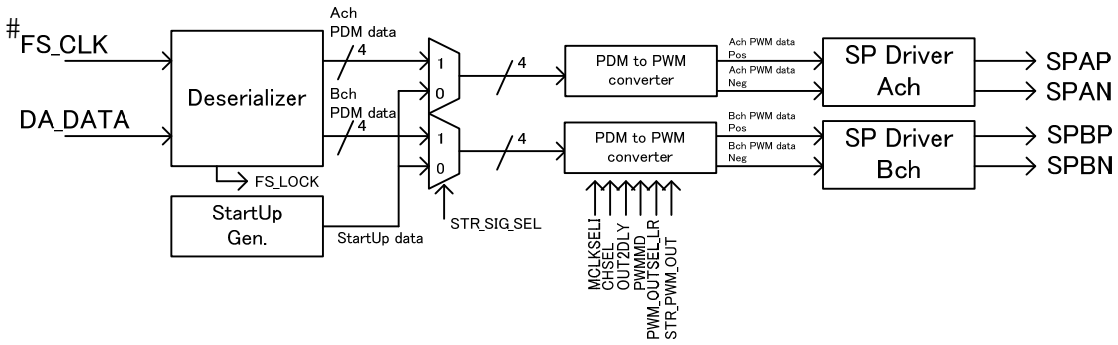
◆Audio interface specifications

CXD5247 performs signal transfer with the CXD5602 using an original format. The timing chart is shown below. The output signals to the SP can be set to the two modes of 16fs or 32fs, and the MIC output can be set to the two modes of 64fs (8Mic) or 128fs (4Mic).



Interface Timing

SP Signal Path

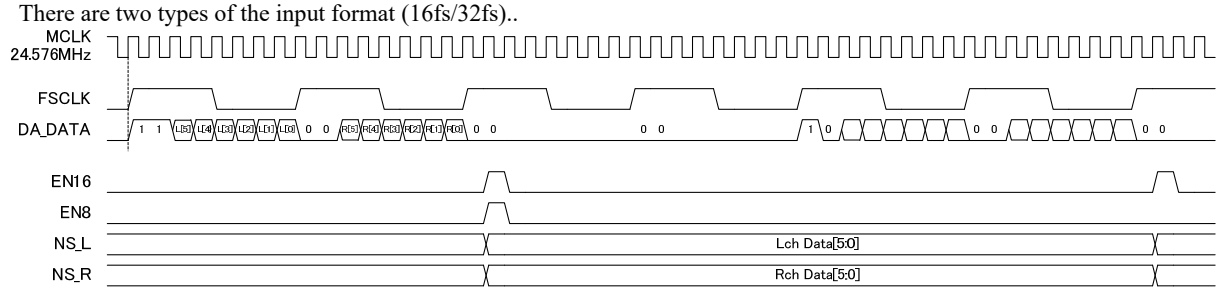


SP Signal Path

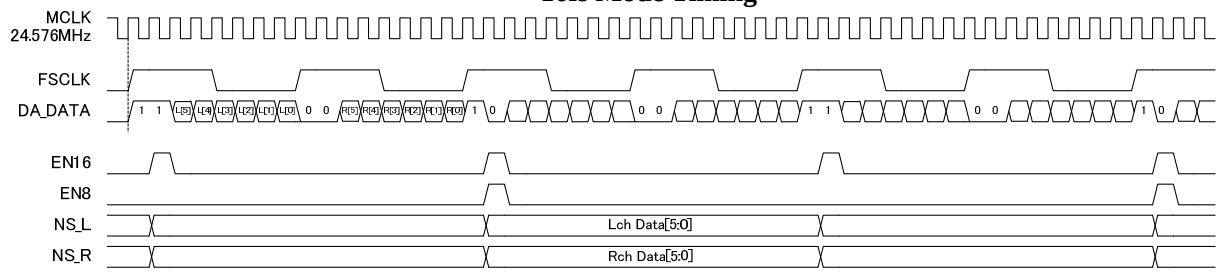
The serialized audio signals (DA_DATA, FS_CLK) output from the CXD5602 are input to the Deserialize circuit and converted into two channels of 6-bit PDM signals. These signals are converted into 1-bit PWM signals by the PDMtoPWM conversion circuit, and then output as audio signals from the drivers. In addition, a StartUP signal generation circuit is provided separately from the main line signal as a popping noise countermeasure during power-on, and when the popping noise countermeasure is set, the generated StartUp signal is selected by the register and output.

Deserialize

There are two types of the input format (16fs/32fs)..



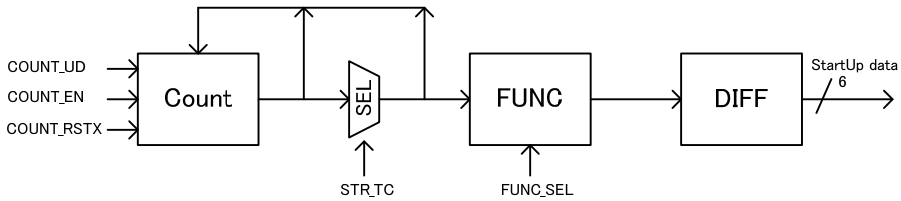
16fs Mode Timing



32fs Mode Timing

There are no settings for this circuit. Operation switches between 16fs and 32fs mode in accordance with the input signal.
This circuit has a function that checks for the presence of a separately input FSCLK, and the result is stored in the internal register as the FS_LOCK status information.

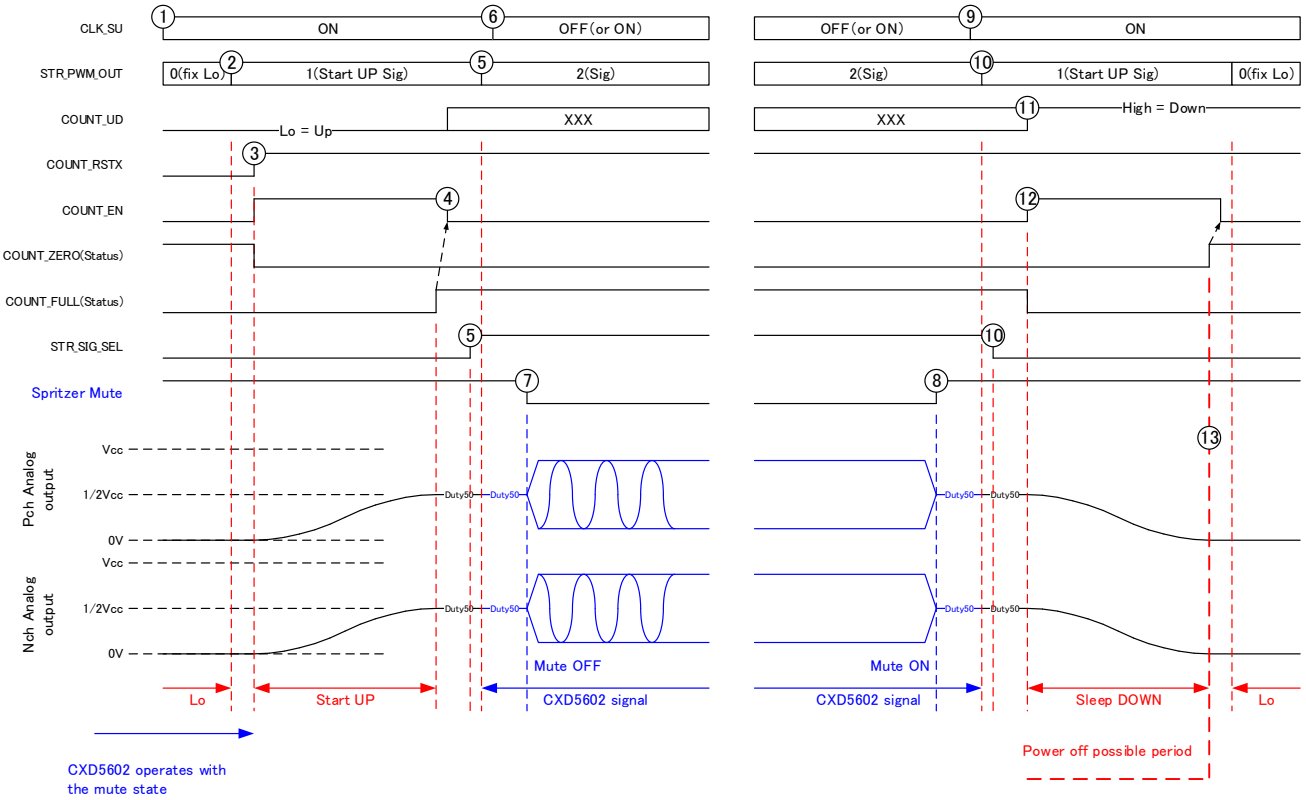
StartUP signal generation



StartUP Block

A sequence circuit raises the output pin voltage gradually from 0 V to 1/2 AVDD_DRV* in order to reduce the popping noise generated during power-on when a headphone speaker is connected to the CXD5247 Audio SP output by capacitor coupling. In addition, popping noise generated during power-off can be reduced by operating this circuit in the reverse direction. The PWM conversion circuit input switches during sequence operation.

StartUP/SleepDOWN sequence



This is the setting sequence when using the sequence circuit. Follow the sequence below and make the settings after the CLK setting sequence.

StartUP (power-on)　Set the CXD5602 side to the MUTE state.

1. CLK_SU　0(default)→1　Set the StartUP circuit CLK to on.
2. STR_PWM_OUT　0(default)→1　Select the StartUP circuit signal.
3. COUNT_RSTX / COUNT_EN　0→1　The StartUP circuit operates. At this time COUNT_UD = 0 (default).
4. Change COUNT_EN from "1" to "0" after the set STR_TC time or when COUNT_FULL = 1 (Status).
5. STR_SIG_SEL　0(default)→1、STR_PWM_OUT　1→2　Select the audio signal from CXD5602.
6. CLK_SU　1→0　Turn off the StartUP circuit CLK to save power. (The CLK can also be left on without problem.)
7. Cancel the CXD5602 MUTE.

SleepDOWN (power-off)

8. Set the CXD5602 side to the MUTE state.
9. CLK_SU　0→1　Set the StartUP circuit CLK to on.
10. STR_SIG_SEL　1→0、STR_PWM_OUT　2→1　Select the StartUP circuit signal.
11. COUNT_UD　0(default)→1
12. COUNT_EN　0→1　The StartUP circuit operates. (SleepDOWN operation)
13. Operation ends (power-off) after the set STR_TC time or when COUNT_ZERO = 1 (Status).

* Do not change the other register values during the period while COUNT_EN = 1.

PWM conversion

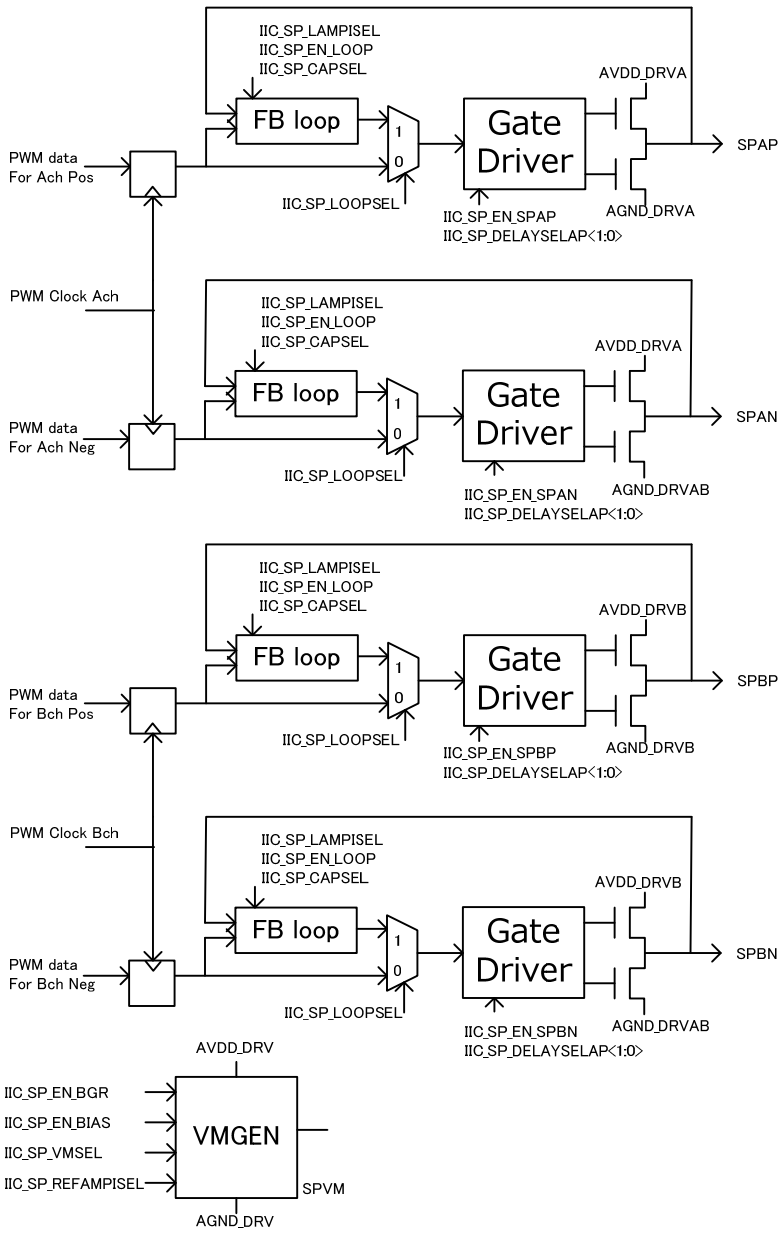
The input 6-bit PDM signals are converted to PWM signals. 2-bit (Pos/Neg) signals are output on each of Ach and Bch. 24.576 MHz operation is set in 16fs mode, and 49.152 MHz is set in 32fs mode.

Register name	Description
MCKSELI	Sets operation according to the CLK frequency. Please change the value below in accordance with the operating mode. 1: 16fs mode with 24.576MHz or 32fs mode with 49.152MHz 0: 16fs mode with 49.152MHz
CHSEL	Replace Ach and Bch 0: standard <default> 1: replace Ach and Bch
OUT2DLY	PWM delay of negative signal (SPAN, SPBN) 0 : <default 1: 1clk@master clock N: n-clk@master clock 15: 15clk@master clock

Register name	Description
PWMMD	Selects PWM convert mode 0 : One side modulation mode 1: Both side modulation mode <default> 2: Alternated one side modulation mode 3: Alternated one side modulation mode
PWM_OUTSEL_LR	Selects negative signal (SPAN/SPBN) of driver output 0: standard operation <default> 1: ~LP/~RP 2/6/7: Low 3: High 4: 50% duty cycle signal 5: inverse of 50%duty cycle signal
STR_PWM_OUT	Selects startup signal 0: Low<default> 1: Select Startup signal 2/3: normal operation

SP Driver

An external speaker (8Ω) is driven by a low resistance driver circuit. The input Ach and Bch 2-bit (Pos/Neg) PWM data is switched to the low jitter clock domain to reduce output noise due to clock jitter. This driver has a pulse width correction circuit called a feedback loop that enables to effectively correct driver error due to factors such as power supply fluctuation, driver Pos/Neg mismatch, or dead time distortion. The driver clock settings are described in the clock generation block section.



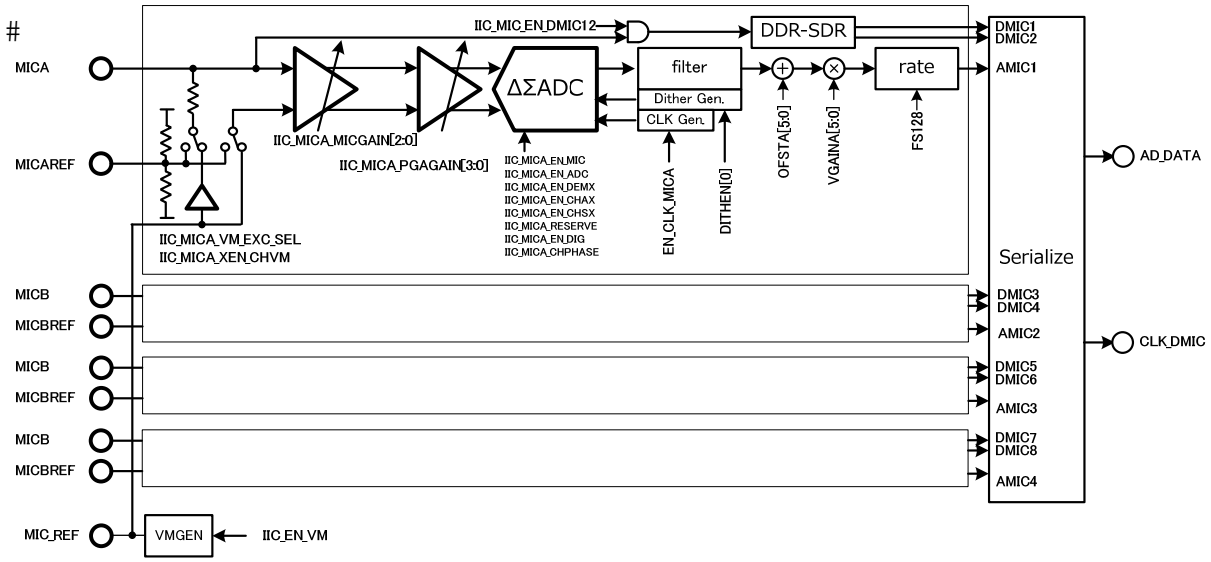
SP Driver Block

Register name	Description
SP_EN_SPAP SP_EN_SPAN SP_EN_SPBP SP_EN_SPBN	Control the driver output 0: disable 1: enable
SP_DELAYSELAP<1:0> SP_DELAYSELAN<1:0> SP_DELAYSELBP<1:0> SP_DELAYSELBN<1:0>	Selects the driver's dead time 0 : shortest <default> 1: shorter 2: longer 3: longest

Register name	Description
SP_LOOPSEL	Selects the output 0: normal operation <default> 1: select the loop signal
SP_LOOPEN	Control loop circuit 0: disable 1: enable
SP_CAPSEL	Selects the feedback capacitor 0: 16fs mode (24.576MHz) <default< 1: 32fs mode (49.152MHz)
SP_LAMPISEL	Internal bias current setting 0: normal <default> 1: test only
SP_EN_BGR	Sets the reference voltage 0: normal operation <default> 1: please set if loop circuits is enable
SP_EN_BIas	Sets the internal bias 0 normal operation <default> 1: please set of loop circuits is enable

◆MIC signal path

This IC has four systems of analog microphone interfaces (microphone amplifier with PGA function: ΔΣADC) and eight systems of digital microphone interfaces. The analog microphone input pins and digital microphone input pins are shared and used exclusively. The analog microphone interfaces convert the analog microphone signals to digital data. A clock generation circuit and a dither generation circuit are provided as ADC control signals. The data output by the ADC is digitally processed and converted to 1-bit PDM signals. This processing consists of a CIC-Decimator, offset adjustment circuit, gain adjustment circuit, and ΔΣModulator circuit. The output data rate can be set to 64fs or 128fs. In addition, the digital microphone interfaces perform DDR-SDR conversion on the signals. The above microphone signals (analog 4ch + digital 8ch, total 12ch) are input to the serialize circuit, converted to 8 channels or 4 channels of 1-bit serial data, and output from CXD5247 as AD_DATA.



MIC Signal Path

Analog microphone input configuration

Each analog microphone input is dc-biased to center voltage between AVDD_MIC and AGND_MIC. Two types setting for biasing can be selected. First is the individually biased using each reference pins(MICAREF/MICBREF/MICCREF/MICDREF), second is the shared biasing using common bias pins(MIC_REF). To minimize the external components (remove decoupling capacitor), shared biasing type is useful. Table * shows the input bias setting.

Table MIC bias configuration

Register name	Description
MIC_EN_VM	MIC_REF control 0: disable 1:enable
MICA_VM_EXC_SEL	Analog microphone input A bias setting 0: shared 1:indivisual
MICB_VM_EXC_SEL	Analog microphone input B bias setting 0: shared 1:indivisual
MICC_VM_EXC_SEL	Analog microphone input C bias setting 0: shared 1:indivisual
MICD_VM_EXC_SEL	Analog microphone input D bias setting 0: shared 1:indivisual

PGA setting

Analog microphones inputs have two stages of programmable gain amplifiers(PGAs). A coarse preamplifier gain stage offers selectable 0dB, 3dB, 6dB, 9dB, 12dB and 15dB gain settings. A fine stage is a PGA adjustable from 0dB to 6dB in 0.5dB steps. (Tables * and *). The two stages provide up to 21dB of signal gain for the analog microphone inputs. To maximize the signal-to-noise ratio, use the coarse gain setting of the first stage whenever possible.

Table MIC Gain configuration

Register name	Description
MICA_MICGAIN<2:0>	Microphone A input MICGAIN setting 101 +15dB 100 +12dB 011 +9dB 010 +6dB 001 +3dB 000 0dB <default> Other prohibited

Register name	Description
MICB_MICGAIN<2:0>	Microphone B input MICGAIN setting 101 +15dB 100 +12dB 011 +9dB 010 +6dB 001 +3dB 000 0dB <default> Other prohibited
MICC_MICGAIN<2:0>	Microphone C input MICGAIN setting 101 +15dB 100 +12dB 011 +9dB 010 +6dB 001 +3dB 000 0dB <default> Other prohibited
MICD_MICGAIN<2:0>	Microphone D input MICGAIN setting 101 +15dB 100 +12dB 011 +9dB 010 +6dB 001 +3dB 000 0dB <default> Other prohibited

Table PGA gain configration

Register name	Description
MICA_PGAGAIN<3:0>	Microphone A input PGA gain setting 1100 +6.0dB 1011 +5.5dB 1010 +5.0dB 1001 +4.5dB 1000 +4.0dB 0111 +3.5dB 0110 +3.0dB 0101 +2.5dB 0100 +2.0dB 0011 +1.5dB 0010 +1.0dB 0001 +0.5dB 0000 0dB <default> Others : prohibited
MICB_PGAGAIN<3:0>	Microphone B input PGA gain setting 1100 +6.0dB 1011 +5.5dB 1010 +5.0dB 1001 +4.5dB 1000 +4.0dB 0111 +3.5dB 0110 +3.0dB 0101 +2.5dB 0100 +2.0dB 0011 +1.5dB 0010 +1.0dB 0001 +0.5dB 0000 0dB <default> Others : prohibited

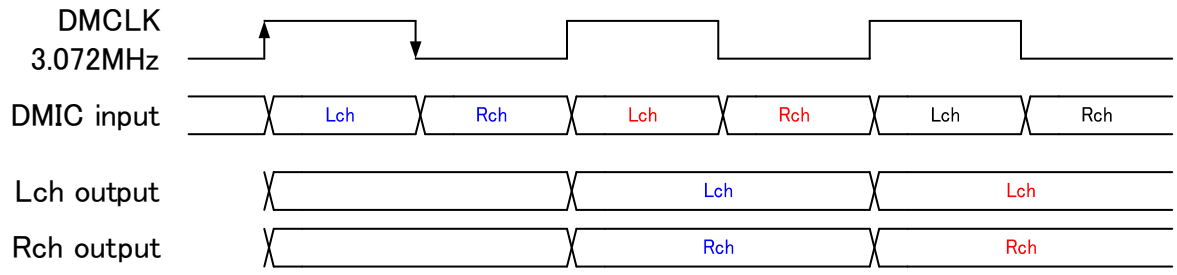
Register name	Description
MICC_PGAGAIN<3:0>	Microphone C input PGA gain setting 1100 +6.0dB 1011 +5.5dB 1010 +5.0dB 1001 +4.5dB 1000 +4.0dB 0111 +3.5dB 0110 +3.0dB 0101 +2.5dB 0100 +2.0dB 0011 +1.5dB 0010 +1.0dB 0001 +0.5dB 0000 0dB <default> Others : prohibited
MICD_PGAGAIN<3:0>	Microphone D input PGA gain setting 1100 +6.0dB 1011 +5.5dB 1010 +5.0dB 1001 +4.5dB 1000 +4.0dB 0111 +3.5dB 0110 +3.0dB 0101 +2.5dB 0100 +2.0dB 0011 +1.5dB 0010 +1.0dB 0001 +0.5dB 0000 0dB <default> Others : prohibited

Table MIC control pins

Register name	Description

Digital Microphone interface

The digital microphone transfers the L/R signal at both the rising and falling edges of DMCLK (CLK for digital microphone), so this function separates the input signal into the two L and R signals. The I/O timing chart is shown below.



DMIC Timing

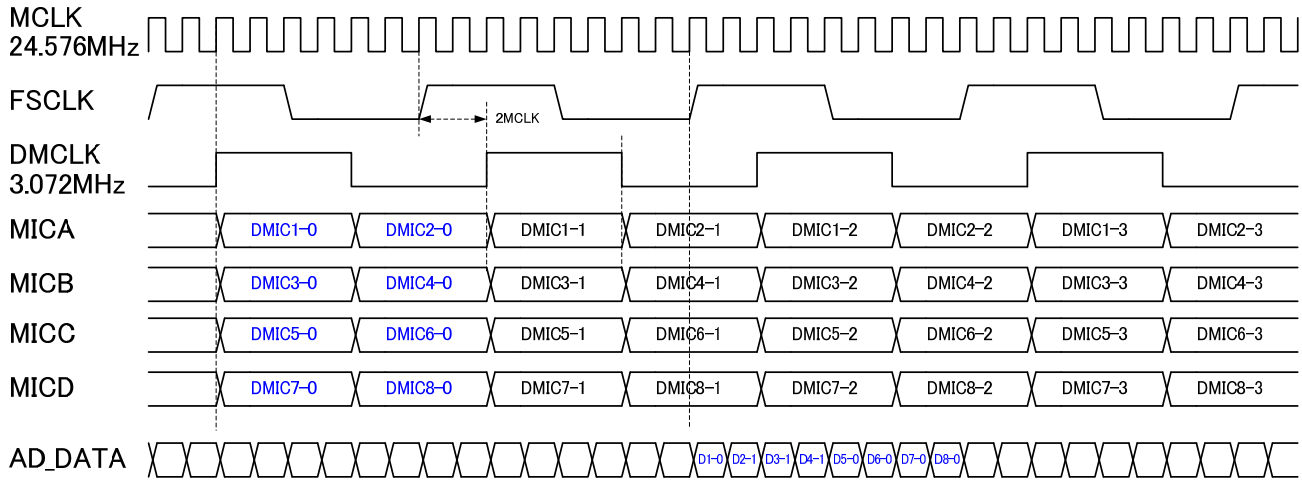
Table Digital MIC interface configuration

Register name	Description
MICA_EN_DMIC12	MICA, Digital microphone interface enabler 0:disable 1:enable
MICA_EN_DMIC34	MICB, Digital microphone interface enabler 0:disable 1:enable
MICA_EN_DMIC56	MICC, Digital microphone interface enabler 0:disable 1:enable
MICA_EN_DMIC78	MICD, Digital microphone interface enabler 0:disable 1:enable

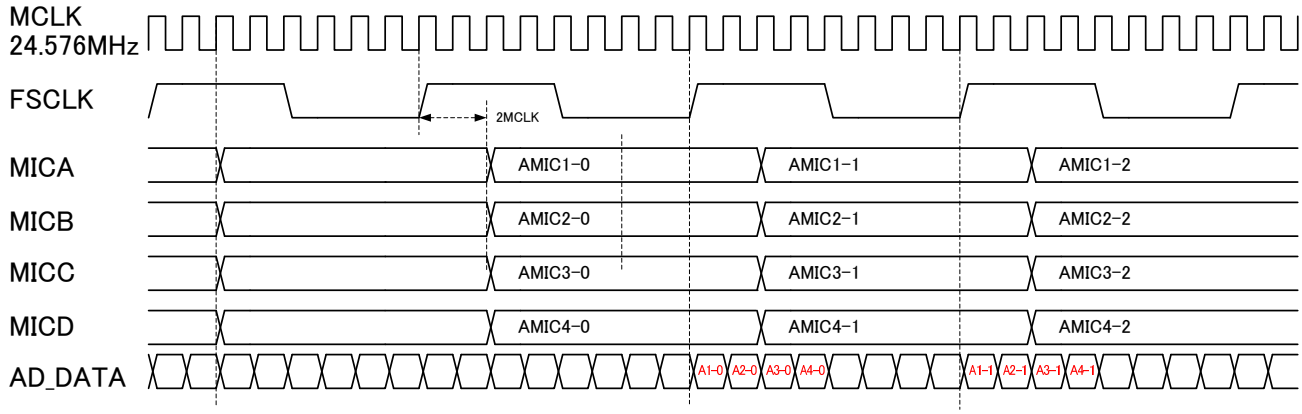
Serialize

This function selects and serializes the 4 channels of analog microphone signals and 8 channels of digital microphone signals (total 12 channels of microphone signals). The signals are output from AD_DATA of CXD5247 synchronized with FSCLK, which is the timing reference for the interface with the CXD5602. Two output formats are available: 64fs (3.072 MHz/sample) and 128fs (6.144 MHz/sample). The 64fs format enables 8-channel signal transfer, and the 128fs format enables 4-channel signal transfer. The timing chart for each format is shown below.

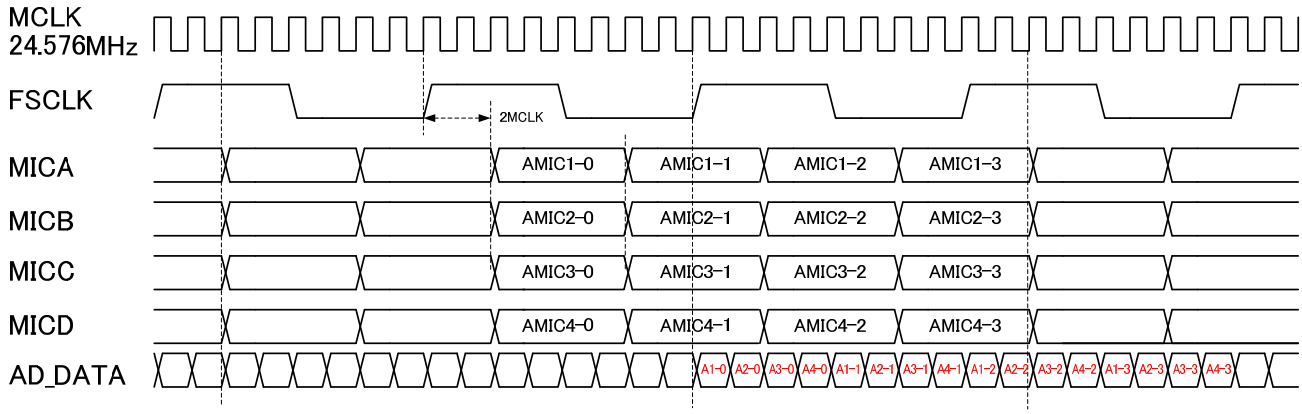
* The digital microphone signal supports only the 64fs format, and cannot be used with the 128fs format.



64fs Mode Digital MIC Interface Timing



64fs Mode Analog MIC Interface Timing



128fs Mode Analog MIC Interface Timing

Serialize mode of 64fs and 128fs is selected by SER_MODE register. Data order in AD_DATA such as D1-0, A1-0 is optionally selectable using configuration register SEL_CHx. (talble * and *)

Table serializer configuration

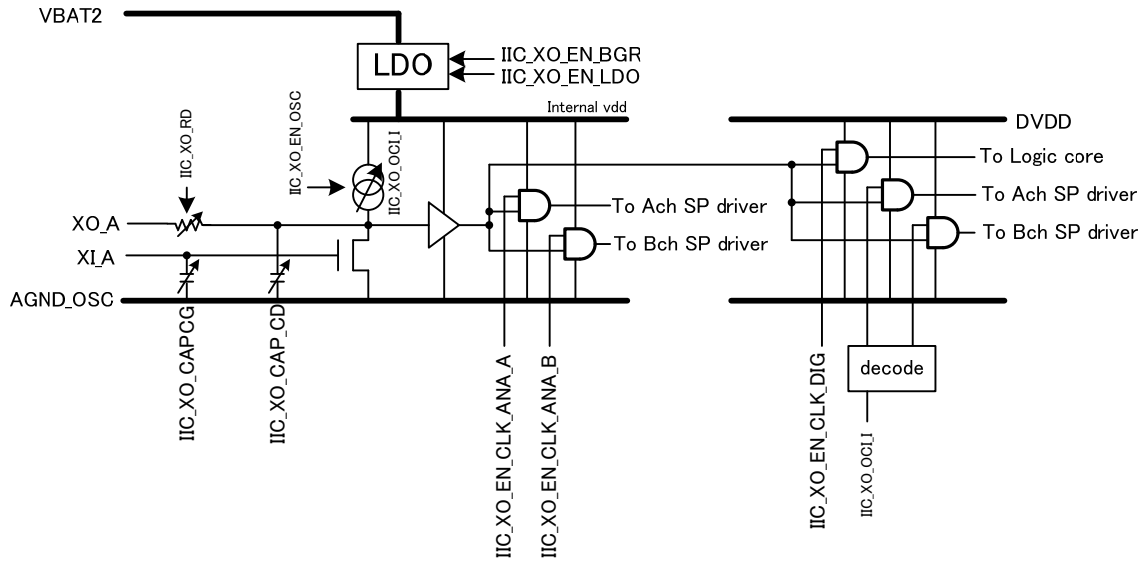
Register name	Description
SER_MODE	Selects serialize mode 64fs or 128fs 0: 64fs mode (8ch data can be transferred) 1:128fs mode (4ch data can be transferred)
SEL_CHx	Selects serial output data order. X=1..8 0: 0 1: selects AMIC1 2: selects AMIC2 3: selects AMIC3 4: selects AMIC4 5: selects DMIC1 6: selects:DMIC2 7: selects DMIC3 8: selects DMIC4 9: selects DMIC5 10: selects DMIC6 11: selects DMIC7 12: selects DMIC8 13-15:0

◆Clock specifications

X’tal Buffer

CXD5247 Audio block has a low jitter crystal oscillator amplifier for the system clock and class-D amplifier reference clock. To minimize the clock jitter, macro has an LDO for internal power supply and internal load capacitance. Load capacitances controlled by CAPCG/CAPCD are integrated to remove external capacitances and selectable for x’tal matching. This is very effective to achieve low jitter performance avoiding noise from uncontrolled GND bounce. Drive strength is selectable for both oscillation frequency of 24.576MHz and 49.152MHz, and also enables to reduce the operating current at stable oscillation. Figure * shows the oscillator block diagram with control register. Internal series resister can be used for control drive level.

Clocks can be controlled by XO_EN_CLK_DIG/XO_CLK_ANA_A/ XO_CLK_ANA_B for several use-case.

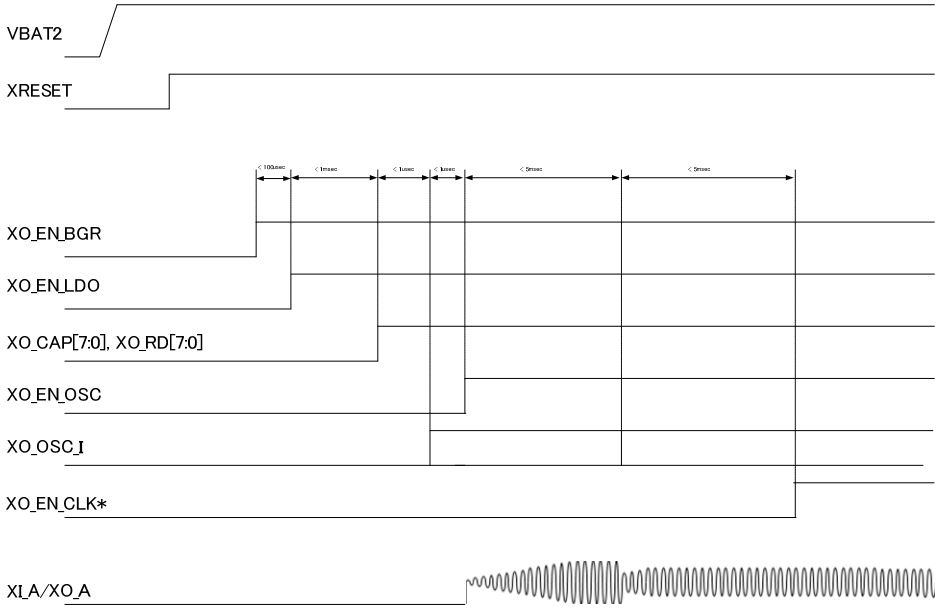


Register name	Description
XO_CAP_CG<7:0> XO_CAP_CD<7:0>	Selects internal load capacitance 0: 0[pF] <default> 19: 9.5[pF] for 49.152MHz 26: 13[pF] for 24.576MHz Others data: data/2 [pF]

Register name	Description
XO_OSC_I<7:0>	Selects driver strength 0 : 0[uA] <default> 6 : 360[uA] for stable oscillation at 49.152MHz, less than 100uW of maximum oscillation level 8 : 480[uA] for stable oscillation at 24.576MHz, less than 200uW of maximum oscillation level 9 : 540[uA] for stable oscillation at 49.152MHz, less than 200uW of maximum oscillation level. 13 : 780[uA] for start-up at 24.576MHz 15:900[uA] for start-up at 49/152MHz Others Data: data x 60 [uA]
XO_RD<1:0>	Selects series resistance of XO_A from driver 0 : 450 ohm for start-up of 49MHz oscillation 1: 550 ohm (spare) 2:650 ohm for stable oscillation of 49MHz 3: 750 ohm for startup and stable oscillation of 24MHz

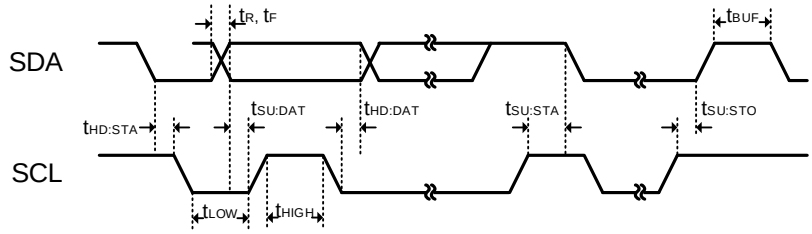
Start up sequence is shown in Figure *.

Internal LDO is controlled by the register (EN_BGR/EN_LDO) to generate the internal power supply. After load capacitance, series resister and drive current registers are set, oscillation is started controlled by EN_OSC register. Drive current can be reduced at stable oscillation.



I2C specifications

Symbol	Item	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD:STA}$	Hold time (repeat) start condition (The first clock pulse is generated after this period.)	0.6	-	us
t_{LOW}	SCL clock Low period	1.3	-	us
t_{HIGH}	SCL clock High period	0.6	-	us
$t_{SU:STA}$	Repeat start condition setup time	0.6	-	us
$t_{HD:DAT}$	Data hold time	0	-	us
$t_{SU:DAT}$	Data setup time	100	-	ns
tr	SDA signal and SCL signal rise time	-	300	ns
tf	SDA signal and SCL signal fall time	-	300	ns
$t_{SU:STO}$	Stop condition setup time	0.6	-	us
t_{BUF}	Bus free time between Stop and Start conditions	1.3	-	us
Cb	Capacitance load of each bus line	-	400	pF



Slave Address of CXD5247 Audio is 7'h1E.

Register Description

◆Power register list

No.	Category	Address	Register name	Application
1	(Power supply block) Output control registers	10h	EN_CTRL1	D/D converter and LDO enable control
		11h	EN_CTRL2	
		12h	LOAD_SW_CTRL1	LOAD_SW enable control
		13h	GPO_CTRL1	GPO0～7 Output control
		14h	GPO_CTRL2	
		15h	VO_DDC_ANA	Sets the DDC_ANA output voltage
		16h	VO_DDC_CORE	Sets the DDC_CORE output voltage
		17h	VO_LDO_EMMC/PERI	Sets the LDO_EMMC/PERI output voltage
		18h	VO_LDO_ANA	Sets the LDO_ANA output voltage
2	(Power supply block) Power supply operating mode setting registers	20h	CONFIG_DDC_IO_1	Sets the DDC_IO operating mode
		21h	CONFIG_DDC_IO_2	
		22h	CONFIG_DDC_IO_3	
		23h	CONFIG_DDC_CORE_1	Sets the DDC_CORE operating mode
		24h	CONFIG_DDC_CORE_2	
		25h	CONFIG_DDC_CORE_3	
		26h	CONFIG_DDC_ANA_1	Sets the DDC_ANA operating mode
		27h	CONFIG_DDC_ANA_2	
		28h	CONFIG_DDC_ANA_3	
		29h	CONFIG_LDO	Sets the LDO operating mode
3	(Power supply block) Status control registers	30h	WKUP_STATUS	Stores the start-up factor
		31h	WKUP_STATUS_CLR	Clears the start-up factor_STATUS
		32h	WKUP_TRG	Stores the start-up factor output trigger
		33h	WKUP_TRG_CLR	Clears the start-up factor output trigger
		34h	INTO_STATUS	Stores the INT_OUT output trigger
		35h	INTO_STATUS_CLR	Clears the INT_OUT output trigger
		36h	VMIN_DDC_CORE	Holds the setting voltage before WDT issues
		37h	CMD_CTRL	Stores the I2C control command
		38h	CONFIG_INT_WKUP	Sets the xINT_WKUP condition
		39h	CONFIG_WDT	WDT setting
		3Ah	SET_DWN_PRE1	System operation lower limit voltage pre-notification voltage setting status
		3Bh	SET_DWN_PRE2	
		3Ch	SET_VSYS_ACT	Sets the system operating voltage
		3Dh	LRQ_SET_VSYS	Reflects the 3Ah to 3Ch settings

No.	Category	Address	Register name	Application
		3Eh	LRQ_VSYS_STATE	VSYS setting status
		3Fh	INT_SEL	Selects the INT_OUT output
4	(Power supply block) RTC control registers	40h	CURT_PRE_CNTR_1	Stores the current time
		41h	CURT_PRE_CNTR_2	
		42h	CURT_POST_CNTR_1	
		43h	CURT_POST_CNTR_2	
		44h	CURT_POST_CNTR_3	
		45h	CURT_POST_CNTR_4	
		46h	RRQ_TIME	Current time read request
4	(Power supply block) RTC control registers	47h	SET_PRE_CNTR_1	Stores the set time to the counter
		48h	SET_PRE_CNTR_2	
		49h	SET_POST_CNTR_1	
		4Ah	SET_POST_CNTR_2	
		4Bh	SET_POST_CNTR_3	
		4Ch	SET_POST_CNTR_4	
		4Dh	LRQ_TIME	Set time load request to the counter
		4Eh	LRQ_OFST	Reflects the offset time
		4Fh	WKUP_PRE_CNTR_1	Sets the WakeUp time (absolute time, relative time)
		50h	WKUP_PRE_CNTR_2	
		51h	WKUP_POST_CNTR_1	
		52h	WKUP_POST_CNTR_2	
		53h	WKUP_POST_CNTR_3	
		54h	WKUP_POST_CNTR_4	
		55h	LRQ_WU	Reflects the WakeUp time registers
		56h	CONFIG_WKUP	Condition settings of WakeUp
		57h	CNTR_STOP	Enable control of RTC counter
5	(Power supply block) Interrupt output control registers	58h	ALM_PRE_CNTR_1	Sets the interrupt output alarm time (absolute time, relative time)
		59h	ALM_PRE_CNTR_2	
		5Ah	ALM_POST_CNTR_1	
		5Bh	ALM_POST_CNTR_2	
		5Ch	ALM_POST_CNTR_3	
		5Dh	ALM_POST_CNTR_4	
		5Eh	LRQ_ALM	Reflects the interrupt output alarm time setting registers
		5Fh	CONFIG_ALARM	Sets the alarm condition
		60h	RRQ_LRQ_STATUS	Time data status
6	(Power supply block) Information storage	61h	DATA_GPS1	Stores the GPS data
		62h	DATA_GPS2	

No.	Category	Address	Register name	Application
	registers	63h	DATA_GPS3	
		64h	DATA_GPS4	
		65h	DATA_GPS5	
		66h	DATA_GPS6	
		67h	DATA_GPS7	
		68h	DATA_GPS8	
		69h	DATA_GPS9	
		6Ah	DATA_GPS10	
		6Bh	DATA_GPS11	
		6Ch	DATA_GPS12	
		6Dh	DATA_GPS13	
		6Eh	DATA_GPS14	
		6Fh	DATA_GPS15	
		70h	DATA_GPS16	
		71h	DATA_FREE1	Stores the information required by the software side
		72h	DATA_FREE2	
		73h	DATA_FREE3	
		74h	DATA_FREE4	
7	(Charge block) Control registers	75h	CNT_CHG1	Battery voltage judgment and control registers
		76h	CNT_CHG2	
		77h	CNT_CHG3	
		78h	SET_T60_1	Battery temperature control registers
		79h	SET_T60_2	
		7Ah	SET_T45_1	
		7Bh	SET_T45_2	
		7Ch	SET_T10_1	
		7Dh	SET_T10_2	
		7Eh	SET_T0_1	
		7Fh	SET_T0_2	
		80h	CNT_USB1	USB charge control registers
		81h	CNT_USB2	
8	(AFE block) Control registers	82h	SET_AFE1	AFE operation setting registers
		83h	SET_AFE2	
		84h	SET_AFE3	
		85h	DATA_AFEV_1	Stores the AFE measurement data
		86h	DATA_AFEV_2	
		87h	DATA_AFEI_1	

No.	Category	Address	Register name	Application
		88h	DATA_AFEI_2	
		89h	DATA_AFET_1	
		8Ah	DATA_AFET_2	
		8Bh	LRQ_AFE	Reflects the AFE measurement data to the registers
		8Ch	LRQ_AFED_STATE	AFE data status
		8Dh	DATA_AFEI_OF1	Stores the DC offset data for AFE current measurement
		8Eh	DATA_AFEI_OF2	

* Note that addresses 90h and higher are assigned as test registers, and should not be used.

◆Audio register list

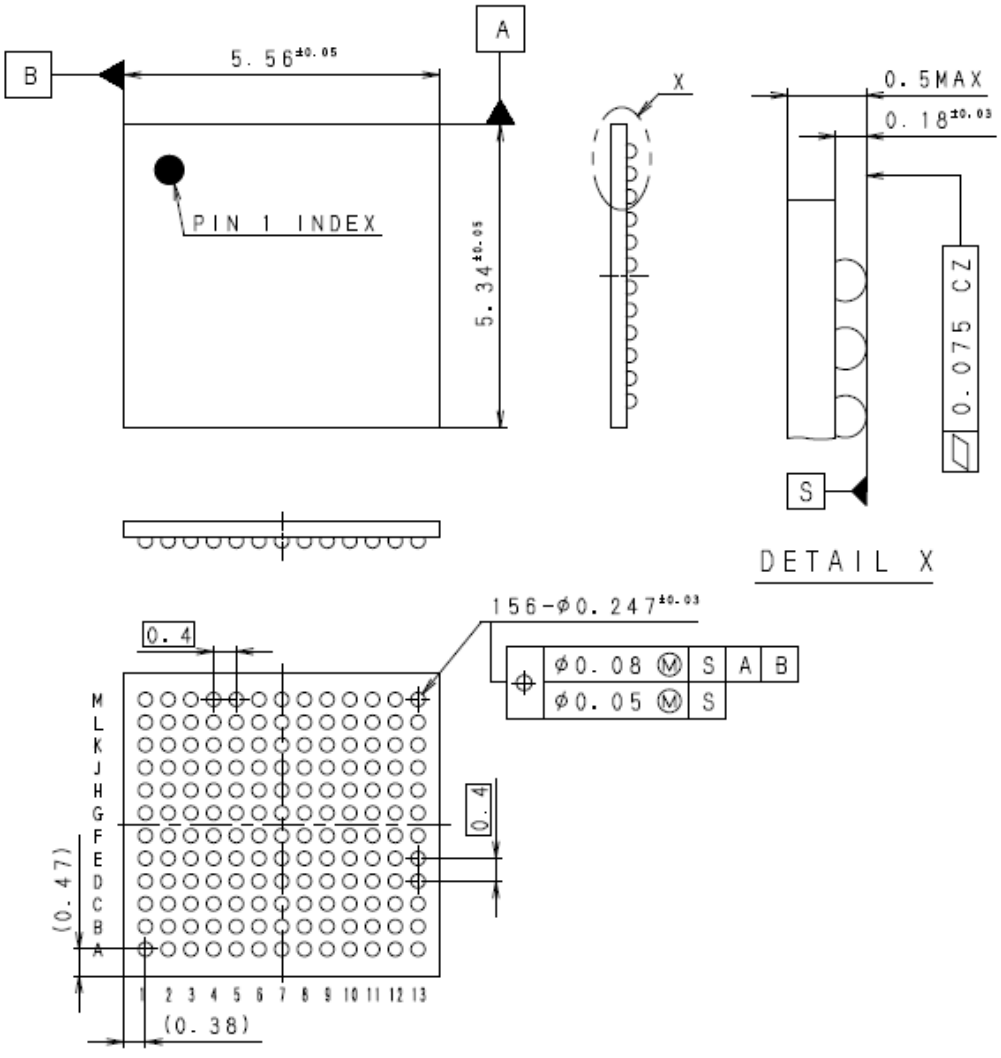
No.	Category	Bank	Address	Register name	Application
1	Audio REG Setting	00h	00h	Bank Setting	
		00h	01h	REG Freeze	
		00h	02h	REG Clear	
		00h	08h	Repeater Setting	
2	MIC Setting	00h	10h	MICIN Control	MIC AMP enable control
		00h	11h	MICGAIN_1	MIC AMP Ｇａｉｎ Setting
		00h	12h	MICGAIN_2	
		00h	13h	PGA GAIN_1	MIC pre AMP Ｇａｉｎ Setting
		00h	14h	PGA GAIN_2	
		00h	15h	ADC Control_1	MIC ADC enable control
		00h	16h	ADC Control_2	
		00h	17h	ADC Control_3	
		00h	18h	ADC Ref Control	MIC AMP setting
		00h	19h	BGR Control	Reference Circuit enable control
		00h	1Ah	MIC Bias Control_1	MIC Bias enable control
		00h	1Bh	MIC Bias Control_2	
		00h	1Ch	DMIC Control	DMIC Buffer enable control
		00h	1Fh	MIC LDO control	MIC LDO control
3	Speaker Setting	00h	20h	Speaker Control_1	Speaker enable control
		00h	21h	Speaker Control_2	
		00h	22h	Speaker loop control	Speaker Loop control
		00h	23h	SP LDO control	Speaker LDO enable control
		00h	24h	SP Delay control	Speaker Dead Time select
4	OSC Setting	00h	26h	MIC LDO control	MIC LDO enable control
		00h	27h	MIC control	MIC VM Exclude pin select
		00h	30h	XOSC control_1	XOSC enable control
		00h	31h	XOSC control_2	
		00h	33h	XOSC setting_1	XOSC Setting
		00h	34h	XOSC setting_2	
		00h	35h	XOSC setting_3	
		00h	36h	XOSC setting_4	
		00h	37h	XOSC setting_5	
		00h	38h	XOSC setting_6	
		00h	39h	XOSC setting_7	
		00h	80h	Logic I/O_1	LOGIC IO Setting

No.	Category	Bank	Address	Register name	Application
		00h	81h	Logic I/O_2	
		00h	82h	Logic I/O_3	
		00h	FDh	chipid	Chip ID

No.	Category	Bank	Address	Register name	Application
	Other Setting	01h	10h	CLK_SEL	CLK Setting
		01h	11h	CLK_EN	CLK enable control
		01h	12h	CLK_OUT_EN	
		01h	14h	SEL_CH12	Serializer setting
		01h	15h	SEL_CH34	
		01h	16h	SEL_CH56	
		01h	17h	SEL_CH78	
		01h	18h	SER_CTRL	
		01h	19h	STARTUP_CTRL_1	Startup control
		01h	1Ah	STARTUP_CTRL_2	
		01h	1Bh	PWM_OUTSEL	SMASTER PWM
		01h	1Ch	SMSTR_PWM_CTRL_1	
		01h	1Dh	SMSTR_PWM_CTRL_2	
		01h	1Fh	LOGIC_STATUS	Status monitor
		01h	20h	ADSEL	ADC Post-circuit control
		01h	21h	ADGAIN_1	
		01h	22h	ADGAIN_2	
		01h	23h	ADGAIN_3	
		01h	24h	ADGAIN_4	
		01h	25h	DITHER_CTRL	
		01h	26h	OFST_1	
		01h	27h	OFST_2	
		01h	28h	OFST_3	
		01h	29h	OFST_4	

Package Outline

156PIN XFBGA



PACKAGE STRUCTURE

SONY CODE	XFBGA-156S-311
JEITA CODE	S-XFBGA156-5.56x5.34-0.4
JEDEC CODE	————

PACKAGE MATERIAL	SI SUBSTRATE
TERMINAL MATERIAL	Sn-4.0Ag-0.5Cu
PACKAGE MASS	0.026g

Caution
The product of the WLCSP package should be used under light-shielded conditions.
Since the WLCSP package has a structure that a silocon wafer is exposed,
if light hits the wafer, the device may malfunction.

Notice

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Customer shall use the Products with the utmost concern for safety, and shall not use the Products for any purpose that may endanger life or physical wellbeing, or cause serious damage to property or the environment, either through normal use or malfunction.

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