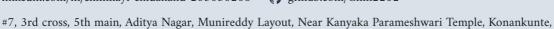
# Chinmayi C

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Bengaluru, 560108





	Education		
PES Institute of Technology and Management, B.E. in Electronics and Communication (8.5)  Narayana PU College, Pre-University Education(PCMB) (94.33%)  RMS International School, Primary, Higher-Secondary (87.9%)			12/2022 – 05/2026 Shimoga, India 04/2019 – 05/2021 Bengaluru Urban, India
- System Verilog	- Generative AI	- Python	
- Design Thinking	- Digital Marketing	- C/C++	
- Embedded Systems	- Robotics Process Automation	- LaTeX	
	Projects		
Learning Detection	Using AES Encryption and LSB Steganography with LSB + ML) enhancing data confidentiality and threa		02/2025 - Presen
, ( (	BOD + WILL CHIMATETING data confidentiality and three	at detection.	
AI Timing Violation Predictor For	,	it detection.	06/2025 – Presen
AI Timing Violation Predictor For A machine learning-powered tool de: RISC-V Processor Core	· VLSI Designs		
AI Timing Violation Predictor For A machine learning-powered tool des RISC-V Processor Core Developed and simulated a custom 3 GTKWave.  AI Driven Threat Detection System	VLSI Designs signed to predict timing violations in VLSI designs.  2-bit RISC-V Processor Core in Verilog using Icarus	Verilog and	06/2025 - Presen 05/2025 - Presen 08/2025 - 09/2025
AI Timing Violation Predictor For A machine learning-powered tool des RISC-V Processor Core Developed and simulated a custom 3 GTKWave.  AI Driven Threat Detection System Developed an AI-driven threat detect cybersecurity risks in real time.  VeriTB STUDIO	VLSI Designs signed to predict timing violations in VLSI designs. 2-bit RISC-V Processor Core in Verilog using Icarus	Verilog and	05/2025 – Presen
AI Timing Violation Predictor For A machine learning-powered tool des RISC-V Processor Core Developed and simulated a custom 3 GTKWave.  AI Driven Threat Detection System Developed an AI-driven threat detect cybersecurity risks in real time.  VeriTB STUDIO A GUI-based Verilog Testbench General Dino game using Hand Gesture results.	VLSI Designs signed to predict timing violations in VLSI designs.  2-bit RISC-V Processor Core in Verilog using Icarus  m tion system leveraging machine learning to identify an erator with Simulation, Assertions, and ZIP Export.	Verilog and nd mitigate	05/2025 - Presen 08/2025 - 09/2025

## **Courses and Certifications**

RTL-TO-GDSII Flow v6.0, Cadence

Generative AI, Microsoft LinkedIn 🛮

Introduction to Data Science, Infosys Springboard 🖸

Cybersecurity Awareness: Cybersecurity Terminology, LinkedIn

Cyber Security Job Simulation, Deloitte Australia

CyberSecurity Foundations, Microsoft LinkedIn 🖸

Robotics and Controls Job Simulation, Johnson and Johnson 🖸

Introduction to Microcontrollers & Coding [Centrado kit], Infosys Springboard

**Technology Job Simulation,** Deloitte Australia ☑

Introduction to Digital Marketing, Infosys Springboard

Cloud Infrastructure 2025 Certified Generative AI Professional, Oracle

#### **Tools**

## Cadence

Utilized for VLSI circuit design and verification in coursework and mini-projects.

## **UiPath Studio**

Applied to build process automation workflows during RPA training.

## Icarus Verilog and GTKWave

Used together for simulating and debugging Verilog modules in RISC-V Processor and testbench generator projects.

## **Keil MicroVision**

Employed for embedded C programming and debugging microcontrollers.

## **Python IDLE**

Used for coding and testing Python scripts in AES encryption, ML key generation, and AI-based security projects.

## Arduino UNO

Implemented in IoT sensor-based projects (DHT11, MQTT, Telegram integration).

## **Power Automate**

Gained hands-on exposure to automating workflows during UiPath training.

#### MATIah

Applied for simulation and implementation in cryptography and VLSI-related projects.

Trainings	
BOSCH, Trainee Attended a 2-day hands-on training program focused on industry practices and emerging technologies.	04/2025 - 04/2025
NXP Semiconductors, Trainee Attended an intensive hands-on workshop covering the fundamentals of RF circuit design, antenna theory, impedance matching, and simulation using industry-standard tools.	03/2025 – 03/2025 Shimoga, Karnataka
NXTWave, Participant Participated in the workshop by AI expert Mr. Abhinav Devaguptapu on 'AI for Students: Build your own Gen AI Model'	10/2024 – 10/2024 Online
Analog and Digital Circuit Simulation, Trainee Participated in a focused training session on analog and digital circuit simulation, covering design workflows, signal analysis, and performance evaluation.	09/2024 – 09/2024 Shimoga, Karnataka
Hackathons and Roles	
Anvesana Entrepreneurial Hub, Social media content writer Developed and managed professional content for social media platforms to promote club activities and enhance community engagement.	08/2023 – 10/2023 Shimoga, India
FOSS Hackathon 2024, Participant Contributed to open-source development by identifying and resolving issues in platforms such as FreeCAD gaining hands-on experience in collaborative problem-solving and software improvement.	07/2024 – 07/2024 Shimoga, India
Smart India Hackathon 2023, Participant Developed an AI-based legal documentation project; selected among top teams to present at the national finals	10/2023 – 12/2023 Kolkata, India

Declaration

**Chinmayi C** Bengaluru Urban

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