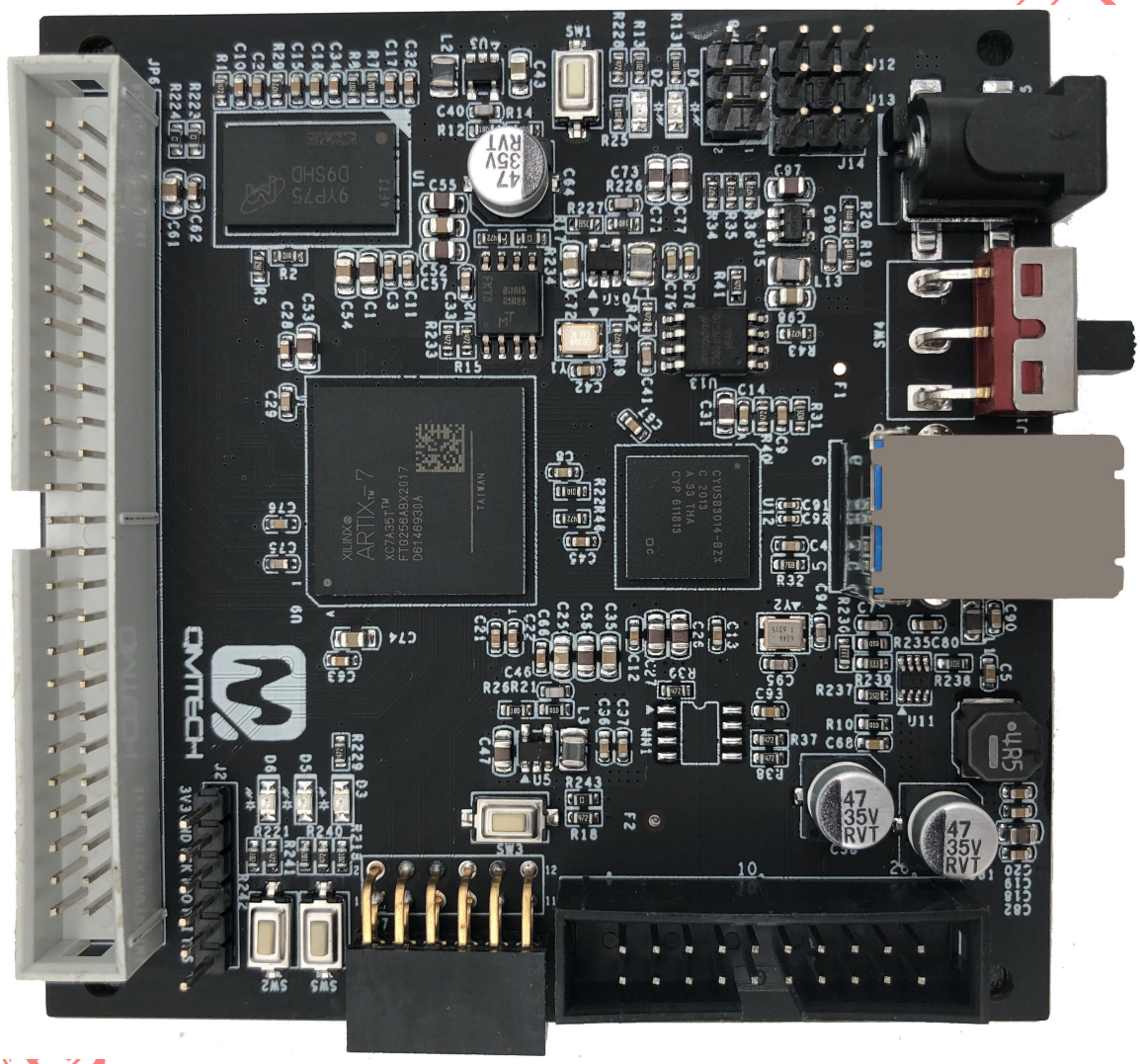
ARTIX-7 USB3.0 DEVELOPMENT BOARD

USER MANUAL(HARDWARE)



Preface

The QMTech® Artix-7 USB 3.0 development board uses Cypress's EZ-USB® FX3™ high-bandwidth USB 3.0 peripheral controller and Xilinx Artix®-7 device to demonstrate USB 3.0 SuperSpeed technology's high usable bandwidth and great power delivery. This user manual introduces the hardware design of the Artix-7 USB3.0 development board.

Table of Contents

1. Introduction

1.1 Kit Overview

The QMTech® Artix-7 USB3.0 development board provides high-bandwidth access to USB 3.0 data. It also integrates an USB 2.0 USB On-The-Go (OTG) controller enables applications in which FX3 may serve dual high-speed roles. Besides, the development board provides a Xilinx Artix-7 FPGA which could extend user peripherals like: ADC/DAC modules, cameras, LCD/HDMI display interfaces etc.

Below section lists the detailed info of the board parameters:

- On-Board USB 3.0 chip: Cypress's CYUSB3014;
- On-Board oscillator for USB 3.0 chip: 19.2MHz;
- CYUSB3014 Core: ARM926EJ@200MHz;
- CYUSB3014 Internal RAM: 512KB SRAM;
- On-Board SPI Flash for CYUSB3014: W25Q64, 8MB;
- On-Board 5.0V->3.3V DC/DC: MPS's MP2315;
- On-Board 3.3V->1.2V,1.5V,1.8V DC/DC: On-Semi's NCP1529;
- Development board provides 3 boot mode select headers, to control the CYUSB3014 boot from USB or external SPI Flash;
- Development board uses USB 3.0 Type-B male connector;
- On-Board FPGA: XC7A35T-1FTG256C;
- On-Board FPGA external crystal frequency: 50MHz;
- On-Board 16M bytes for user configuration code: MT28QL128A SPI Flash;
- On-Board 512MB Micron DDR3: MT41K256M16TW-107:P;
- Development board PCB size is: 83.8mm x 83.8mm;
- Default power source for board is: 1A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;

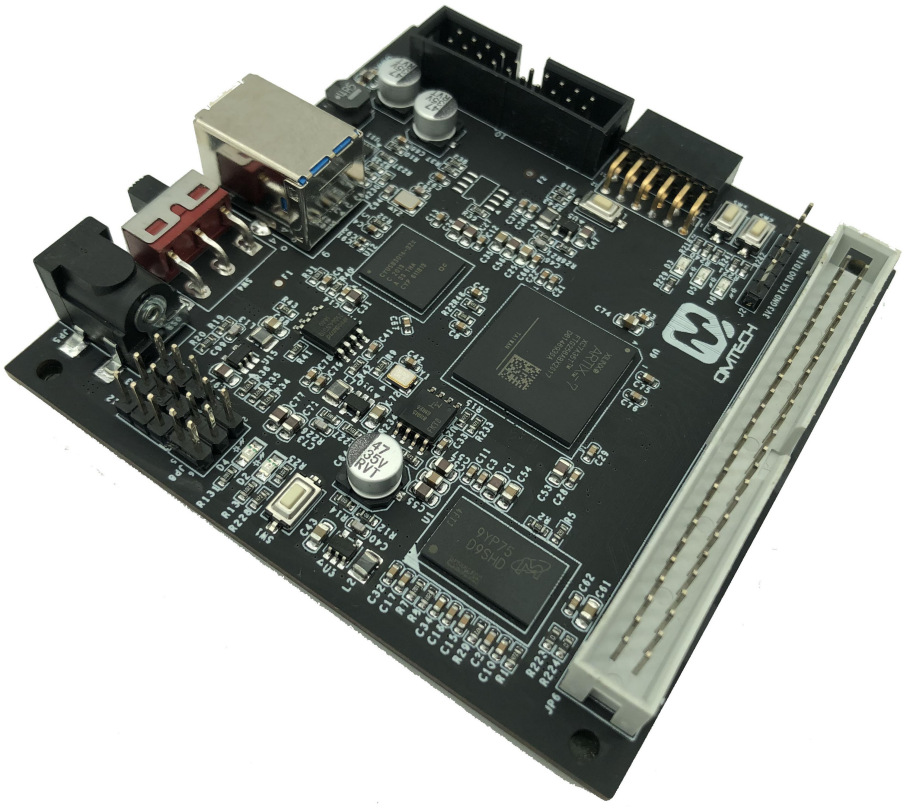


Figure 1-1. Side View of Development Board

2. Getting Started

Below image shows the detailed functional parts of the Artix-7 USB3.0 Development Board:

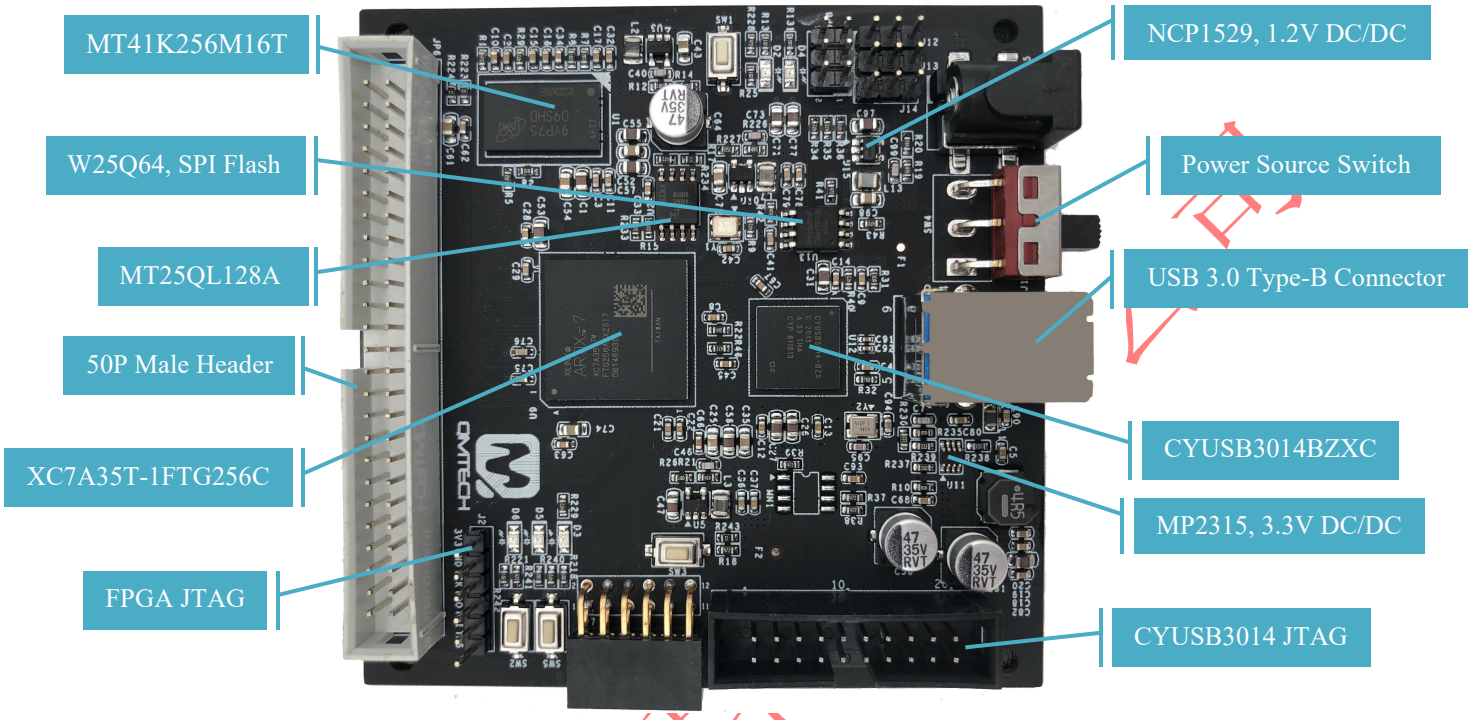


Figure 2-1. Top View of CYUSB3014 DB

Below image shows the development board's dimension: 83.8mm x 83.8mm：

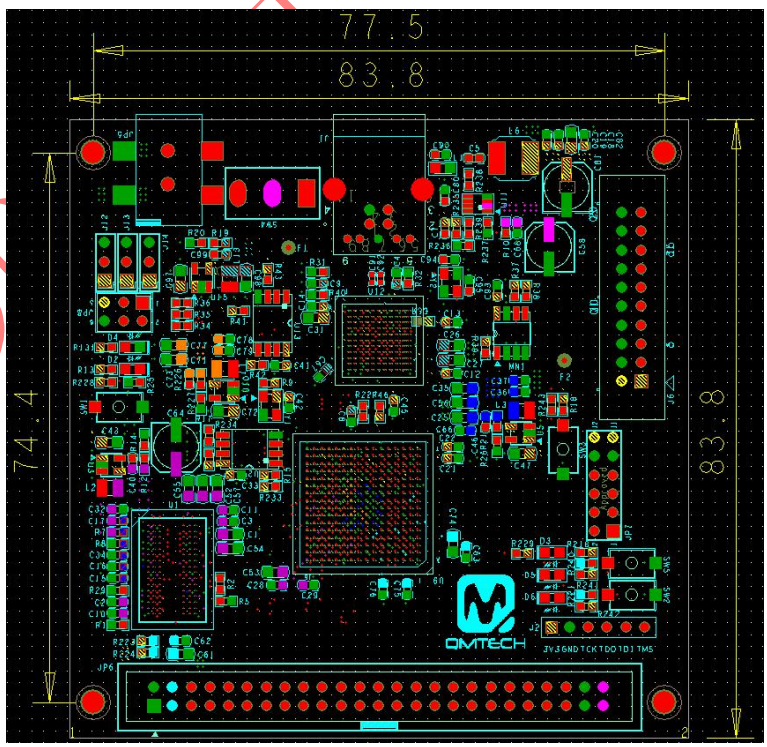


Figure 2-2. Dimension

2.2 Hardware Design

2.2.1 CYUSB3014 Power Supply

In default, the main power source for the development board is provided by the DC-050 header or USB 3.0 cable directly. The on-board high efficiency DC/DC MP2315 provides CYUSB3014 peripheral power source 3.3V and core power source 1.2V. It also provides the FPGA's BANK power source 3.3V/1.5V and core power source 1.0V.

Note: The on board LED D4 indicates the 3.3V supply status, it will be turned on when the 5V power supply is active.

Below image shows the hardware design of the CYUSB3014's power input pins. CYUSB3014 core supply 1.2V is regulated by On-Semi DC/DC chip NCP1529 which could output maximum 1A current.

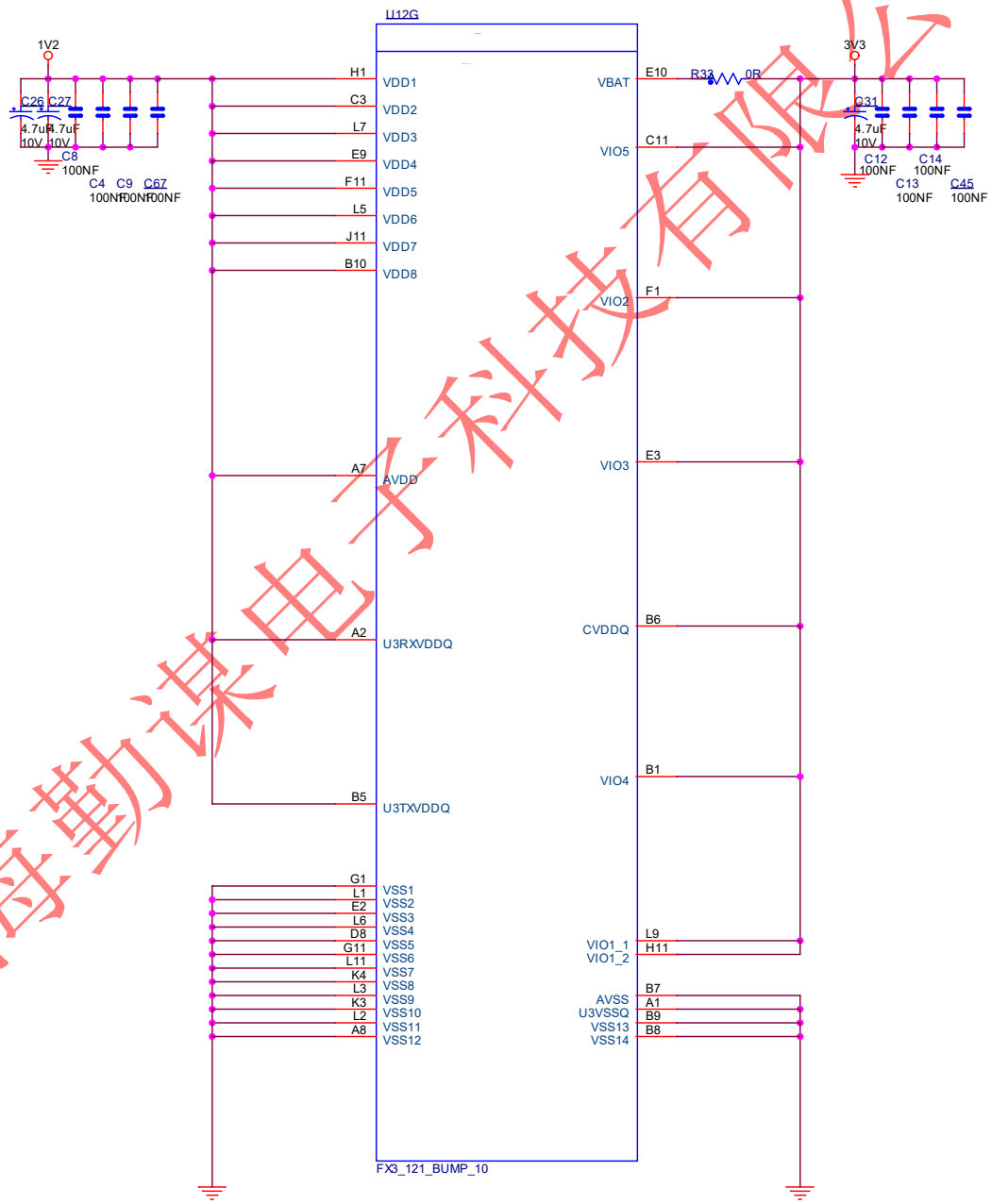


Figure 2-3. Power Supply for the CYUSB3014

Below image shows the 3.3V DC/DC and 1.2V DC/DC hardware design. The switch SW4 selects the power source for the board, either from USB3.0 cable or external 5V DC source.

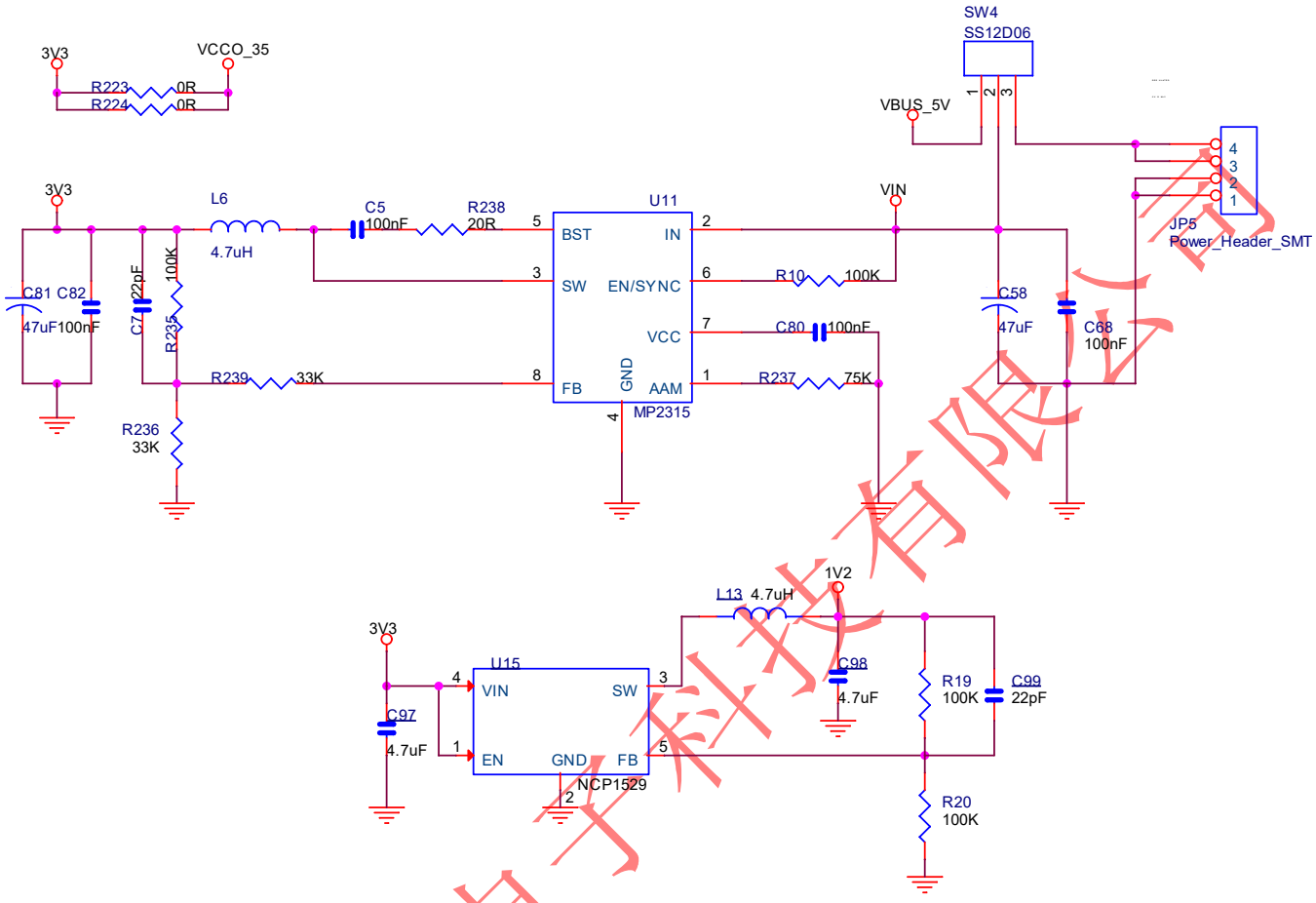


Figure 2-4. DC/DC Hardware Design

Below image shows the USB3.0 type-B header hardware design.

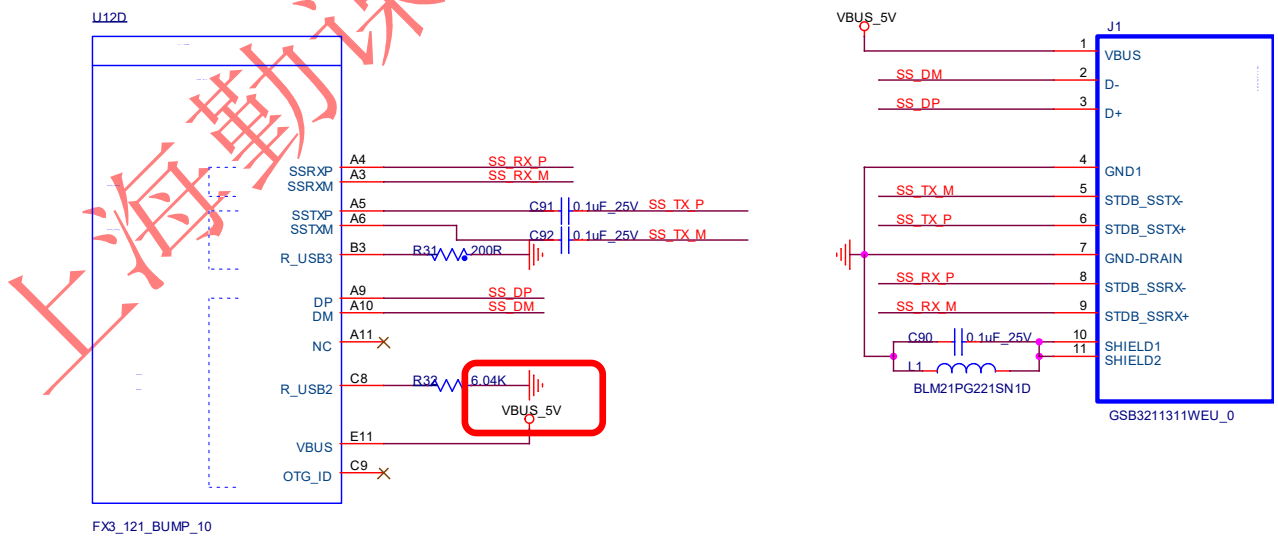


Figure 2-5. VUSB_5V Connection

2.2.2 CYUSB3014 Boot Mode Select

The CYUSB3014 could boot from external SPI Flash or USB directly. The boot mode selection could be controlled by these three PMODE[2:0] pins.

Table 2. FX3 Booting Options

PMODE[2:0][1]	Boot From
F00	Sync ADMux (16-bit)
F01	Async ADMux (16-bit)
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I^2C, On Failure, USB Boot is Enabled
1FF	I^2C only
0F1	SPI, On Failure, USB Boot is Enabled

Figure 2-6. PMODE Boot Selection

Below image shows the hardware design of the PMODE control pins. Users could customized their own boot options by configuring the jumpers' connection.

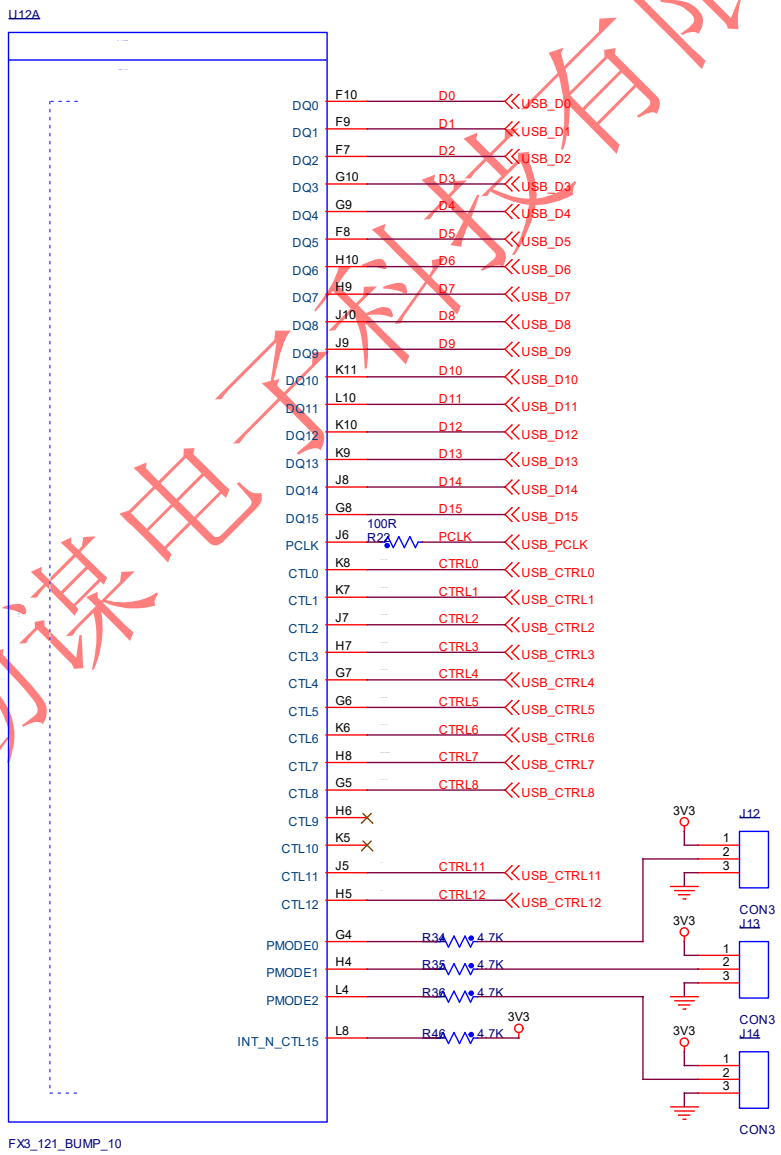


Figure 2-7. PMODE Hardware Design

The CYUSB3014 SPI interface is connected to a Winbond 8MB SPI Flash W25Q64. Below image shows the hardware design of the SPI flash:

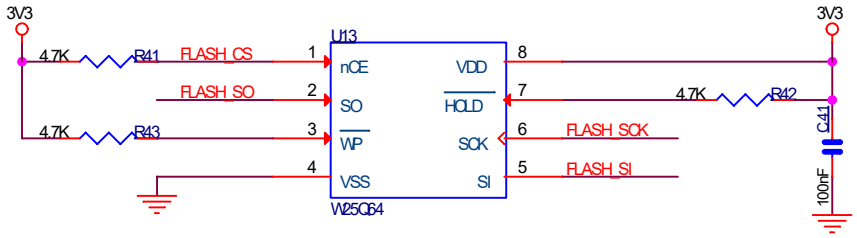


Figure 2-8. SPI Flash

The CYUSB3014 I2C interface is connected to an Atmel 16KB EEPROM AT24C128. In default, the EEPROM is not populated. Below image shows the hardware design of the EEPROM:

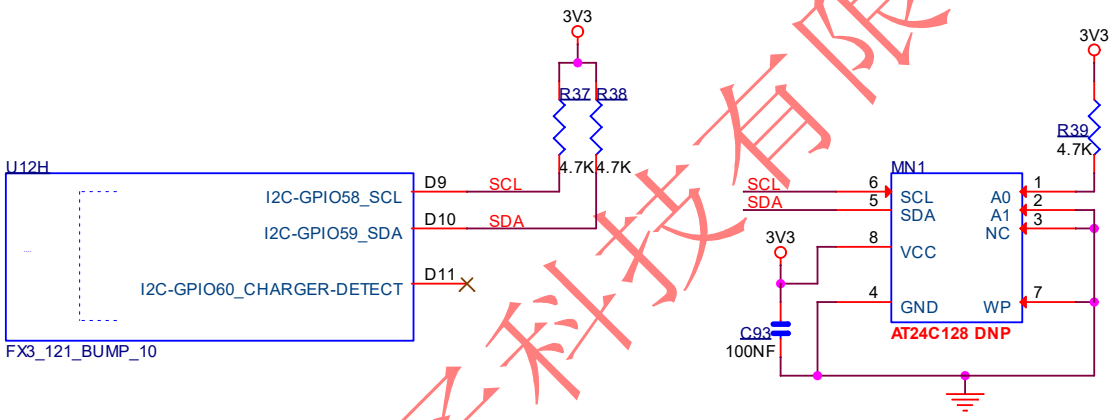


Figure 2-9. EEPROM

2.2.3 CYUSB3014 External Oscillator

The CYUSB3014 has an external 19.2MHz oscillator connected to XTALIN/XTAOUT pins. The input frequency of the oscillator is compatible to the setting of FSLC[2:0] pins. Below image shows the hardware design of the oscillator:

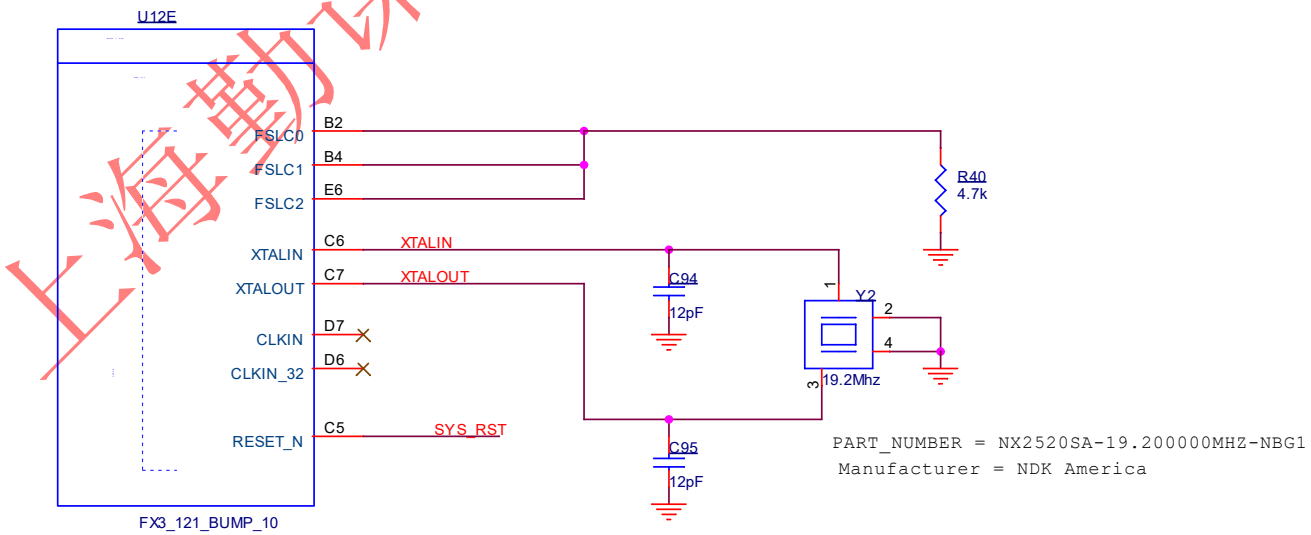


Figure 2-10. External 19.2MHz Oscillator

2.2.4 CYUSB3014 JTAG Interface

The CYUSB3014 Development Board provides one standard 20P JTAG interface. The JTAG header could be directly connected to debuggers like J-Link.

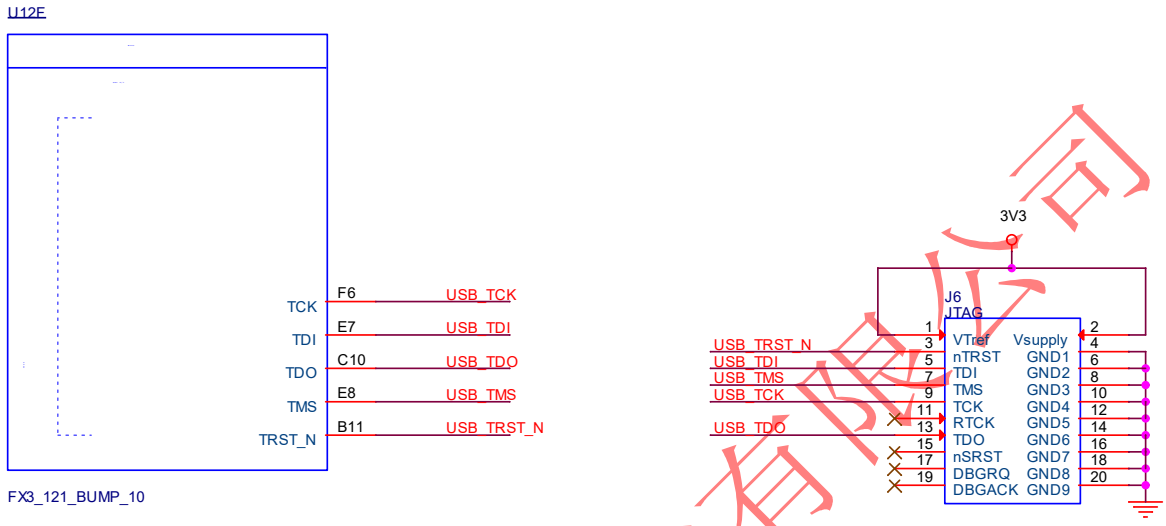


Figure 2-11. JTAG Interface

2.2.5 CYUSB3014 Reset Circuit

Below image shows the reset circuit of the CYUSB3014 Development Board. The reset signal is also connected to FPGA IO N2:

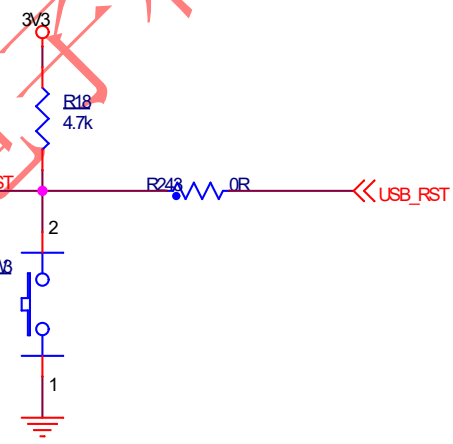


Figure 2-12. Reset Circuit

2.2.6 XC7A35T Power Supply

In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V. However, BANK35 IO's power level could be changed according to detailed custom requirement. There are two 0 ohm resisters could be removed: R223/R224, and instead the BANK35's power supply could be injected from 50P male header JP6. Detailed design refer to hardware schematic.

Note: FPGA core supply 1.0V is regulated by On-Semi DC/DC chip NCP1529 which could output maximum 1A current.

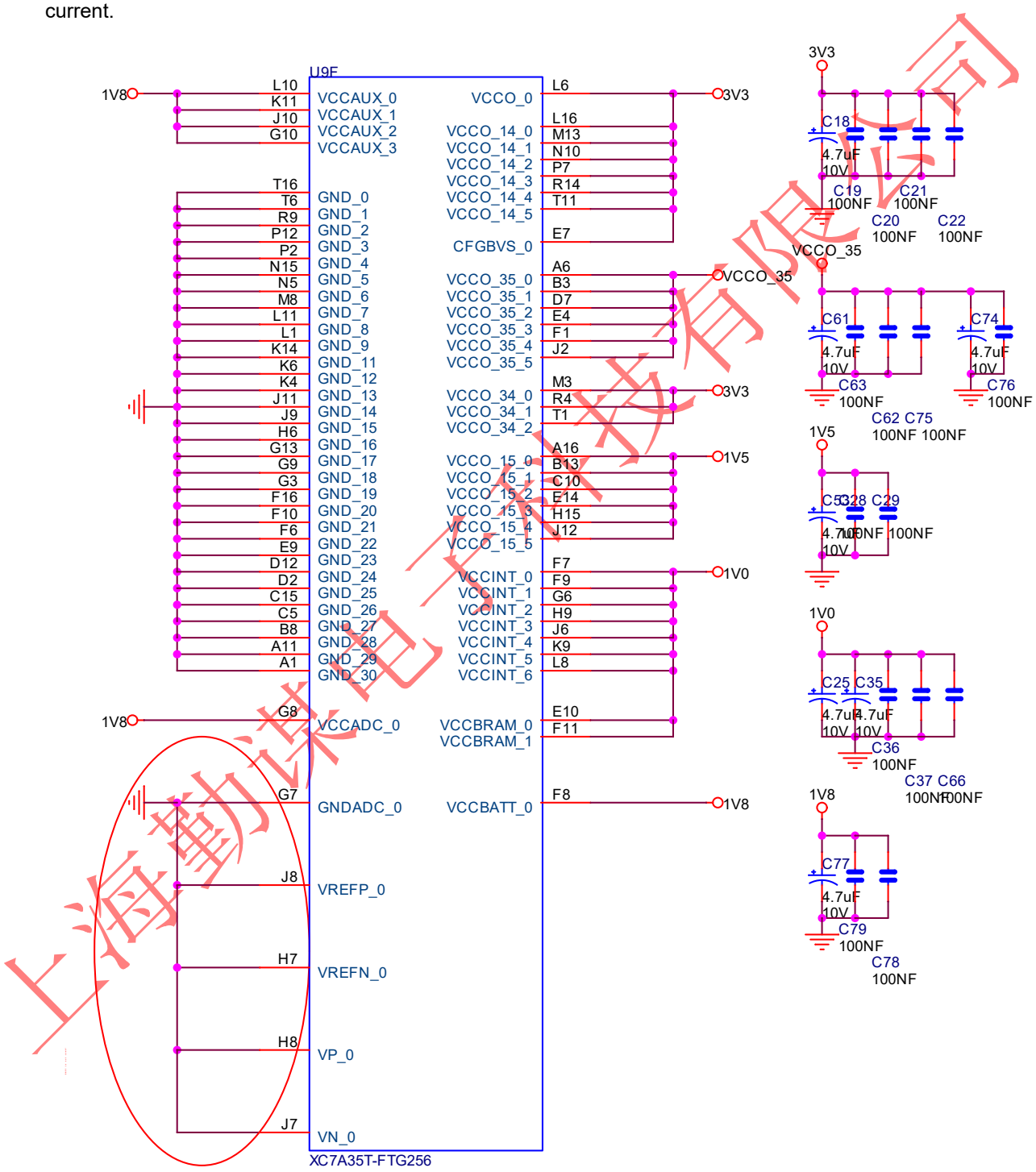


Figure 2-13. Power Supply for the FPGA

2.2.7 XC7A35T SPI Boot

In default, XC7A35T boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using MT25QL128 manufactured by Micron, with 128Mbit memory storage.

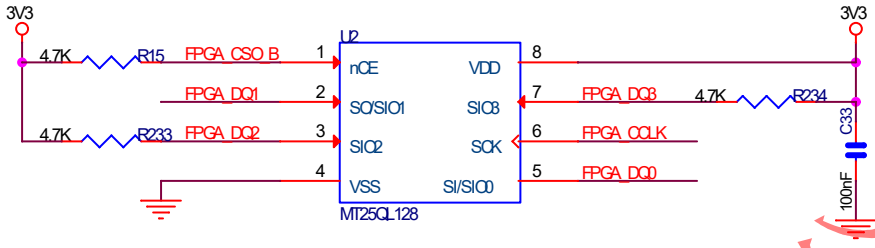


Figure 2-14. SPI Flash

The FPGA boot sequence setting M0:M1:M2 is configured as 1:0:0 which indicates FPGA will boot from SPI Flash after power on.

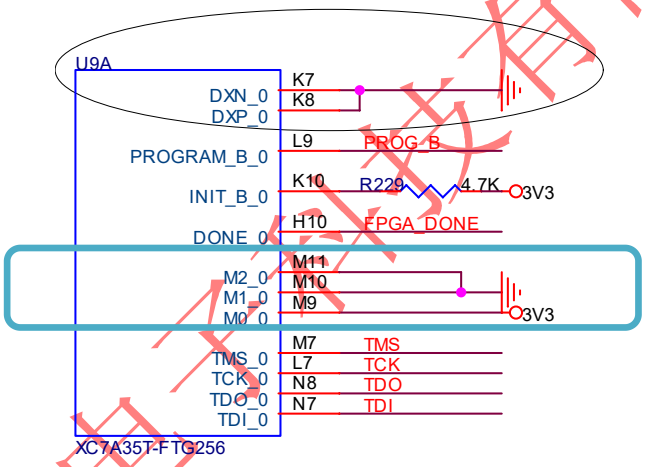


Figure 2-15. M0:M1 Hardware Settings

The LED D2 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D2 could be used as FPGA loading status indicator.

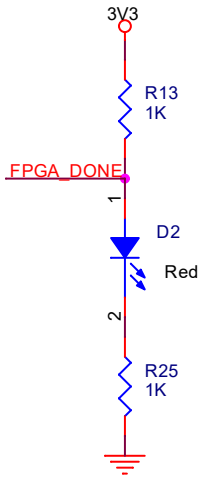


Figure 2-16. FPGA_DONE Status Indicator

2.2.8 XC7A35T DDR3 Memory

The development board has on board 16bit width data bus, 512MB memory size DDR3 MT41K256M16TW-107:P provided by Micron. Below image shows the detailed hardware design:

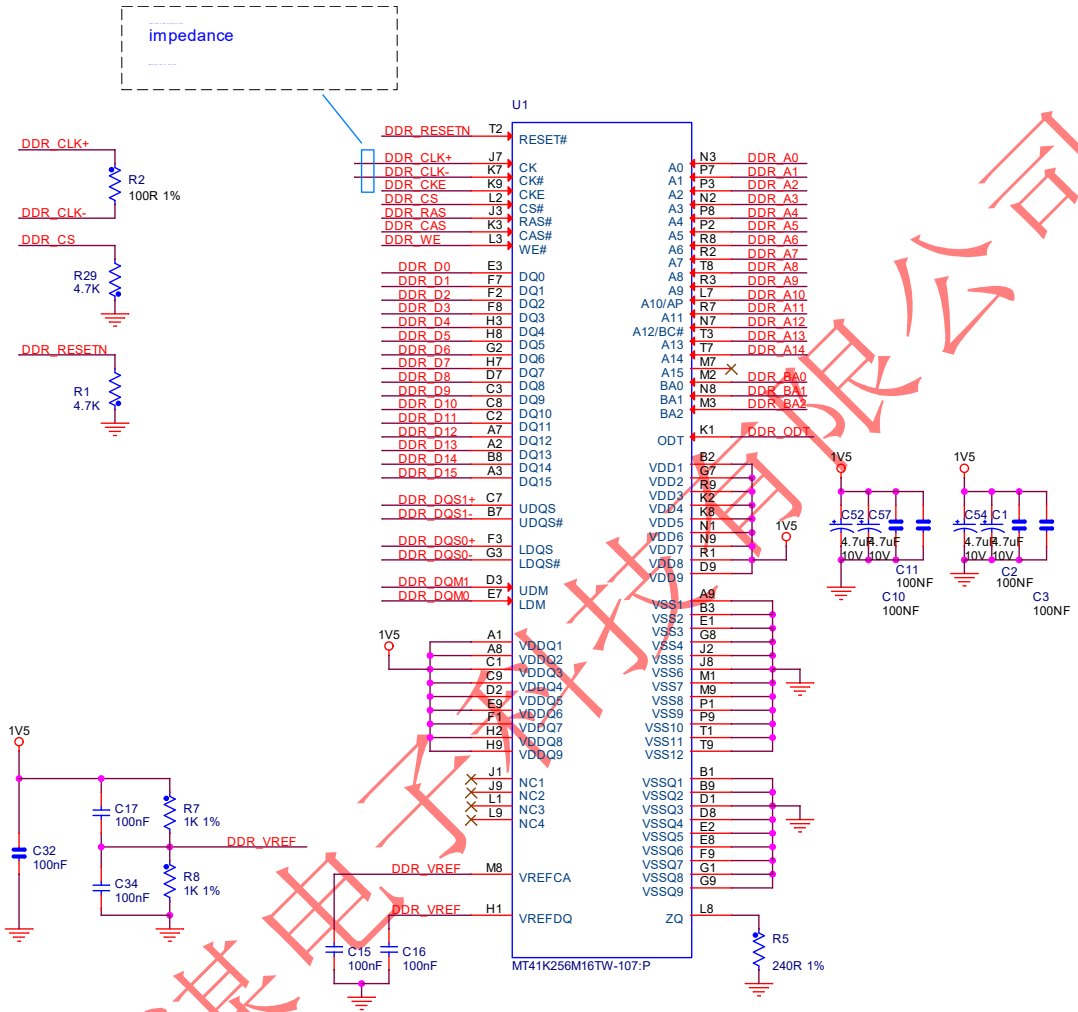


Figure 2-17. DDR3

2.2.9 XC7A35T System Clock

The FPGA chip XC7A35T has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

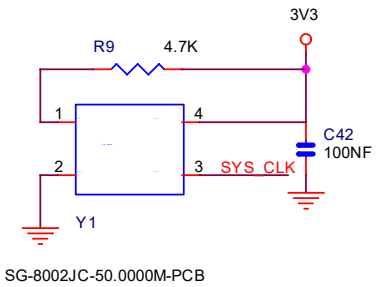


Figure 2-18. 50MHz System Clock

2.2.10 XC7A35T JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

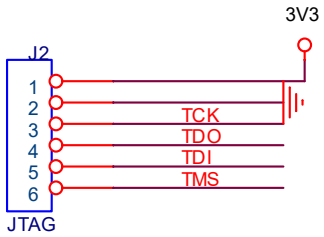


Figure 2-19. JTAG Port

2.2.11 XC7A35T User LEDs

Below image shows 3 user LEDs and one 3.3V power supply indicator:

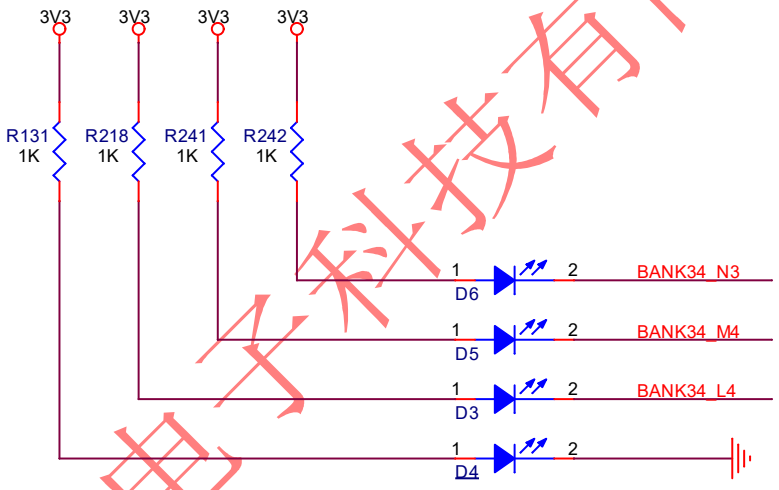


Figure 2-20. LEDs

2.2.12 XC7A35T User Keys

Below image shows the PROGRAM_B key and two user keys:

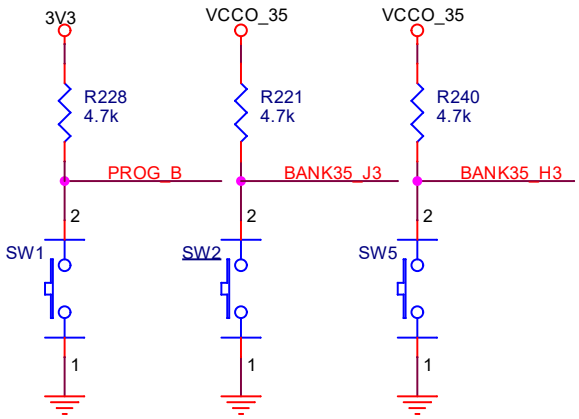


Figure 2-21. Keys

2.2.13 GPIF interface to FPGA

Below image shows the hardware connection between the CYUSB3014 and the XC7A35T:

Figure 2-22. GPIF Connection

3. Reference

[1] EZ-USB FX3 SuperSpeed USB Controller.pdf
[2] MP2359.pdf
[3] NCP1529-D.PDF
[4] W25Q64.pdf
[5] Atmel-8734-SEEPROM-AT24C128C-Datasheet.pdf
[6] ug470_7Series_Config.pdf
[7] ds181_Artix_7_Data_Sheet.pdf
[8] ug475_7Series_Pkg_Pinout.pdf
[9] MT25QL128A.pdf
[10] MT41K256M16TW-107:P .pdf
[11] MP2315.pdf

4. Revision

Doc. Rev.	Date	Comments
0.1	07/02/2020	Initial Version.
1.0	07/15/2020	V1.0 Formal Release.