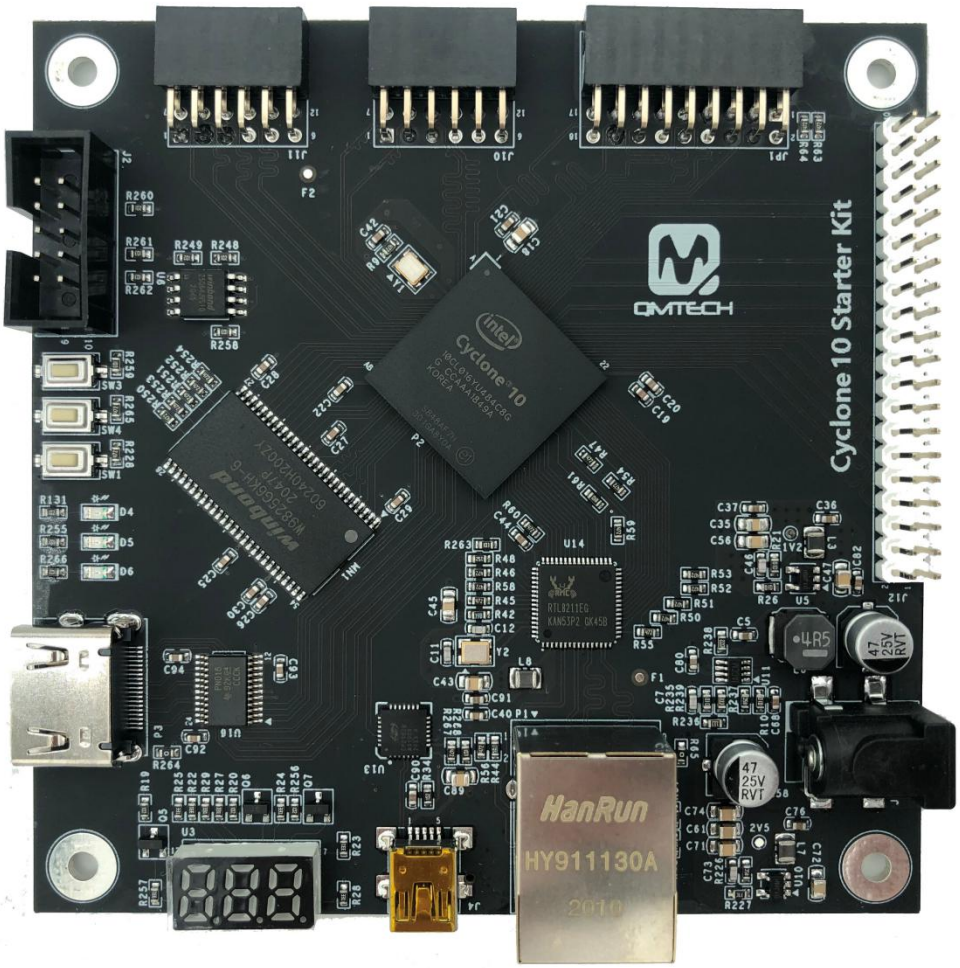
QMTECH CYCLONE10 STARTER KIT

USER MANUAL



Preface

The QMTech® Cyclone 10 Starter Kit uses Intel® (Altera) 10CL016 device to demonstrate the industry's lowest system cost and power, along with performance levels that make the device family ideal for differentiating your high-volume applications. All Intel® Cyclone® 10 LP FPGAs require only two core power supplies for operation, simplifying your power distribution network and saving you board costs, board space, and design time. The flexibility of the Intel® Cyclone® 10 LP FPGA enables you to design in a smaller, lower cost device, lowering your total system costs.

Users could visit QMTECH official website from here: http://www.chinaqmtech.com/

Table of Contents

1. QMTECH Cyclone 10 Starter Kit Introduction

1.1 Kit Overview

The Cyclone 10 Starter Kit provides several user interfaces to meet different customer needs. Below section lists the detailed info of these user interfaces:

- USB to UART Serial Port, by using Silicon Labs' CP2102N chip.
- HDMI display interface, by using TI's TPD12S016;
- GMII ethernet interface, by using Realtek's RTL8211EG chip;
- CMOS/CCD camera interface, by using 18pin female header;
- Two Digilent PMOD standard compatible female headers;
- 7-SEG LEDs for user info display;

1.2 Cyclone 10 Starter Kit Top View

Below figure shows the top view of Cyclone 10 Starter Kit. The development board's dimension is 99.6mm x 99.6mm. Below images shows the detailed functional parts of this kit.

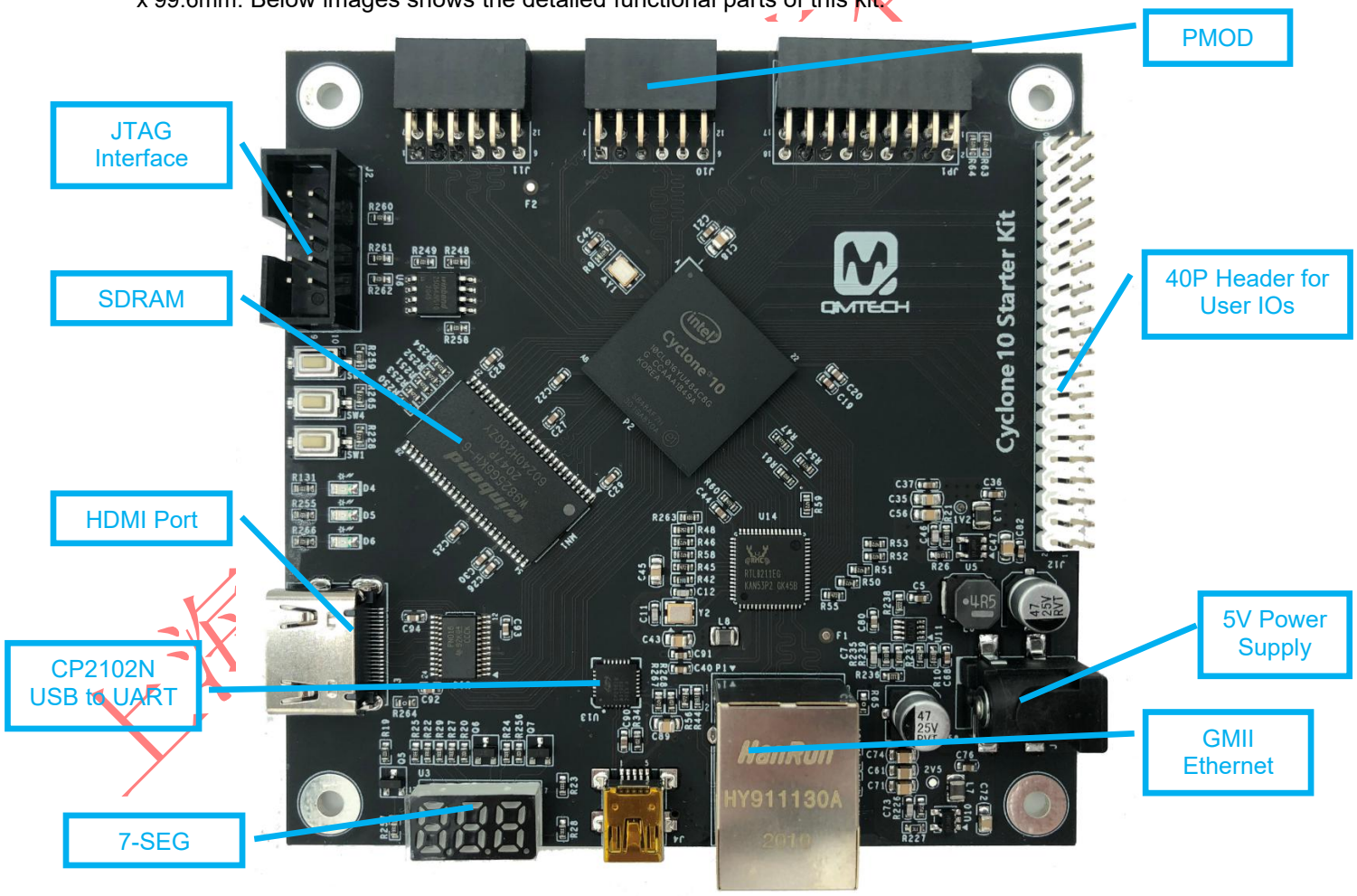


Figure 1-1. Cyclone 10 Starter Kit Top View

2. Experiment (1): USB to Serial Port

The CP2102N is a USB 2.0 to serial port bridge chip designed by Silicon Labs. The CP2102N includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components are required for development. Below figure shows the hardware design of CP2102N on the Cyclone 10 Starter Kit.

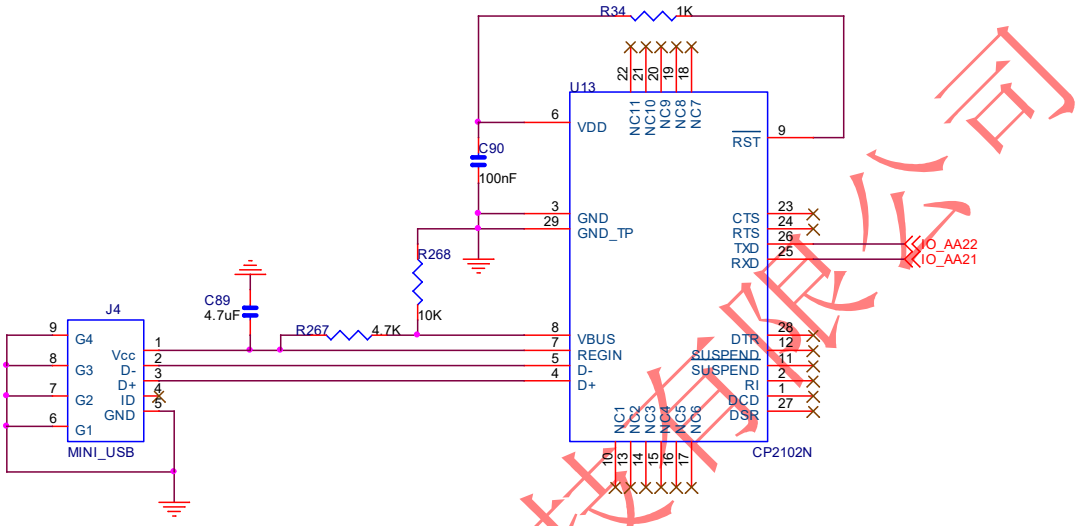
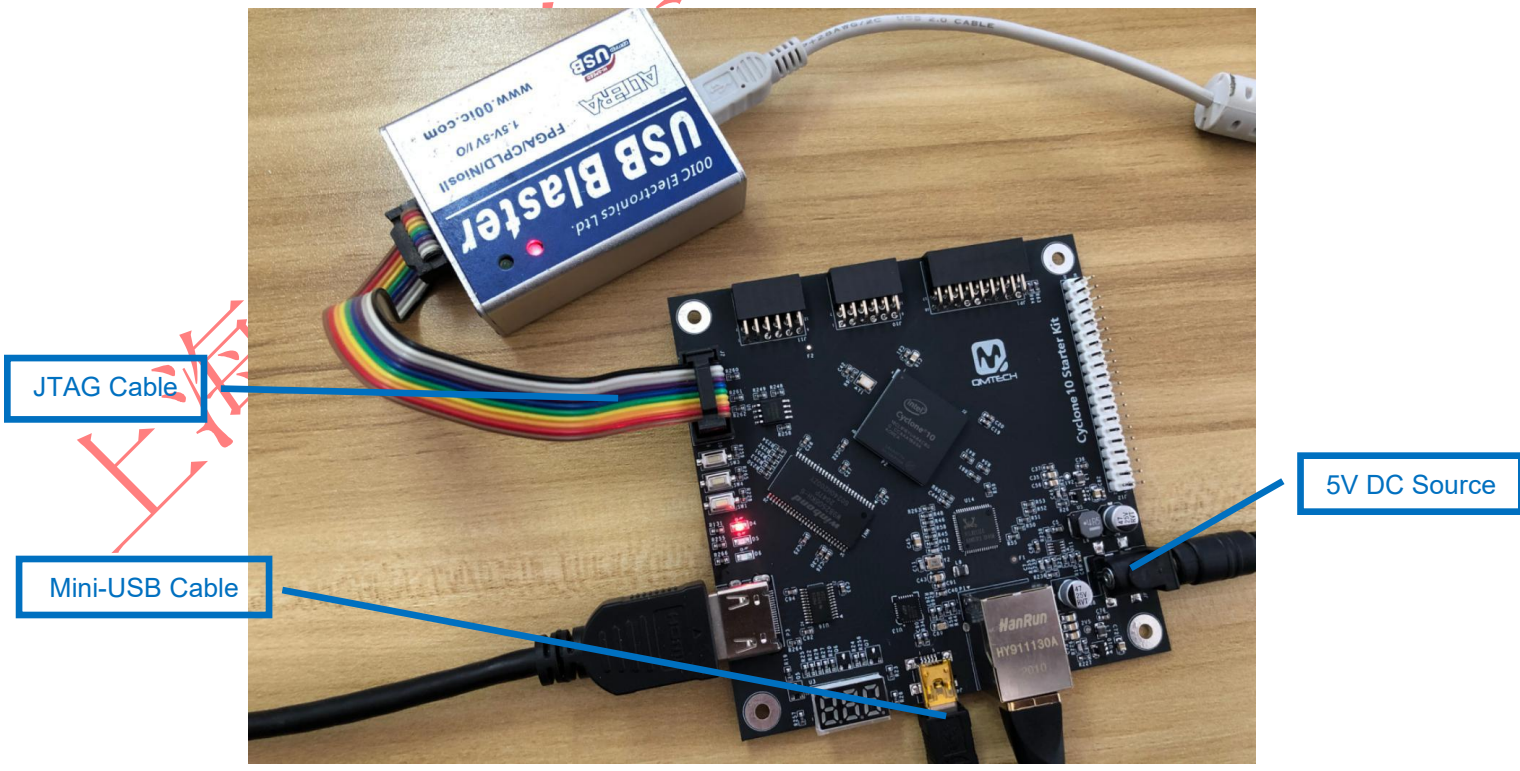


Figure 2-1. CP2102 Hardware Design

Before start to test the CP2102N's USB to UART serial communication function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to development board's JTAG interface. Then power on the development kit with 5V DC power source and plug the Mini-USB cable in the board, below figure shows an example hardware setup:



All the test examples are developed in the Quartus II 18.1environment. Open the CP2102N test project located in this release folder: /Software/Project05_CP2102N_UART. Below figure shows the example project of **uart_top**:

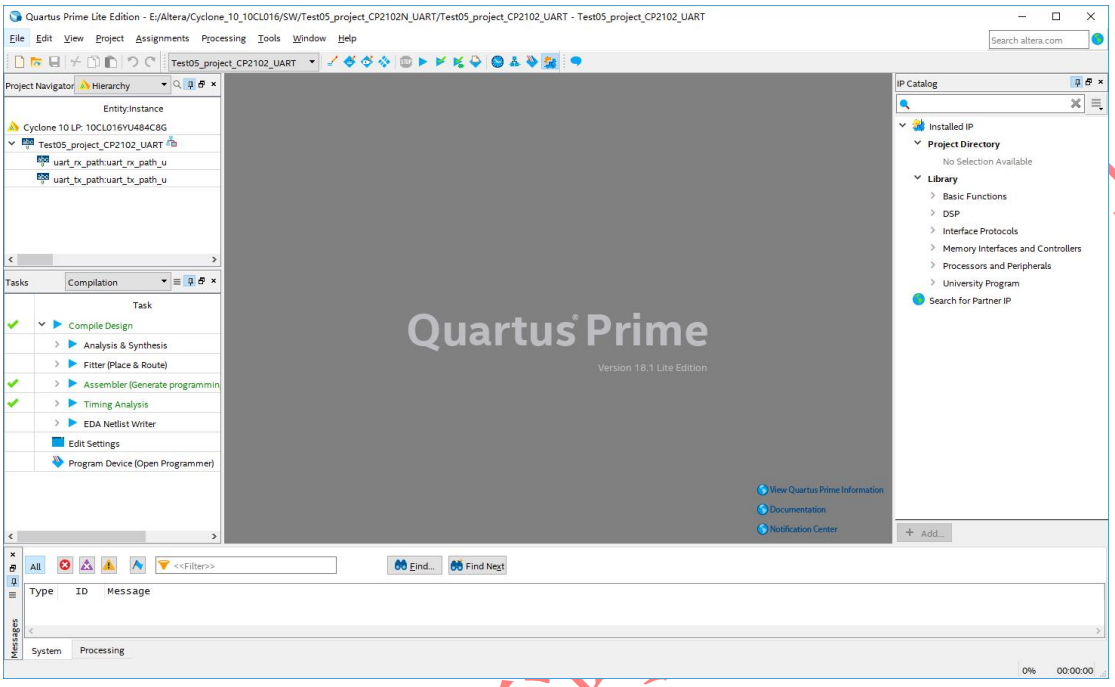


Figure 2-2. CP2102N UART Communication Test Example

In this example project, the default communication parameters are: 9600bps, 8 data bit, No Parity Check, 1 stop bit. If users want to test other communication parameters, change the source code accordingly.

uart_rx_path.v

```
`timescale 1ns / 1ps

module uart_rx_path(
    input clk_i,
    input uart_rx_i,

    output [7:0] uart_rx_data_o,
    output uart_rx_done,
    output baud_bps_tb          //for simulation
    );

parameter [12:0] BAUD_DIV     = 13'd5208;   //波特率时钟，9600bps，50Mhz/9600=5208
parameter [12:0] BAUD_DIV_CAP = 13'd2604;   //波特率时钟中间采样点，50Mhz/9600/2=2604

reg [12:0] baud_div=0;                      //波特率设置计数器
reg baud_bps=0;                             //数据采样点信号
reg bps_start=0;                            //波特率启动标志
always@(posedge clk_i)
begin
    if(baud_div==BAUD_DIV_CAP)              //当波特率计数器计数到采样点时，产生采样信号baud_bps
```

uart_tx_path.v

```
`timescale 1ns / 1ps

module uart_tx_path(
    input clk_i,

    input [7:0] uart_tx_data_i,         //待发送数据
    input uart_tx_en_i,                 //发送发送使能信号

    output uart_tx_o
);

parameter BAUD_DIV     = 13'd5208;      //波特率时钟，9600bps，50Mhz/9600=5208，波特率可调
parameter BAUD_DIV_CAP = 13'd2604;      //波特率时钟中间采样点，50Mhz/9600/2=2604，波特率可调

reg [12:0] baud_div=0;                  //波特率设置计数器
reg baud_bps=0;                         //数据发送点信号,高有效
(* MARKDEBUG = "TRUE" *)reg [9:0] send_data=10'b1111111111;     //待发送数据寄存器，1bit起始信号+8bit有效信号+1bit结束信号
(* MARKDEBUG = "TRUE" *)reg [3:0] bit_num=0;                    //发送数据个数计数器
reg uart_send_flag=0;                   //数据发送标志位
reg uart_tx_o_r=1;                      //发送数据寄存器，初始状态位高
```

After the CP2102N communication test project correctly synthesized, implemented and generated *.sof file, users could use Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.

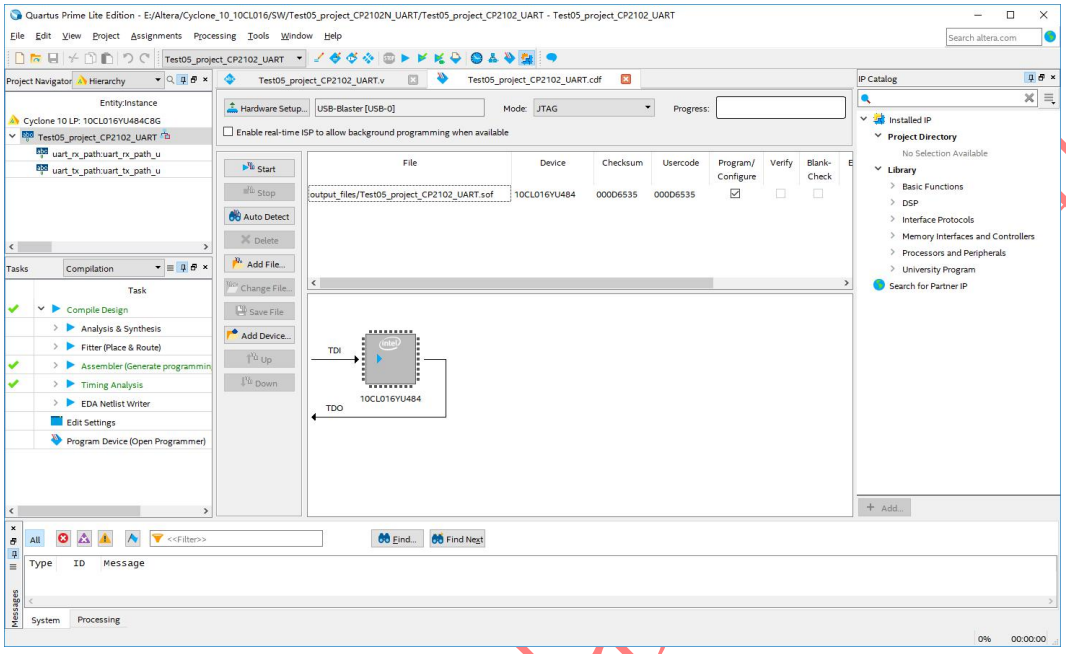


Figure 2-3. Program *.sof File

The CP2102N example test project's main functionality is performing an UART loopback communication. The FPGA program will send the received UART data back to the PC. Below figure shows user employees some PC based UART test tool to send data to FPGA: *http://www.cmsoft.cn QQ:10865600*. After a short while the PC UART test tool will receive the same data stream from FPGA, which means the CP2102N loopback test program is running correctly.

Figure 2-4. UART Loopback Test

3. Experiment (2): HDMI Displays

Transition Minimized Differential Signaling (TMDS) is used for transmitting video data over the High-Definition Multimedia Interface (HDMI). The Cyclone10 Starter Kit uses TI's TPD12S016 chip, which is a single-chip High Definition Multimedia Interface (HDMI) device with auto-direction sensing I2C voltage level shift buffers, a load switch, and integrated low capacitance high-speed electrostatic discharge (ESD) transient voltage suppression (TVS) protection diodes. Below image shows the hardware design.

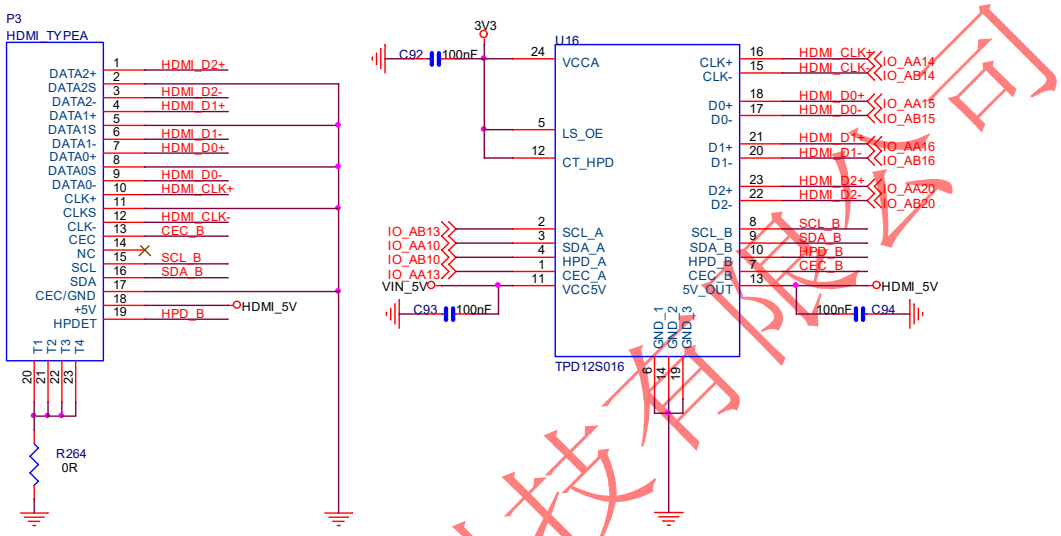
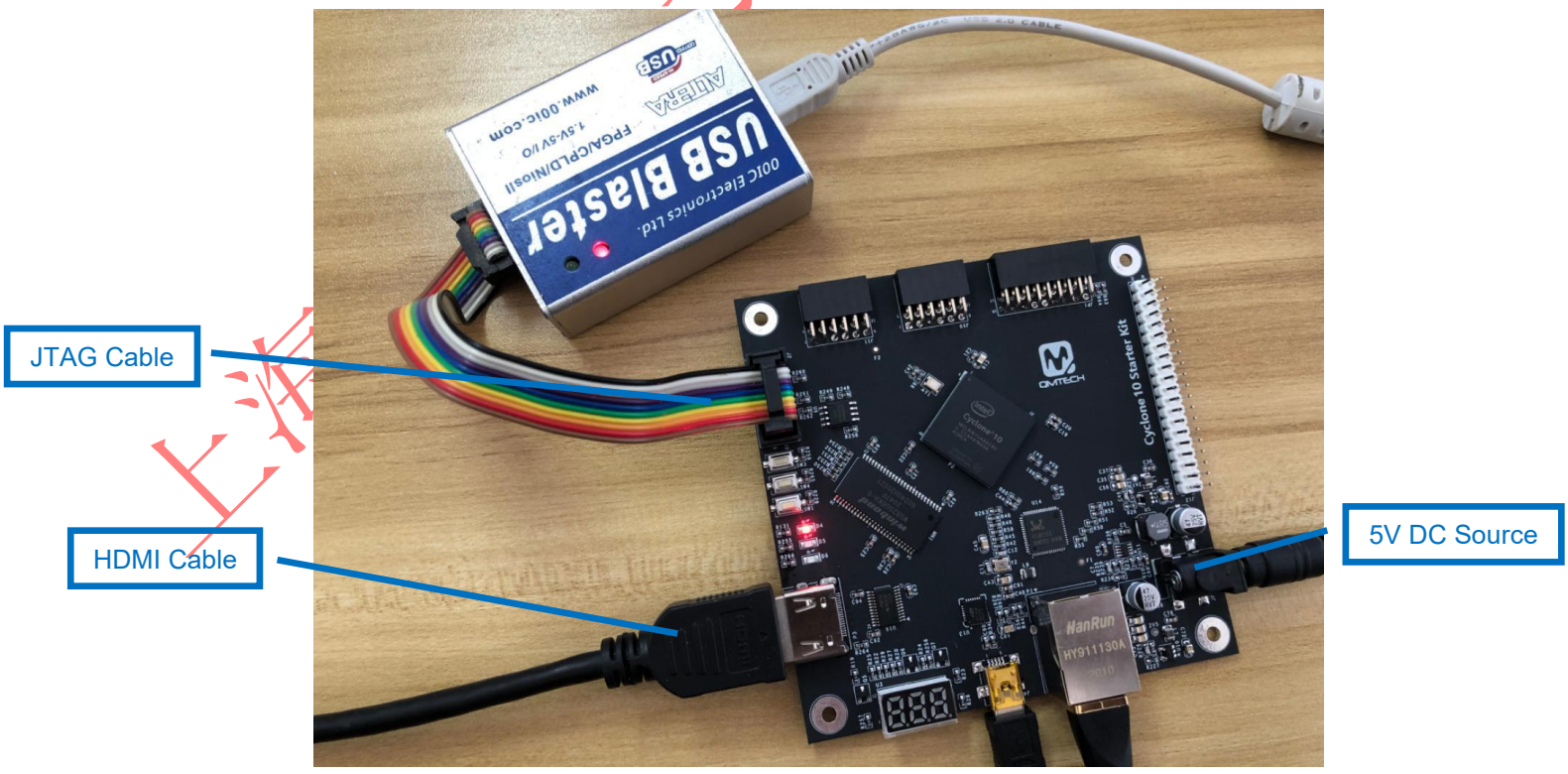


Figure 3-1. HDMI Display Hardware Designs

Before start to test the HDMI display function, make sure all the hardware connections of the starter kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to Cyclone 10 Starter Kit's JTAG interface. Then power on the development kit with 5V DC power source and the HDMI cable shall also be plugged in the board, below figure shows an example hardware setup:



Open the HDMI test project located in this release folder: /Software/Test13_project_HDMI. Below figure shows the example project of **HDMI_test**:

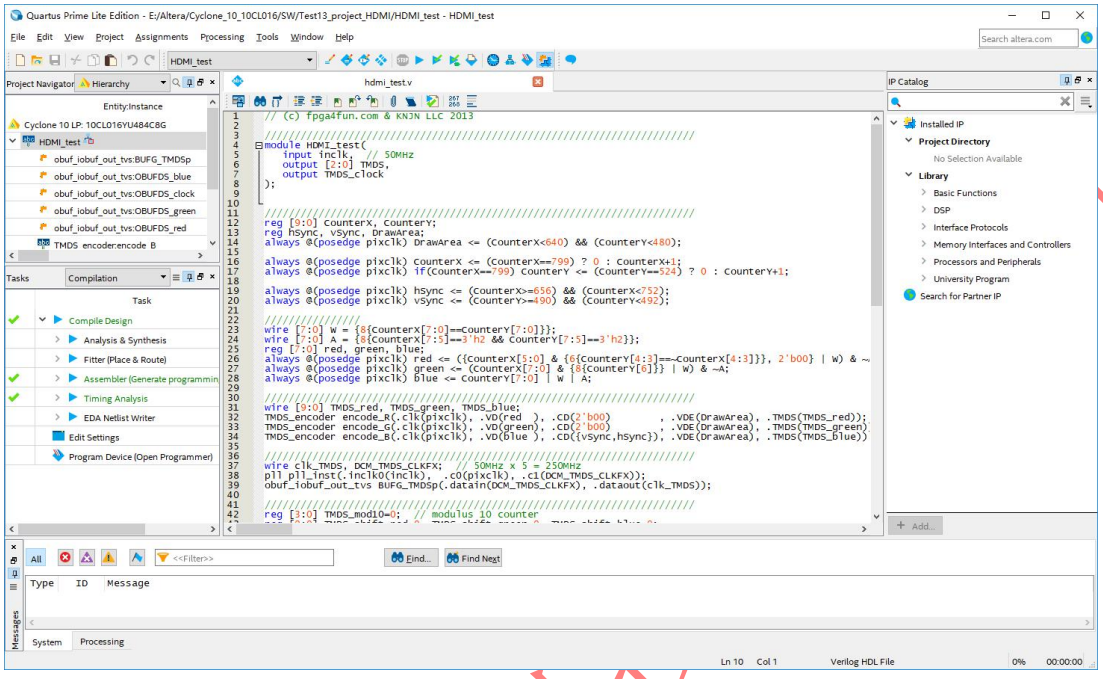


Figure 3-2. HDMI Display Function Test

After the HDMI display test project correctly synthesized, implemented and generated *.sof file, users could use Altera Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.

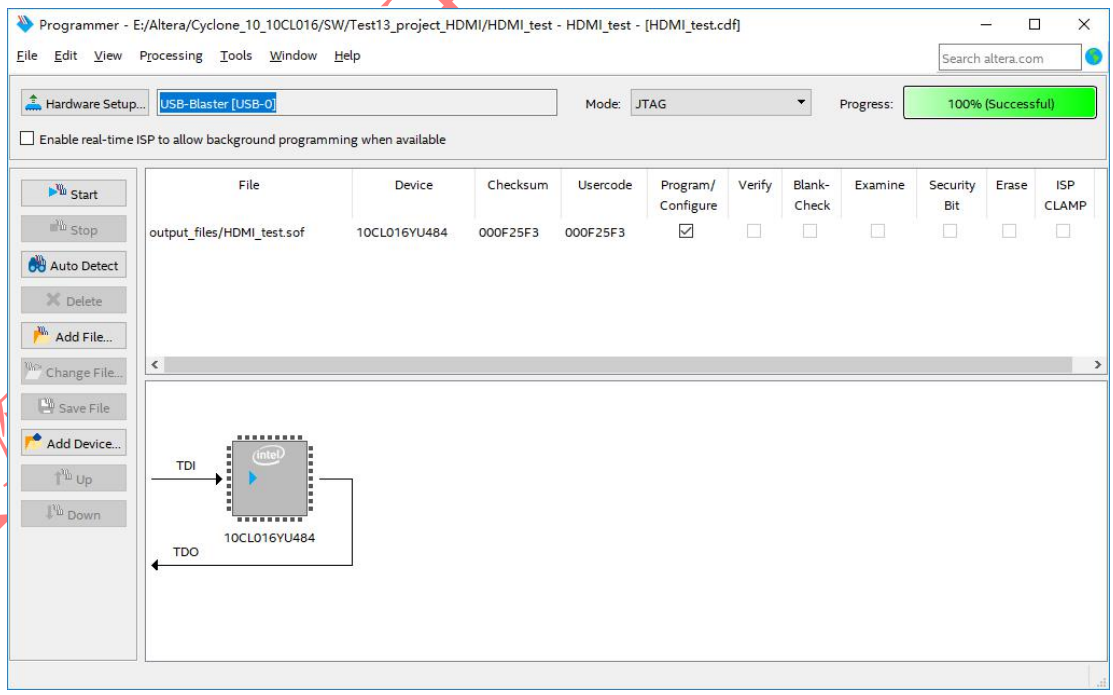


Figure 3-3. Program FPGA

After the FPGA correctly loaded the HDMI_test.sof file and the HDMI monitor will display color pattern. Below image shows the example color pattern.

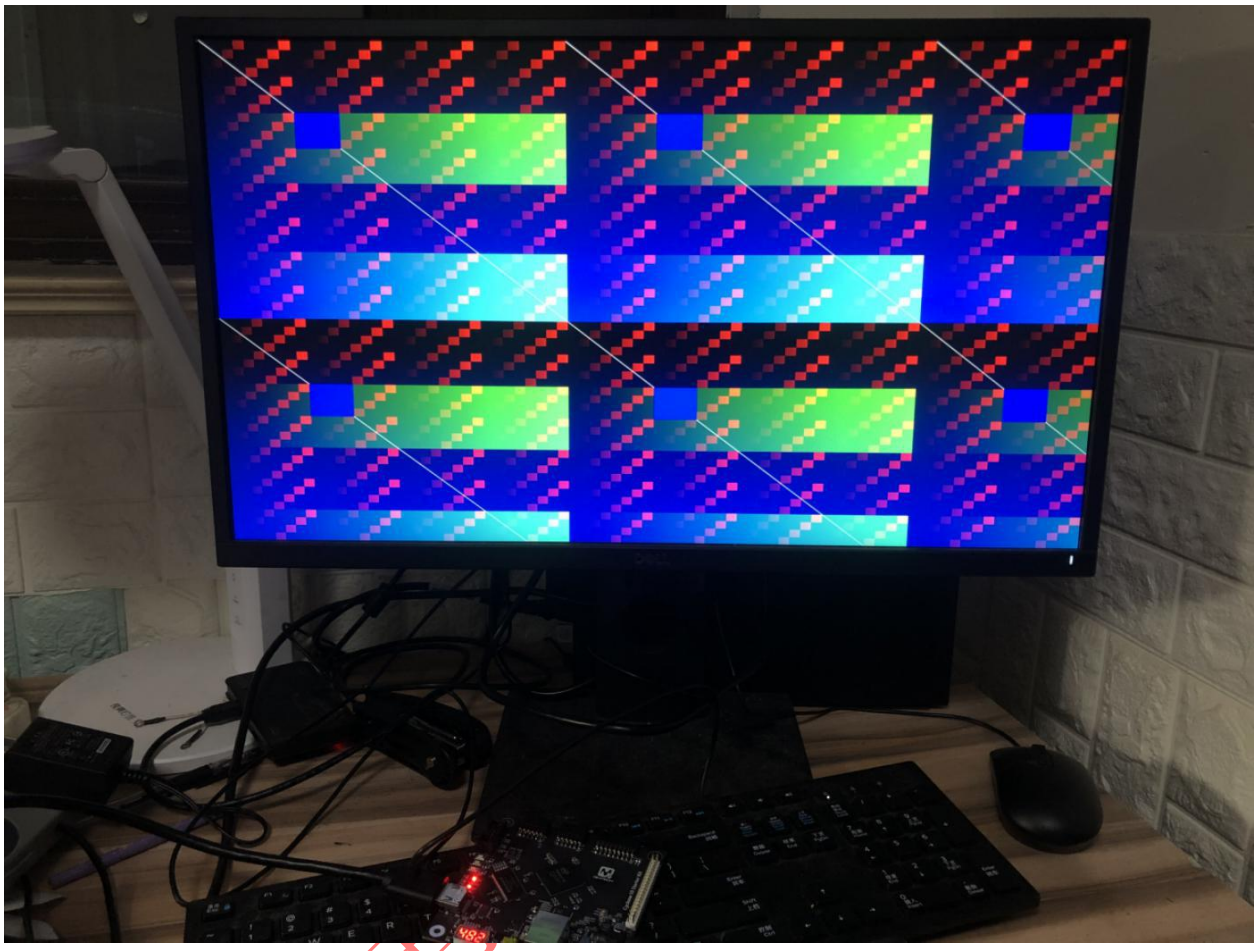


Figure 3-4. HDMI Display Test

1. Experiment (3): GMII Ethernet Test

The Starter Kit uses RTL8211EG to implement the 10M/100M/1000M triple speed ethernet interface. It provides all the necessary physical layer functions to transmit and receive ethernet packets over the CAT.5 UTP cable. The data transfer between PHY and FPGA is via the Gigabit Media Independent Interface(GMII) for 1000Base-T. The RTL8211EG-VB chip supports 3.3V signaling for GMII interface. Below image shows the hardware design of RTL8211EG:

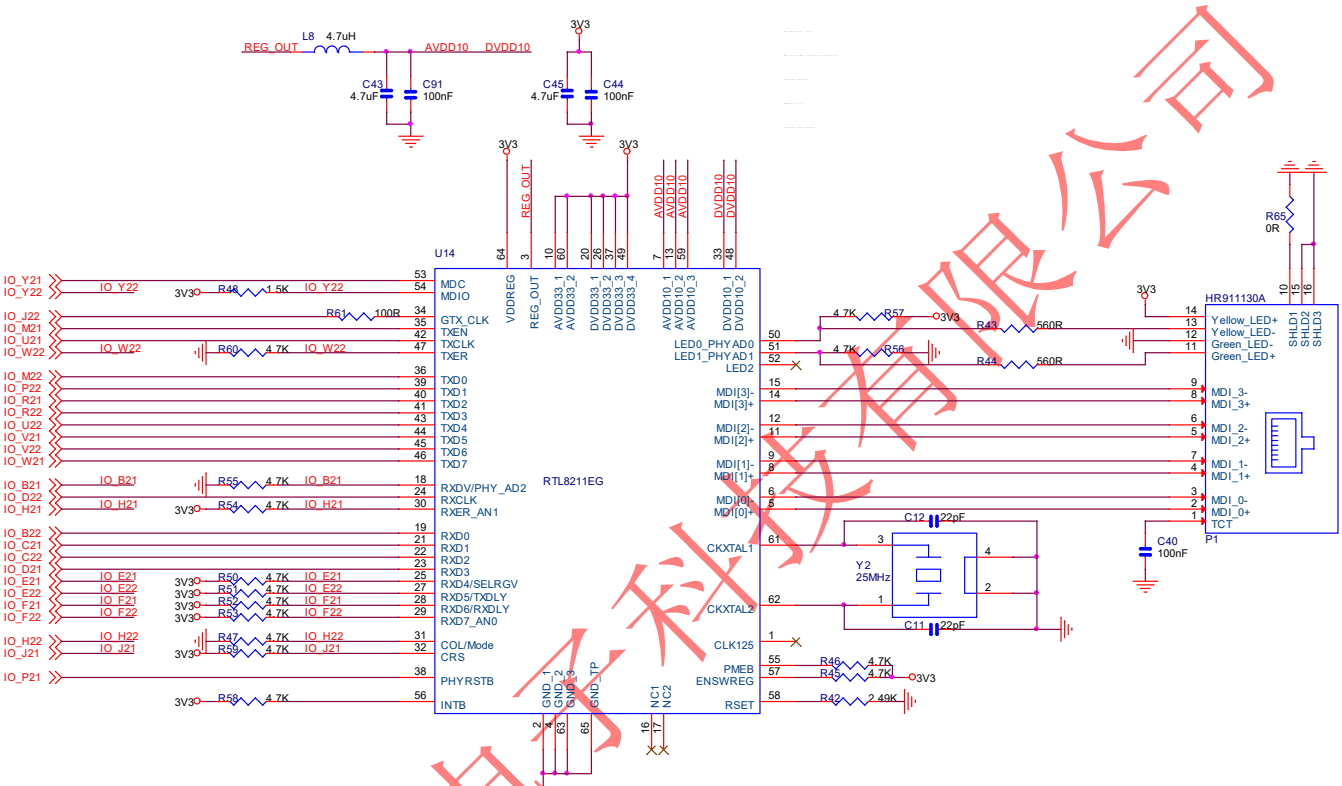


Figure 1-1. RTL8211 Hardware Design

Before start to test the GMII ethernet communication function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to Cyclone 10 Starter Kit's JTAG interface. The ethernet cable shall be plugged in the board and the test computer simultaneously. Then power on the development kit with 5V DC power source. Below figure shows an example hardware setup:

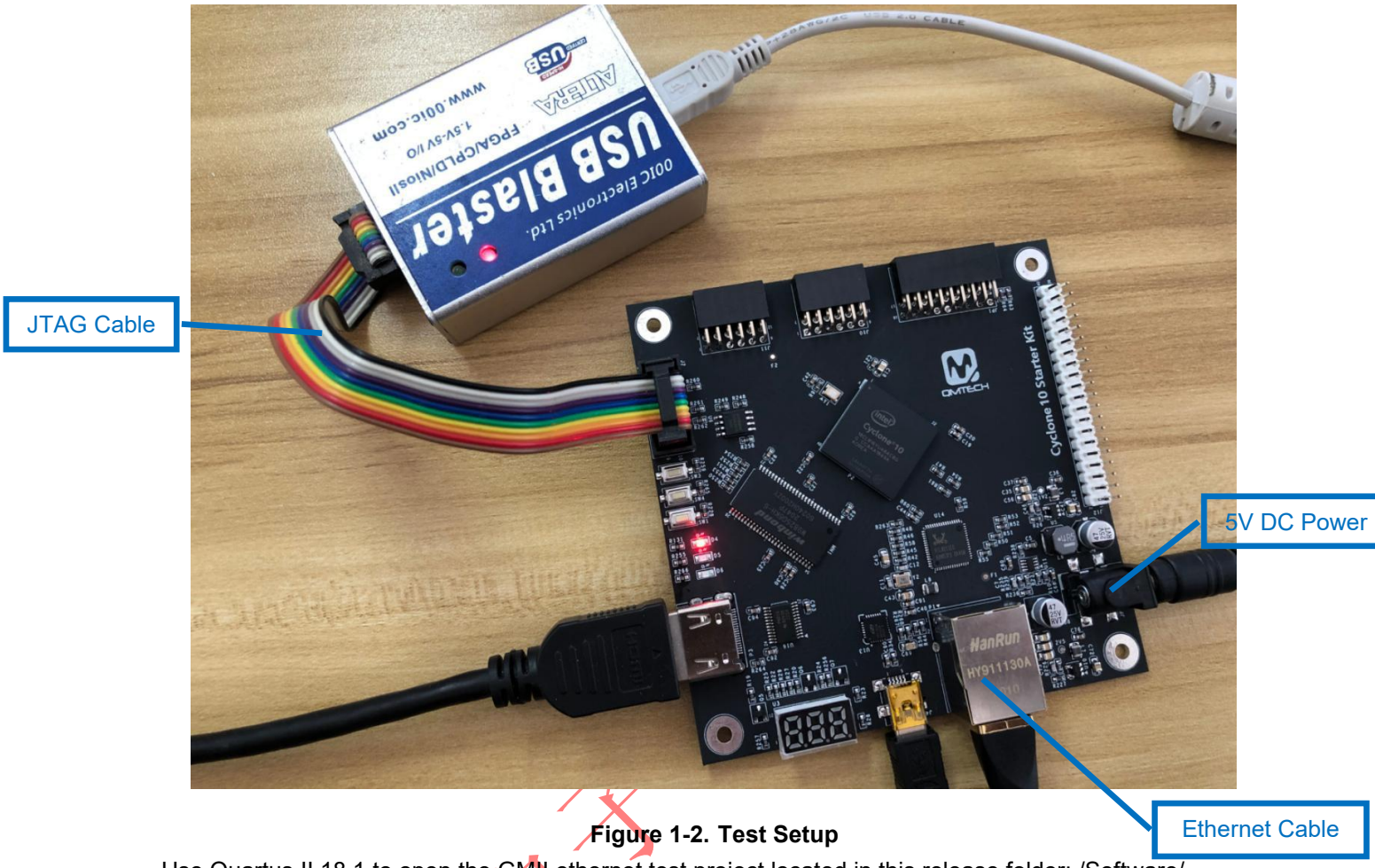
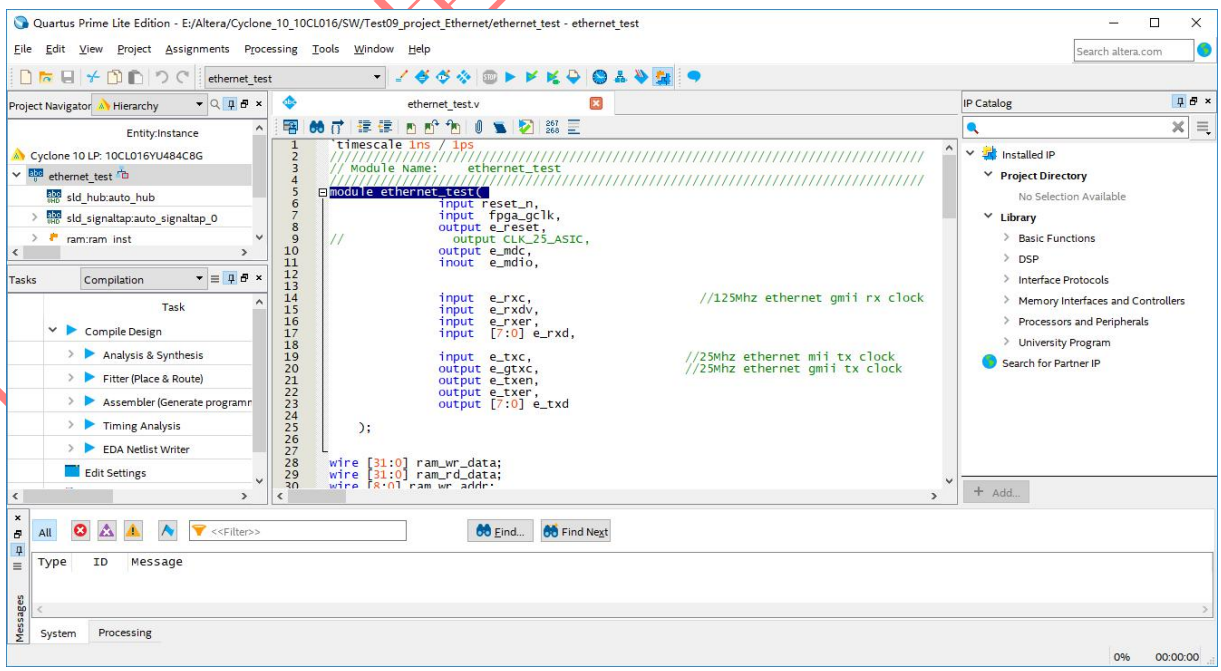


Figure 1-2. Test Setup

Use Quartus II 18.1 to open the GMII ethernet test project located in this release folder: /Software/ Project09_Test_Ethernet. Below figure shows the example project of **ethernet_test**:



After the ethernet test project correctly synthesized, implemented and generated *.sof file, users could use Altera Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.

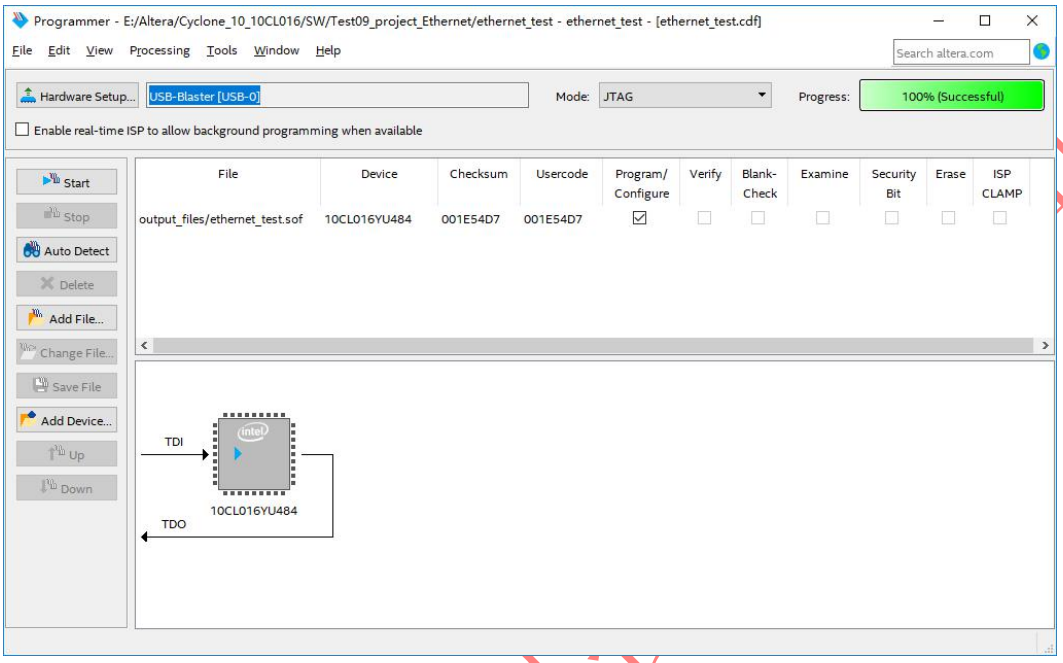


Figure 1-3. FPGA Program

Users could check the ethernet connection status in the Windows OS. Below images shows the ethernet communication speed between the FPGA development board and the test computer is 1Gbps based.

In order to finish this ethernet test, users need to set the Windows's Static IP into 192.168.0.3:

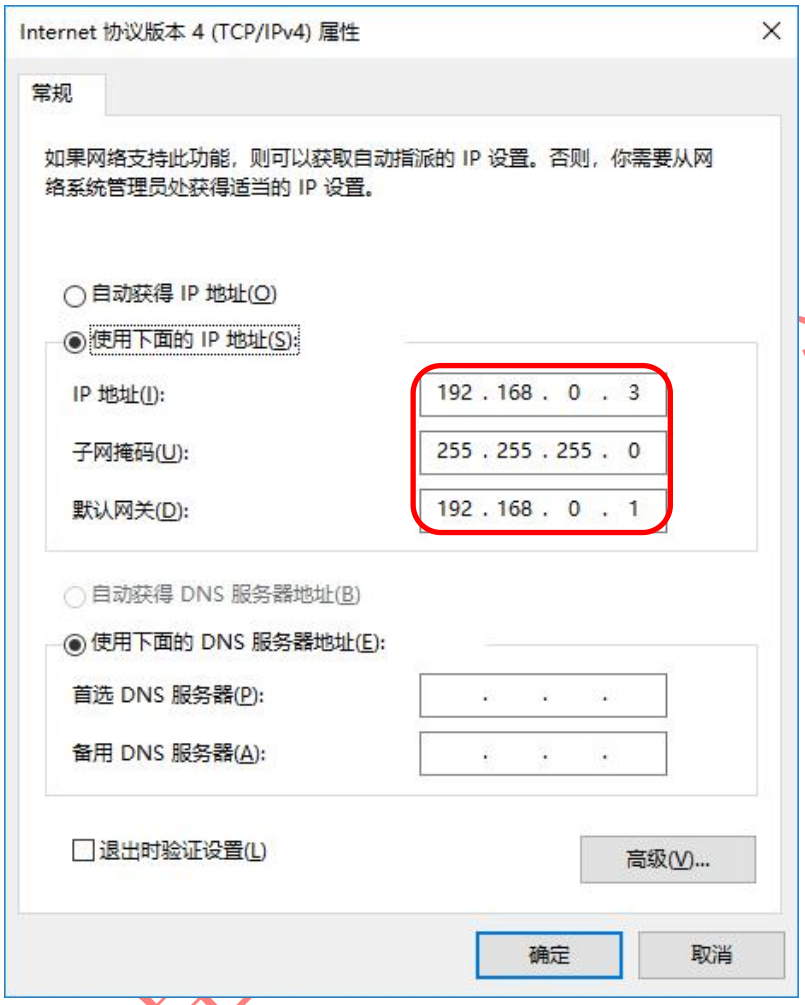


Figure 1-4. Configure PC's IP

Run Windows Command Console as administrator. In that DOS type command window bind the development board's IP address(192.168.0.2) and MAC address (00-0a-35-01-fe-c0) by typing command: ARP -s 192.168.0.2 00-0a-35-01-fe-c0:

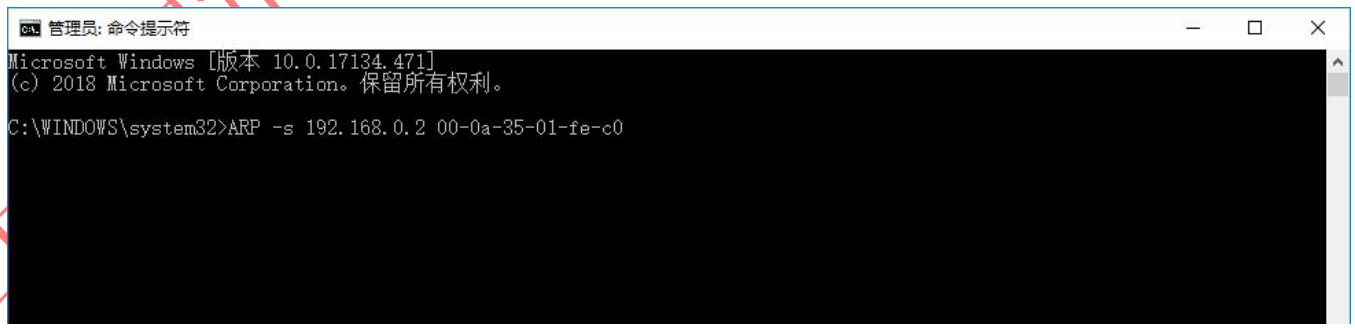


Figure 1-5. Binding IP and MAC

Open the NetAssist ethernet debug tool and set the communication parameters as shown in below figure. Initially, the development board is periodically sending test data “HELLO QMTECH BOARD” to the test PC. Then if user presses the【Send】button to send the test data *http://www.cmsoft.cn* to the FPGA development board. In response, the FPGA will send back test data “*http://www.cmsoft.cn*” to the test PC.

Figure 1-6. GMII Ethernet Test Result

2. Reference

[1] QMTECH-Cyclone10-10CL016-V02.pdf
[2] c10lp-51002.pdf
[3] c10lp-51003.pdf
[4] pcg-01021.pdf
[5] cyclone-10-lp-product-table.pdf
[6] an800.pdf
[7] aib-01029.pdf

3. Revision

Doc. Rev.	Date	Comments
0.1	17/07/2019	Initial Version.
1.0	18/07/2019	V1.0 Formal Release.
2.0	17/01/2121	Upgraded to V2.0 Hardware.