QMTECH CYCLONE IV STARTER KIT

USER MANUAL(QUARTUS 15.1)



Preface

The QMTech® Cyclone IV Starter Kit uses Intel(Altera) EP4CE15F23 device to demonstrate Intel's leadership in offering power-efficient FPGAs. With enhanced architecture and silicon, advanced semiconductor process technology, and power management tools, power consumption for Cyclone IV FPGAs has been reduced by up to 25 percent compared to Cyclone® III FPGAs. The result is the lowest power consumption of any comparable FPGA.

Users could visit QMTECH official website from here: http://www.chinagmtech.com/

Table of Contents

1.	QUAR	QUARTUS PRIME 15.1 INSTALLATION			
2.	FPGA	FPGA PROJECT COMPILE AND *.SOF DOWNLOAD			
	2.1 2.2 2.3 2.4 2.5	CREATE NEW PROJECT COMPILE THE PROJECT PIN ASSIGNMENT DOWNLOAD *.SOF INTO FPG A DOWNLOAD *.JIC INTO SPI FLASH			
3. 4.	SIGNA	ALTAP II LOGIC ANALYZER	2		
5.	RFVIS	SION	2		



1. Quartus Prime 15.1 Installation

The revolutionary Intel® Quartus® Prime Design Software includes everything you need to design for Intel® FPGAs, SoCs, and CPLDs from design entry and synthesis to optimization, verification, and simulation. Dramatically increased capabilities on devices with multi-million logic elements are providing designers with the ideal platform to meet next-generation design opportunities.

The Intel® Quartus® Prime Software design flow comprises of the following high-level steps:



The Quartus Prime software version 15.1 supports the following device families: Stratix IV, Stratix V, Arria II, Arria V, Arria V GZ, Arria 10, Cyclone IV, Cyclone V, MAX II, MAX V, and MAX 10 FPGA. Below image shows the startup UI of Quartus II Prime 15.1:

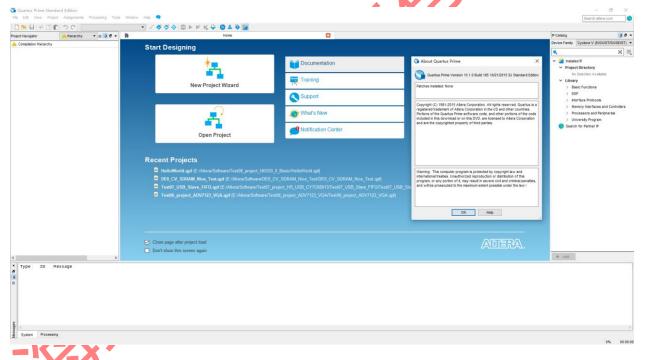


Figure 1-1. Quartus II Prime 15.1

After the Quartus II Prime 15.1 is correctly installed, users still need to install the device package from Intel official website. Below lists the download center address:

https://www.intel.com/content/www/us/en/programmable/downloads/download-center.html

In the Intel Download Center website, select the tab of 'Select by Device' and then all the available device packages will be listed as below image. The device used in this user manual is Cyclone IV E series and the detailed chip part number is EP4CE15F23C8N, so please download the device package for Quartus II 15.1: cyclone-15.1.0.185.qdz.



Software Selector

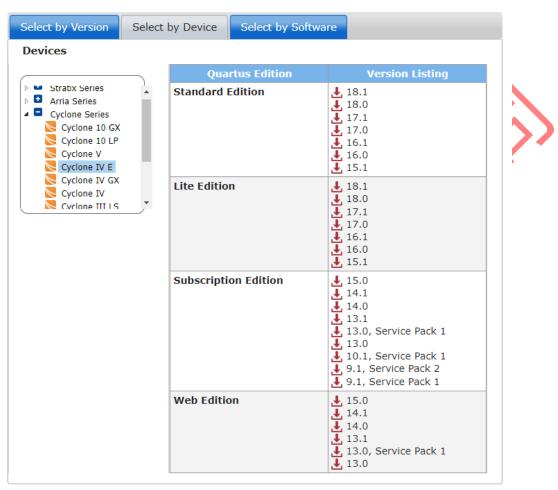


Figure 1-2. Download Device Package

Open Quartus II 15.1, Click Tools → Install Device and then select the downloaded device package:

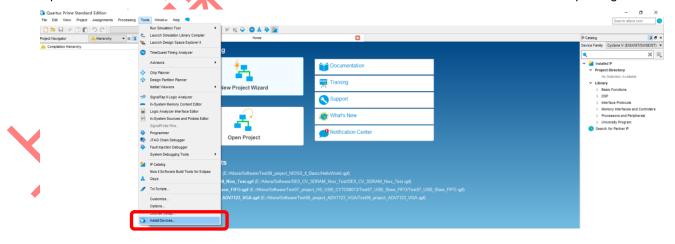


Figure 1-3. Install Device Package



Below window will pop up and click Next:

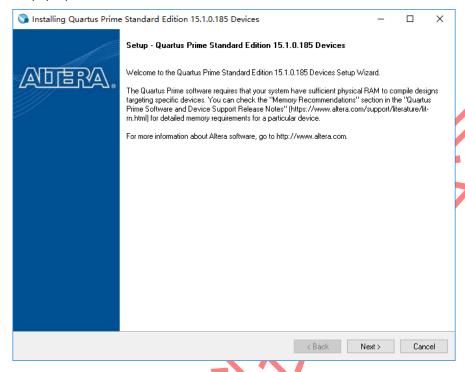


Figure 1-4. Install Device Package

Choose the Download Directory where contains the cyclone-15.1.0.185.qdz file:

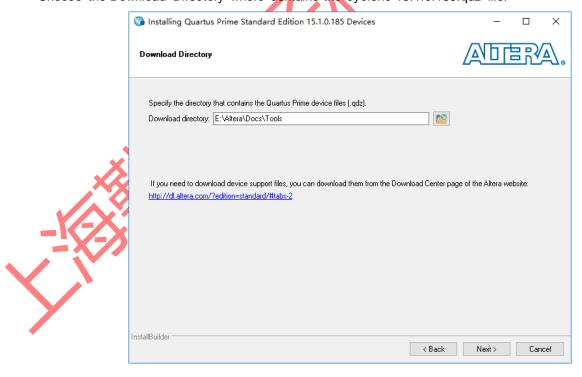


Figure 1-5. Choose Device Package



Choose the device package needs to be installed and click Next:

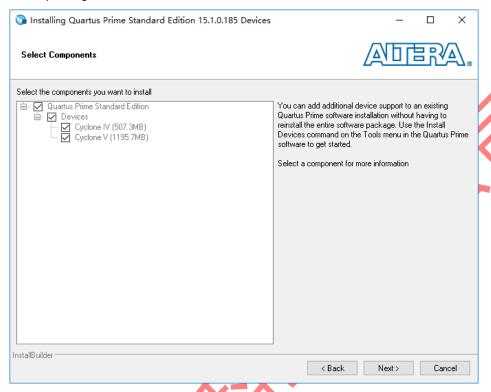


Figure 1-6. Install the Device Package

User could also install the device package by using Quartus II Prime 15.1 Device Installer directly:

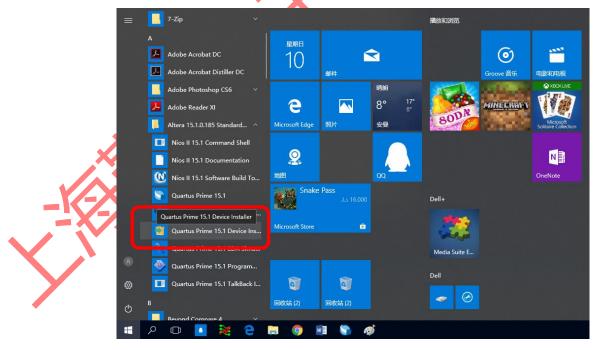


Figure 1-7. Device Installer



2. FPGA Project Compile and *.sof Download

2.1 Create New Project

Click 【File】 → 【New Project Wizard…】 to create a new project:

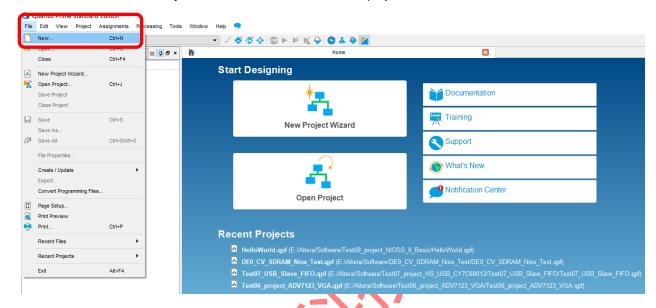


Figure 2-1. Create New Project

Choose [New Quartus Prime Project]

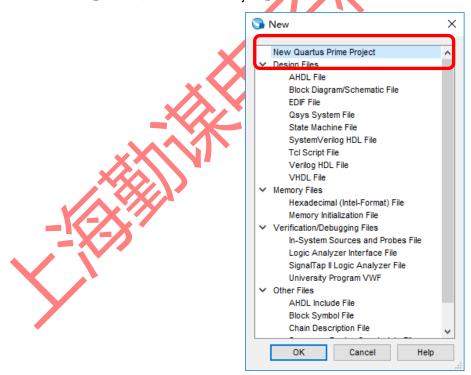


Figure 2-2. New Quartus Prime Project



In below [New Project Wizard] page, choose Next:

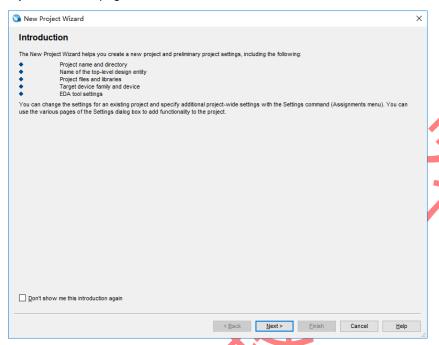


Figure 2-3, New Project Wizard

Set the target working folder below [What is the working directory for this project?]. Set the new project name below [What is the name of this project?]. And finally set the example project name:

Test01_Project_LED shown as below.

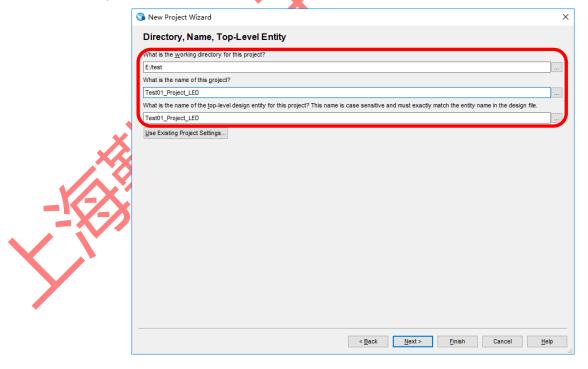


Figure 2-4. Set Working Directory and Project Name



Select [Empty Project] and then click Next:

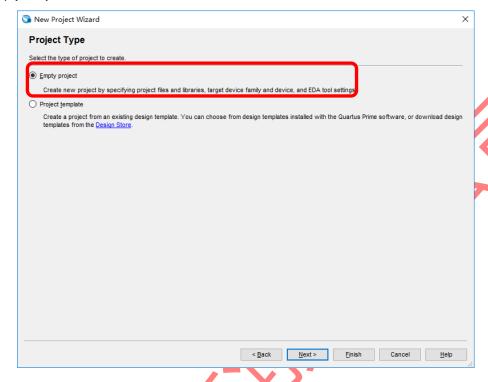


Figure 2-5. Create Empty Project

If user already has some source code, please add all these necessary files in this step:

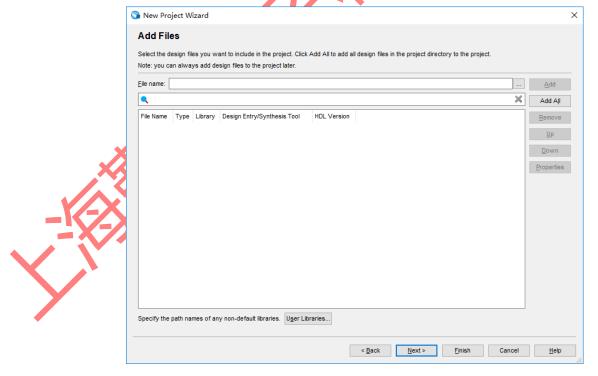


Figure 2-6. Add Source Code



Choose the FPGA Chip number: EP4CE15F23C8N.

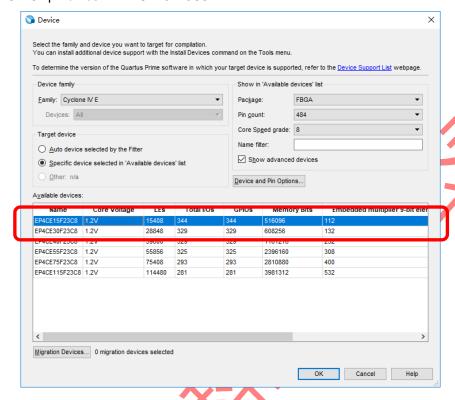


Figure 2-7. Select Device

Summary page will be shown and click [Finish] if there's nothing needs to be changed:

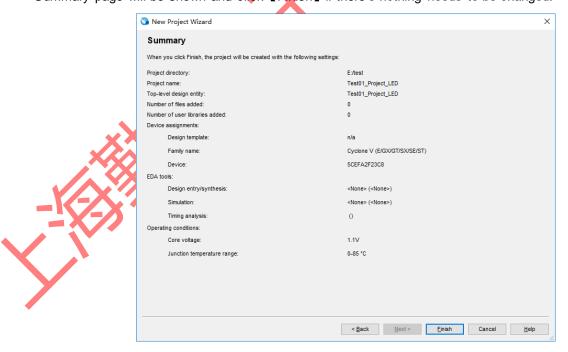


Figure 2-8. Project Summary Page



After the Empty Project created, below image will be shown:

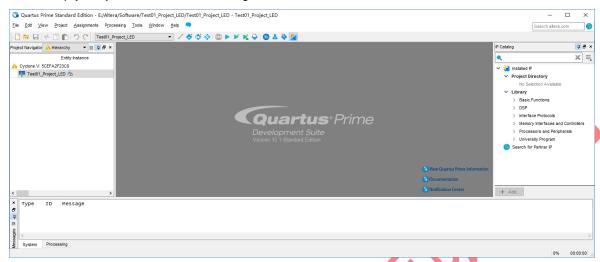


Figure 2-9. Empty Project

Users may add example source file Test01_Project_LED.v into this Empty Project shown as below:

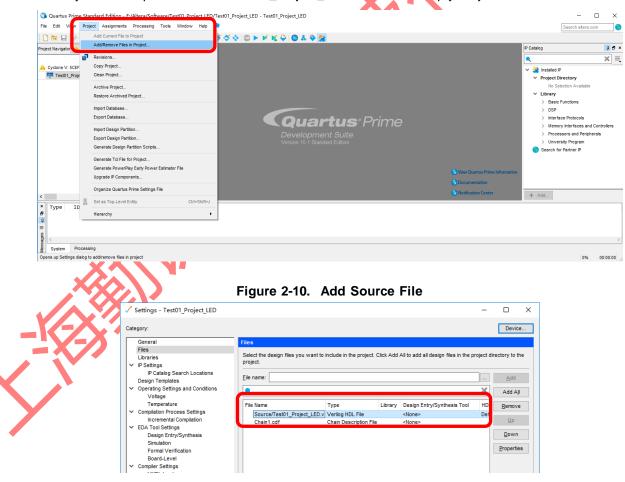


Figure 2-11. Add Source File



After the newly added source file loaded into project, user can view the source code shown as below:

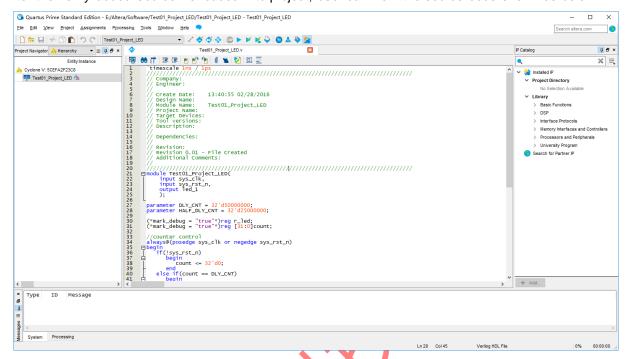


Figure 2-12. View of Source Code

2.2 Compile the Project

Users could use the button [Start Compilation - Ctrl + L] shown in below image to compile the project:

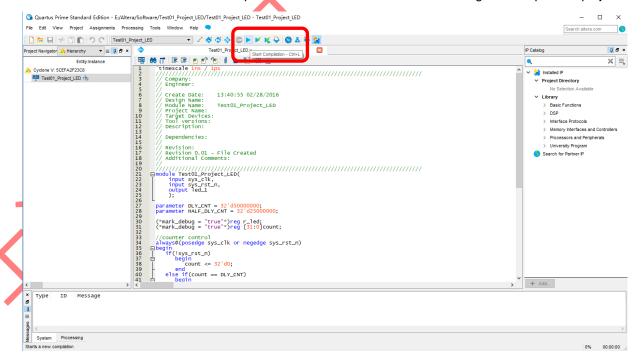


Figure 2-13. Compilation



There will be compilation report after the compile finished, in which shows the info like logical element resource usage, how many PLLs are used, etc. Below image shows an example Compilation Report:

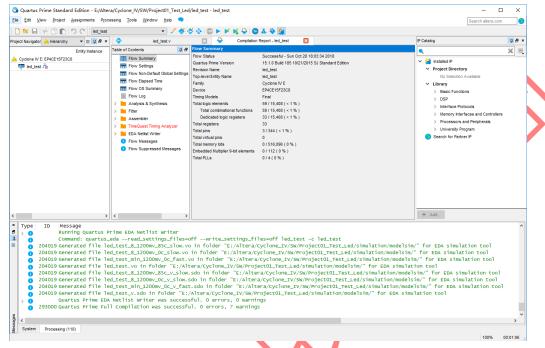


Figure 2-14. Compilation Report

2.3 PIN Assignment

There are several ways to assign the Pins for the example project. Method 1: Choose 【Assignment】 → 【Pin Planner】:

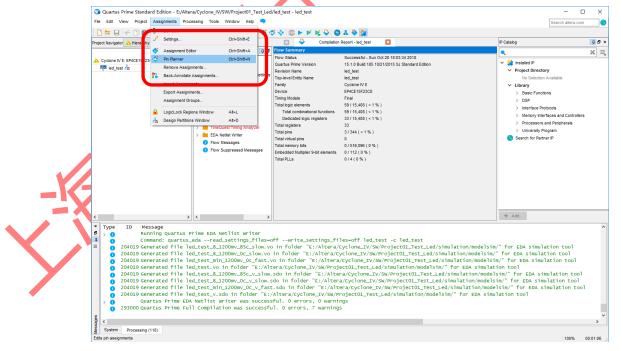


Figure 2-15. Pin Planner



Below image shows PIN settings for this test example:

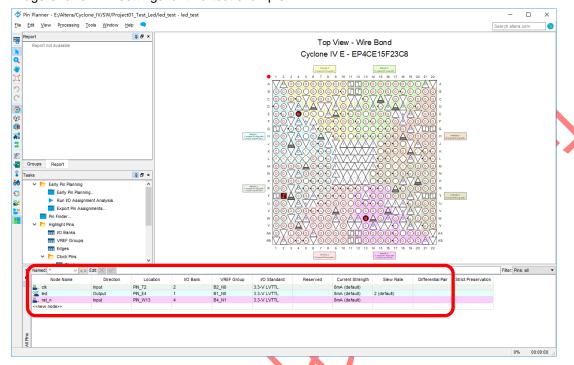


Figure 2-16. PIN Assignment

Method 2: Prepare a *.csv file from other project, then use $Assignment \rightarrow Import Assignment$ to import the existing *.csv file to allocate the Pin assignment:

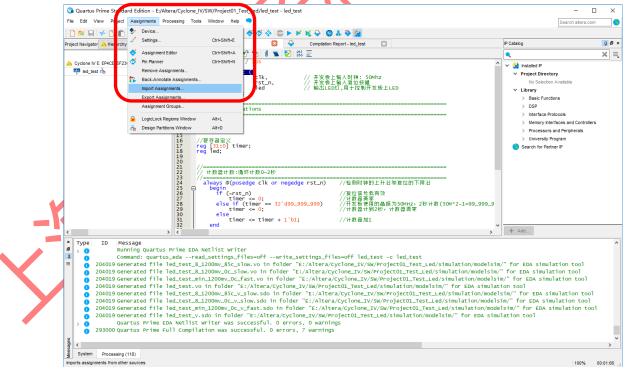


Figure 2-17. Import Assignment



2.4 Download *.sof into FPGA

After the test example correctly compiled, the Quartus will generate a *.sof file which could be directly loaded into FPGA to check whether implemented functions perform as expected. User could use [Tools] > [Programmer] to start a new download:

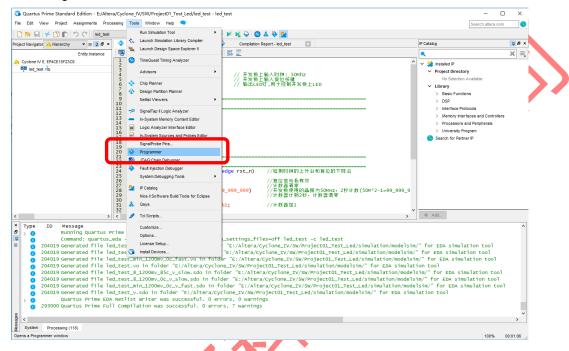


Figure 2-18. Programmer

Make sure the USB Blaster's cable are correctly connected to FPGA's JTAG port before using Programmer to download *.sof file. Then click [Auto Detect] to check the hardware setup is okay or not:

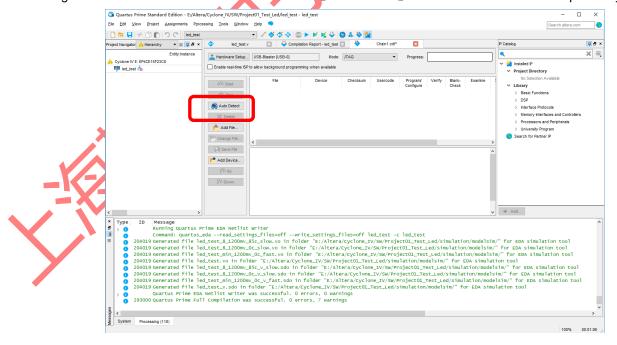


Figure 2-19. JTAG Setup



Below image shows the FPGA has been detected by the Programmer:

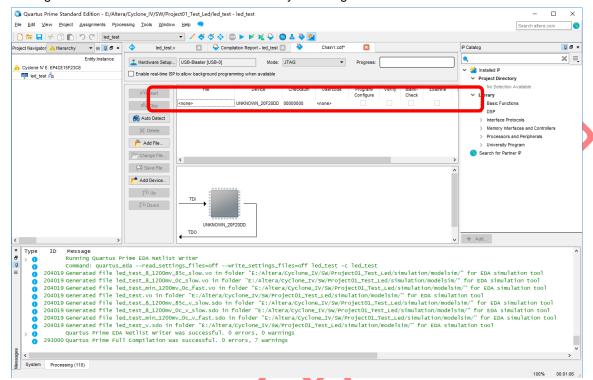


Figure 2-20. Detect FPGA

Users click [None] column to choose the *.sof file to be loaded into FPGA.

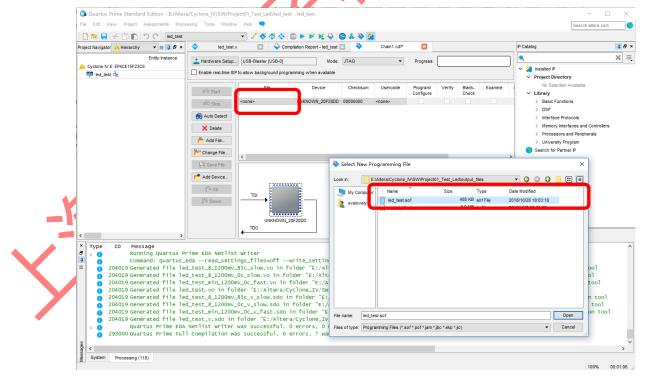
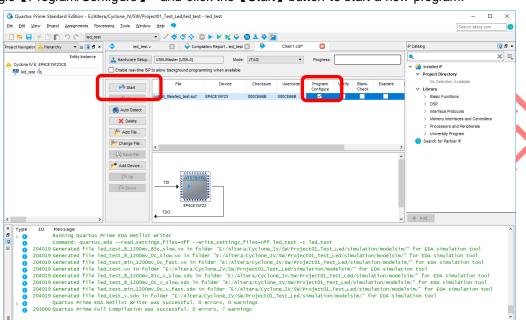


Figure 2-21. Choose *.sof File





Then toggle [Program/Configure] and click the [Start] button to start a new program:

Figure 2-22. Program *.sof

If the *.sof file is correctly programed, the Progress bar will show info like: 100%(Successful). Then users could check whether the LEDs on FPGA board blinking or not.

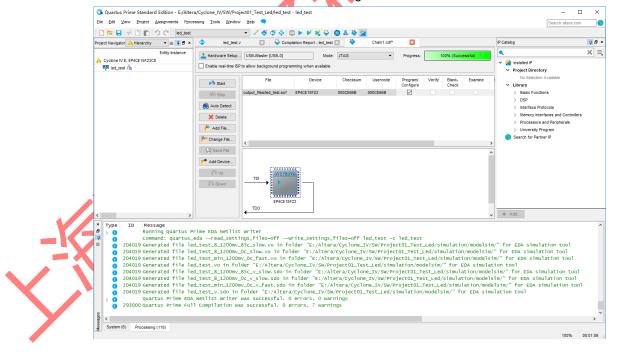


Figure 2-23. Program Successful



2.5 Download *.jic into SPI Flash

Cyclone IV EP4CE15 core board has mounted an external SPI Flash with 8MB capacity. The hardware design chooses Active Serial x 1 method to make the FPGA could boot up from external SPI Flash after power on. In this section, it describes how to program eternal SPI Flash through JTAG port. The SPI Flash is non-volatile device which means the programmed *.jic file will never lose its content after power down.

The SPI Flash programing file *.jic is converted by *.sof file described in previous chapter. So make sure *.sof could be correctly running on FPGA before performing below steps. Step1: choose the Quartus II Prime 15.1file convert tool by click 【File】 → 【Convert Programming File】:

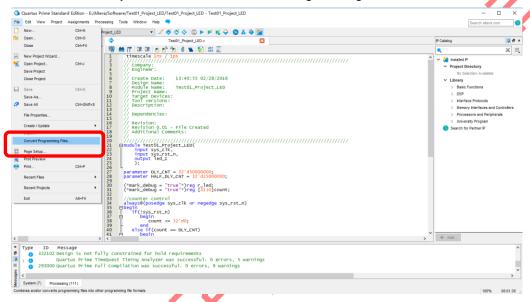


Figure 2-24. Convert Programming File Tool

Change the settings following below figure: choose EPCQ64, generated file name output_file.jic, etc.

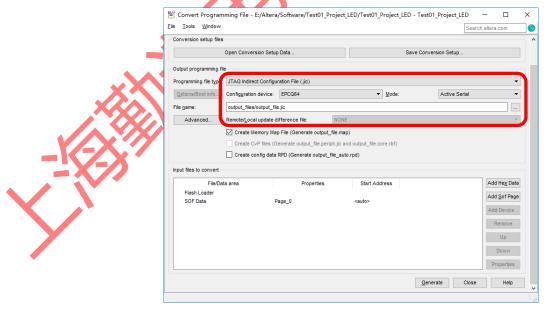


Figure 2-25. Configure Convert Programming File Tool



Convert Programming File - E:/Altera/Software/Test01_Project_LED/Test01_Project_LED - Test01_Project_LED -File Tools Window Search altera.com Conversion setup files Open Conversion Setup Data.. Save Conversion Setup. Output programming file Programming file type: JTAG Indirect Configuration File (.jic) Options/Boot info... Configuration device: EPCQ64 Active Serial ▼ Mode: Manced Options output_files/output_file.jic mote/<u>L</u>ocal update difference file: ☑ Disable EPCS/EPCQ ID check Create Memory Map File (Generate ☑ Disable AS mode CONF_DONE error check Create CvP files (Generate output Create config data RPD (Generate of Post-chain bitstream pad bytes: Post-device bitstream pad bytes: Input files to convert Prope Bitslice padding value: 1 ▼ Add Hex Data Flash Loader QSPI Flash single IO mode dummy clock: Unchangeable Add Sof Page SOF Data Page_0 QSPI Flash quad IO mode dummy clock: Unchangeable Add Device... Down

Click the 【Advanced...】 option, and set these below two options in the red rectangle in Disable status:

Figure 2-26. Advanced Options

<u>G</u>enerate Close

Select [Flash Loader] and then click [Add Device] button:

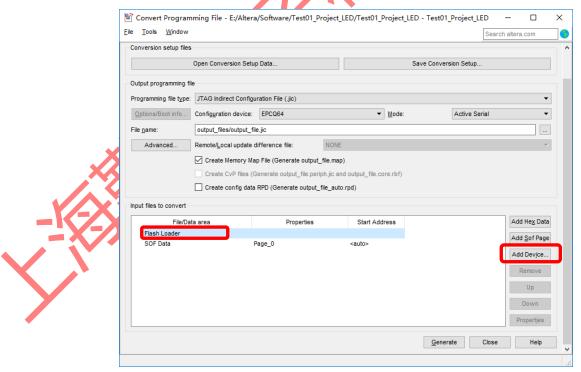


Figure 2-27. Flash Loader



Choose the target Flash Loader device: EP4CE15:

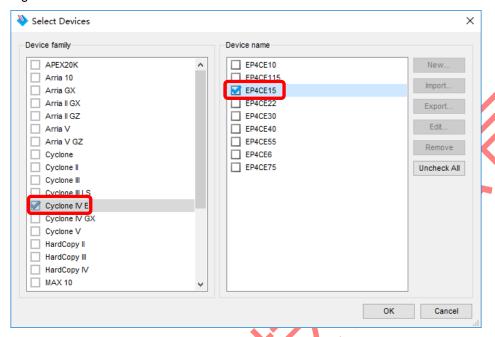


Figure 2-28. Flash Loader for EP4CE15

Select [SOF Data] and then choose [Add File...] to add the verified *.sof file. And then click [Generate] to generate the output_file.jic_file:

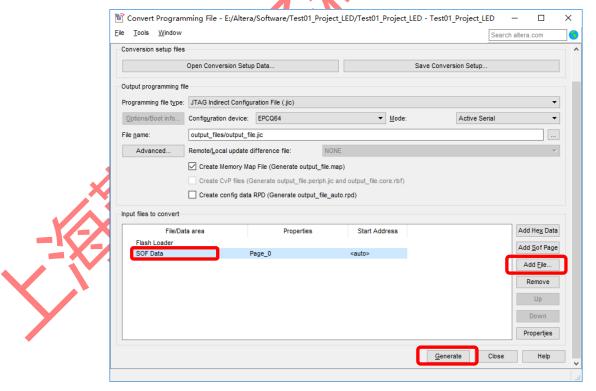


Figure 2-29. Generate *.jic File



After the output_file.jic correctly generated, run the $[Tools] \rightarrow [Programmer]$. And then click [Add File...] to choose the output_file.jic.

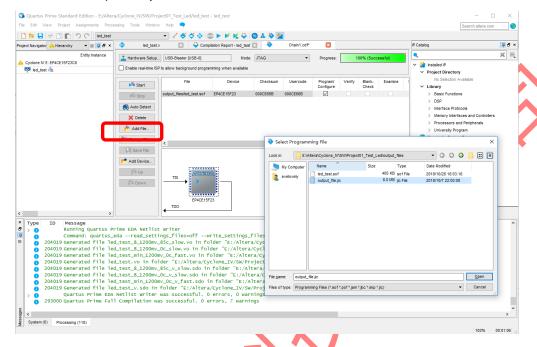


Figure 2-30. Choose *jic File

Toggle [Program/Configure] and then click [Start] button to program the external SPI Flash. Program status will be shown in the [Progress] bar. After the *.jic correctly programmed, user may repower on the board to check whether the FPGA could boot from external SPI Flash.

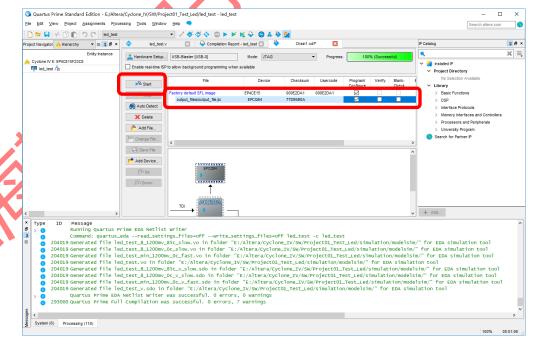


Figure 2-31. Program *.jic



3. SignalTap II Logic Analyzer

The SignalTap II Embedded Logic Analyzer is a system-level debugging tool that captures and displays signals in circuits designed for implementation in Intel's FPGAs. The user is expected to have access to a computer that has Quartus II 15.1 software installed. The detailed example in this chapter was obtained using Quartus II version 15.1, but newer versions of the software can also be used.

After successfully compiling the Project04_SDRAM project and setting pin assignments, select SignalTap II Logic Analyzer from the tools dropdown menu (as shown below). Ensure the JTAG programmer (USB Byte Blaster) is connected between the board and the computer.

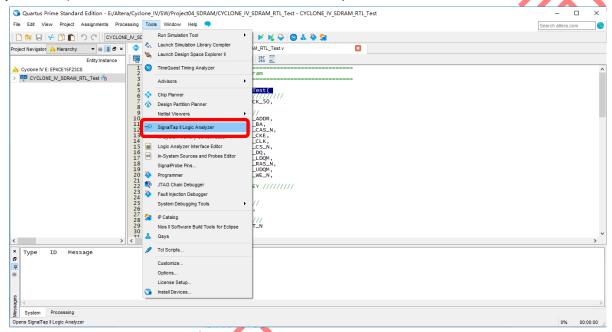


Figure 3-1. Open SignalTap II Logic Analyzer

Below image shows the UI of the Signal Tap II:

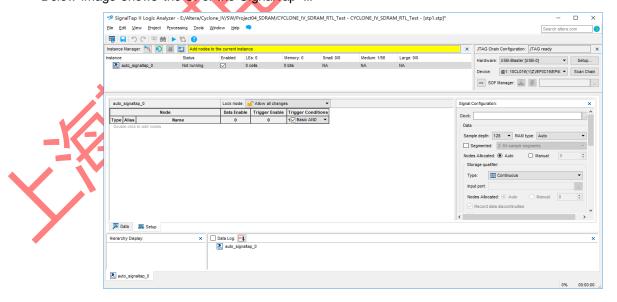


Figure 3-2. SignalTap II Logic Analyzer sUI



🥦 SignalTap II Logic Analyzer - E:/Altera/Cyclone_IV/SW/Project04_SDRAM/CYCLONE_IV_SDRAM_RTL_Test - CYCLONE_IV_SDRAM_RTL_Test - [stp1.... — **JTAG** File Edit View Project Processing Tools Window Help Search altera.com Configuration, ■ ■ りで | ※ * | ▶ は 3 Device Setup, Instance Manager: 🍳 🔊 🔳 × JTAG Chain Configuration: JTAG ready Download *.sof Enabled LEs: 0 Small: 0/0 Memory: 0 Hardware: USB-Blaster [USB-0] auto_signaltap_0 0 cells 0 bits Device: @1: 10CL016(Y|Z)/EP3C16/EP4(▼ Scan Cha Compile >> SOF Manager: Lock mode: Allow all changes auto signaltap 0 Data Enable Trigger Enable Trigger Conditions Signal Sampling Clock Monitor Signals Storage qualifier: Capture Data **Buffer Size** Nodes Allocated: Auto Manual: 0 Record data discontinuities Trigger Nodes Allocated:

Auto

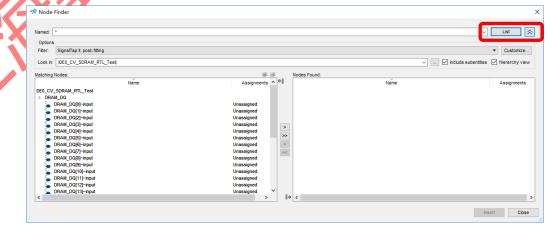
Manual:

0 Trigger flow control: Sequential Trigger position: Trigger conditions: 1 O Instance: Hard Processor System (HPS) trigger out Pattern: T High Data Setup × Data Log: Hierarchy Display: auto_signaltap_0 auto_signaltap_0

Below image shows the settings of the Project04 SDRAM example project:

Figure 3-3. SignalTap II Logic Analyzer Main Window

Double click the [Node] column shown in the above image. Below window will pop up and user clicks the [List] button to add the signals need to be monitored:





All the signals added in the above step will be displayed in the 【setup】 page. Please also select the signal sampling clock 【DRAM_CLK】:

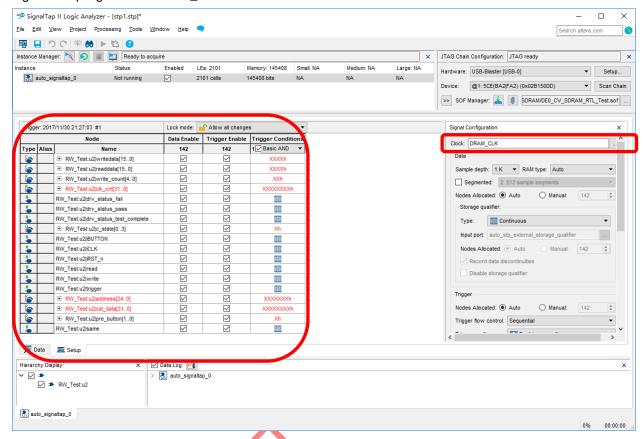


Figure 3-4. Sampling Signals and Clocks

User needs to click the 【Compile】 button shown in the below image to recompile the whole project. Then user may download the newly compiled *.sof into FPGA.

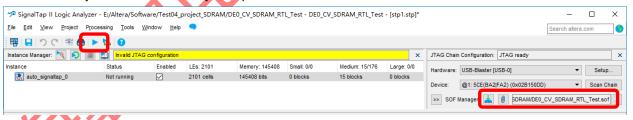


Figure 3-5. Compile the SignalTap II Projects

User could click the button 【AutoRun Analysis】 or button 【Run Analysis】 to start the waveform capture:

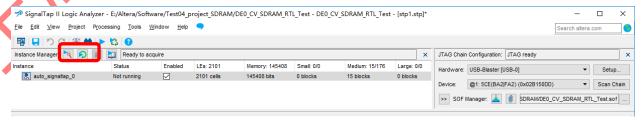


Figure 3-6. Start Capture



Below two images show the SDRAM data write and SDRAM data read: Fig. Edit View Project Processing | Relative Standard | Relative × JTAG Chain Configuration: JTAG ready Hardware: USB-Blaster [USB-0] Device: @1: 10CL016(Y|Z)/EP3C16/EP4CE15 (0x020F > Scan Chain >> SOF Manager: MVCYCLONE_IV_SDRAM_RTL_Test sof ... 169 169 179 184 182 200 209 219 224 222 240 249 259 264 272 260 269 269 269 304 312 320 320 339 Data 🐺 Setup auto_signaltap_0 Figure 3-7. Waveform for Writing Data into SDRAM 04_SDRAM/CYCLONE_IV_SDRAM_RTL_Test - CYCLONE_IV_SDRAM_RTL_Test - [stp1.stp] e Manager: 🔯 👂 🔳 🔼 Hardware: USB-Blaster [USB-0] Setup... auto_signaltap_0 Device: @1: 10CL016(Y|Z)/EP3C16/EP4CE15 (0x020F → Scan Chain log: Trig @ 2019/01/04 23:24:39 (0:0:0.1 elapsed) #3 $oldsymbol{m}$ 1

② data Log ②

② mata_systember_0

③ mata_systember_0

⑤ mata_systember_0

⑤ mata_systember_0

⑥ mata_syst 🧧 Ps 🔚 🧑 💿 🐠 🕥 🚿

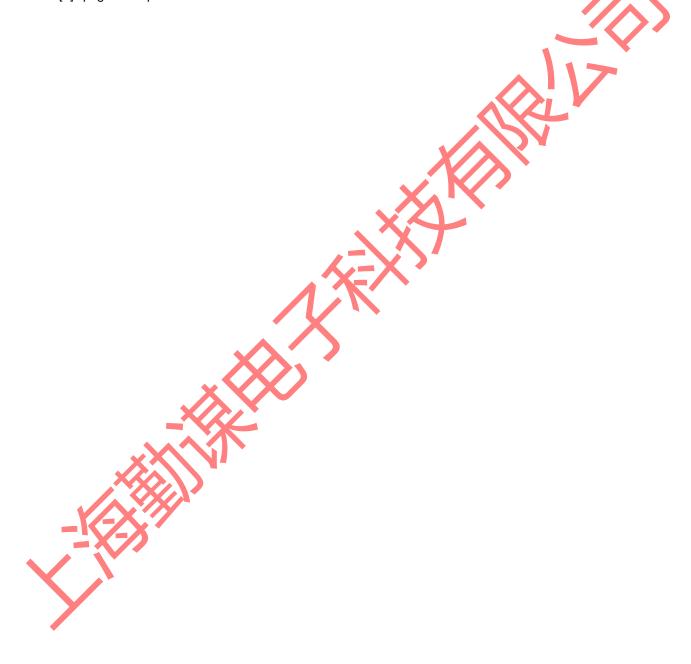
Figure 3-8. Waveform for Reading Data from SDRAM



Reference 4.

- [1] ep4ce15f23-starter-kit.pdf[2] an592.pdf[3] an592_ch.pdf

- [4] cyiv-5v1.pdf [5] cyiv-5v2.pdf [6] cyiv-5v3.pdf
- [7] pcg-01008.pdf





5. Revision

Doc. Rev.	Date	Comments
0.1	17/04/2019	Initial Version.
1.0	18/04/2019	Formal Release.



