

→ 5V DC

→ HDMI Cable, connected to monitor

→ USB Blaster

Step1: Open project CV_SOC_HDMI_TX.qpf by Quartus II 18.1 or newer version.

Quartus Prime Lite Edition - E:/Altera/Cyclone_V_SOC/Workspace/HDMI_TX_QMTECH/HDMI_TX/CV_SOC_HDMI_TX - CV_SOC_HDMI_TX

File Edit View Project Assignments Processing Tools Window Help

CV_SOC_HDMI_TX

Entity Instance

Cyclone V: SCSEMA6U23A7

CV_SOC_HDMI_TX

Compilation Report - CV_SOC_HDMI_TX

CV_SOC_HDMI_TX.v

```
1 //define ENABLE_HPS
2
3
4 module CV_SOC_HDMI_TX(
5
6     //FPGA
7     input FPGA_CLK1_50,
8     input FPGA_CLK2_50,
9     input FPGA_CLK3_50,
10
11     //HDMI
12     inout HDMI_I2C_SCL,
13     inout HDMI_I2C_SDA,
14     inout HDMI_I2S,
15     inout HDMI_LRCLK,
16     inout HDMI_MCLK,
17     inout HDMI_SCLK,
18     output HDMI_TX_CLK,
19     output [23:0] HDMI_TX_D,
20     output HDMI_TX_DE,
21     output HDMI_TX_HS,
22     input HDMI_TX_INT,
23     output HDMI_TX_VS,
24
25     //KEY
26     input [1:0] KEY,
27
28     //LED
29     output [7:0] LED,
30
31     //SW
32     input [3:0] SW
33 );
34
35
36
37
38 //REG/WIRE declarations
39
40 wire reset_n;
41 wire p11_1200k;
42 reg [12:0] counter_1200k;
43 reg en_150;
44 wire vpg_mode_change;
45 wire [3:0] vpg_mode;
46 wire AUD_CTRL_CLK;
47 //Video Pattern Generator
48 wire [3:0] vnn_disp_mode;
```

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programmin
- Timing Analysis
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

IP Catalog

Installed IP

- Project Directory
 - No Selection Available
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
- Search for Partner IP

Messages

System Processing (244)

Ln 20 Col 37 Verilog HDL File 100% 00:01:45

332146 worst-case minimum pulse width slack is 0.617

332114 Report Metastability: Found 2 synchronizer chains.

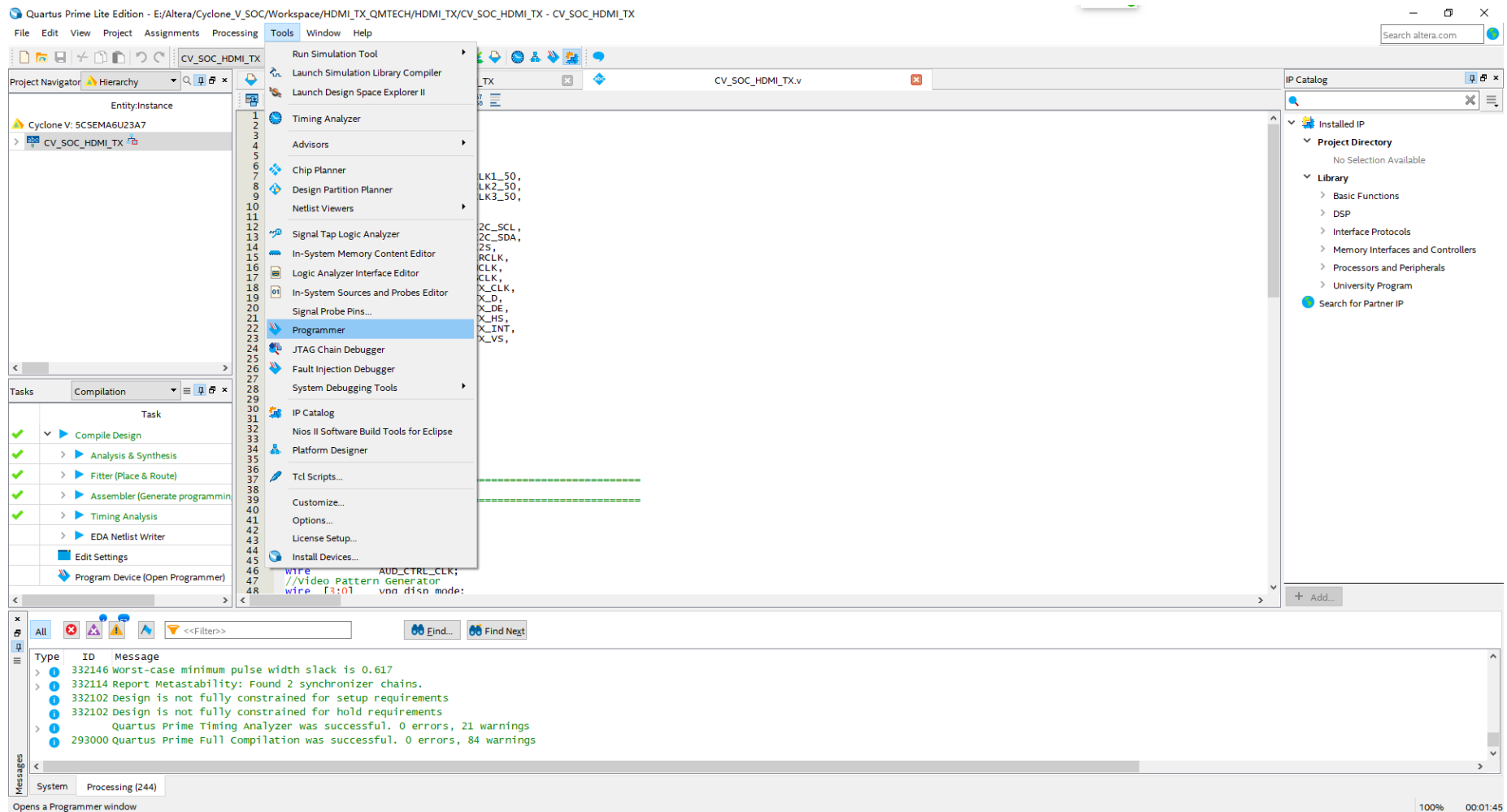
332102 Design is not fully constrained for setup requirements

332102 Design is not fully constrained for hold requirements

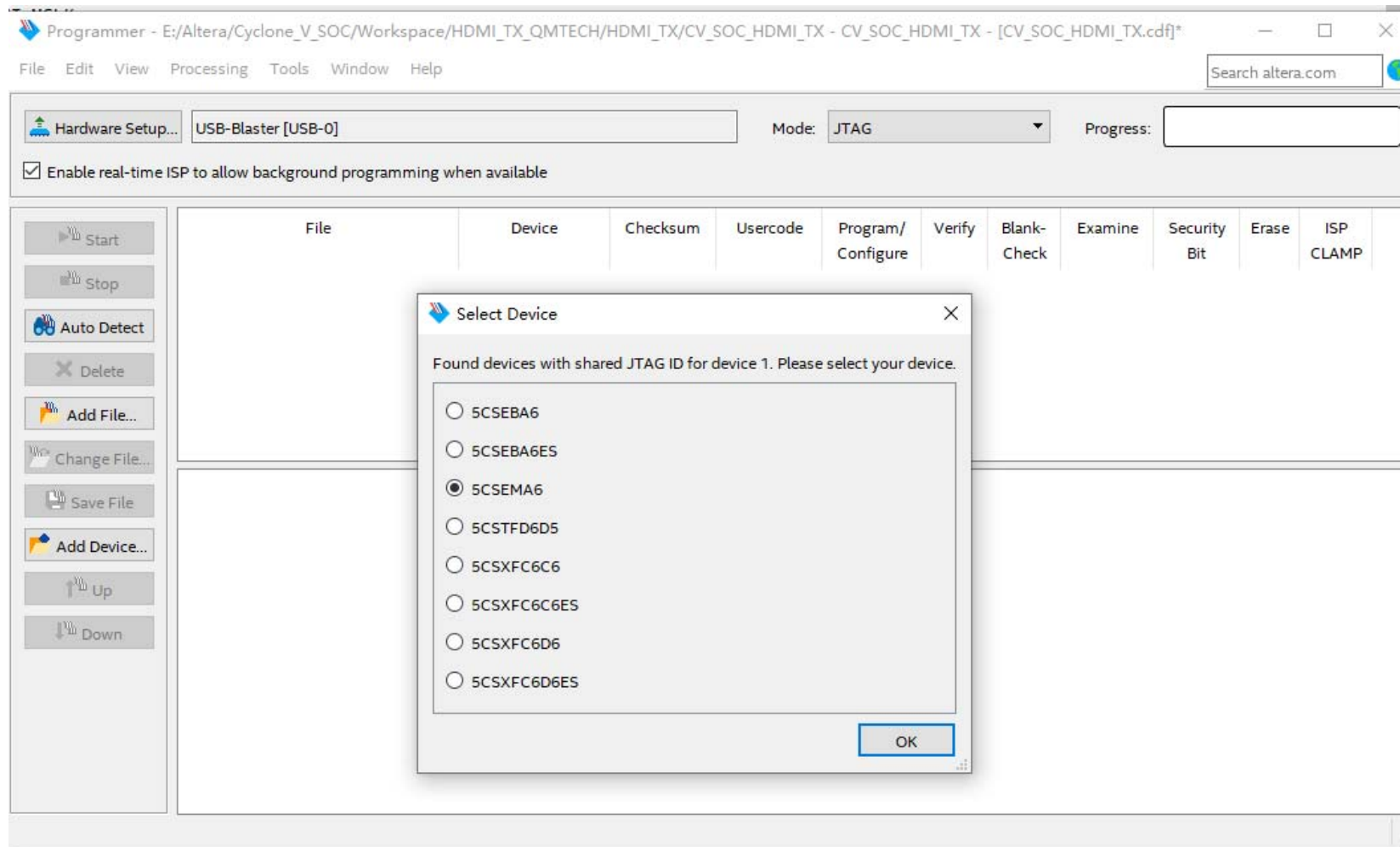
Quartus Prime Timing Analyzer was successful. 0 errors, 21 warnings

293000 Quartus Prime Full Compilation was successful. 0 errors, 84 warnings

Step2: Make sure there's no compilation issue happen. Then start the **Programmer** shown in below image.



Step3: Select chip on your board. 5CSEMA6, 5CSEBA6 or 5CSXFC6C6...



Step4: Select the test file: CV_SOC_HDMI_TX.sof

The screenshot shows the Altera Programmer application window. The title bar indicates the file being opened is `E:\Altera\Cyclone_V_SOC\Workspace\HDMI_TX_QMTECH\HDMI_TX\CV_SOC_HDMI_TX - CV_SOC_HDMI_TX - [CV_SOC_HDMI_TX.cdf]*`. The menu bar includes File, Edit, View, Processing, Tools, Window, and Help. A search bar for `altera.com` is present.

The Hardware Setup section shows `USB-Blaster [USB-0]` selected, with the Mode set to `JTAG`. A checkbox for `Enable real-time ISP to allow background programming when available` is checked.

The main interface features a table with columns: File, Device, Checksum, Usercode, Program/Configure, Verify, Blank-Check, Examine, Security Bit, Erase, and ISP CLAMP. The first row shows `<none>` for File, `5CSEMA6` for Device, `00000000` for Checksum, and `<none>` for Usercode. The Program/Configure, Verify, Blank-Check, Examine, Security Bit, Erase, and ISP CLAMP columns all have checkboxes that are currently unchecked.

On the left side, there is a vertical toolbar with buttons: Start, Stop, Auto Detect, Delete, Add File..., Change File..., Save File, Add Device..., Up, and Down. Below these buttons is a diagram of the 5CSEMA6 device with TDI and TDO pins indicated.

A "Select New Programming File" dialog box is open, showing the file `CV_SOC_HDMI_TX.sof` selected in the file list. The file is 6.4 MB and is a sof File, last modified on 2024/2/21 10:49:48. The "Look in" path is `E:\Altera\Cyclone_V_SO...H\HDMI_TX\output_files`. The "File name" field contains `CV_SOC_HDMI_TX.sof`, and the "Files of type" dropdown is set to `Programming Files (*.sof *.pof *.jam *.jbc *.ekp *.jic)`. The "Open" button is highlighted.

Step5: check the box named as “Program/Configure”. Then click the **Start** button.

Programmer - E:/Altera/Cyclone_V_SOC/Workspace/HDMI_TX_QMTECH/HDMI_TX/CV_SOC_HDMI_TX - CV_SOC_HDMI_TX - [CV_SOC_HDMI_TX.cdf]*


File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

☒ Enable real-time ISP to allow background programming when available

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/CV_SOC_HDMI_TX.sof	5CSEMA6U23	00CF6406	00CF6406	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

TDI →  TDO

5CSEMA6U23

Step6: Program result.

Programmer - E:/Altera/Cyclone_V_SOC/Workspace/HDMI_TX_QMTECH/CV_SOC_HDMI_TX - CV_SOC_HDMI_TX - [CV_SOC_HDMI_TX.cdf]*

File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 100% (Successful)

☒ Enable real-time ISP to allow background programming when available

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/CV_SOC_HDMI_TX.sof	5CSEMA6U23	00D01462	00D01462	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

Diagram illustrating the JTAG connection to the 5CSEMA6U23 device:

```
graph LR; TDI --> Device[5CSEMA6U23]; Device --> TDO;
```

Step7: HDMI TX result.

