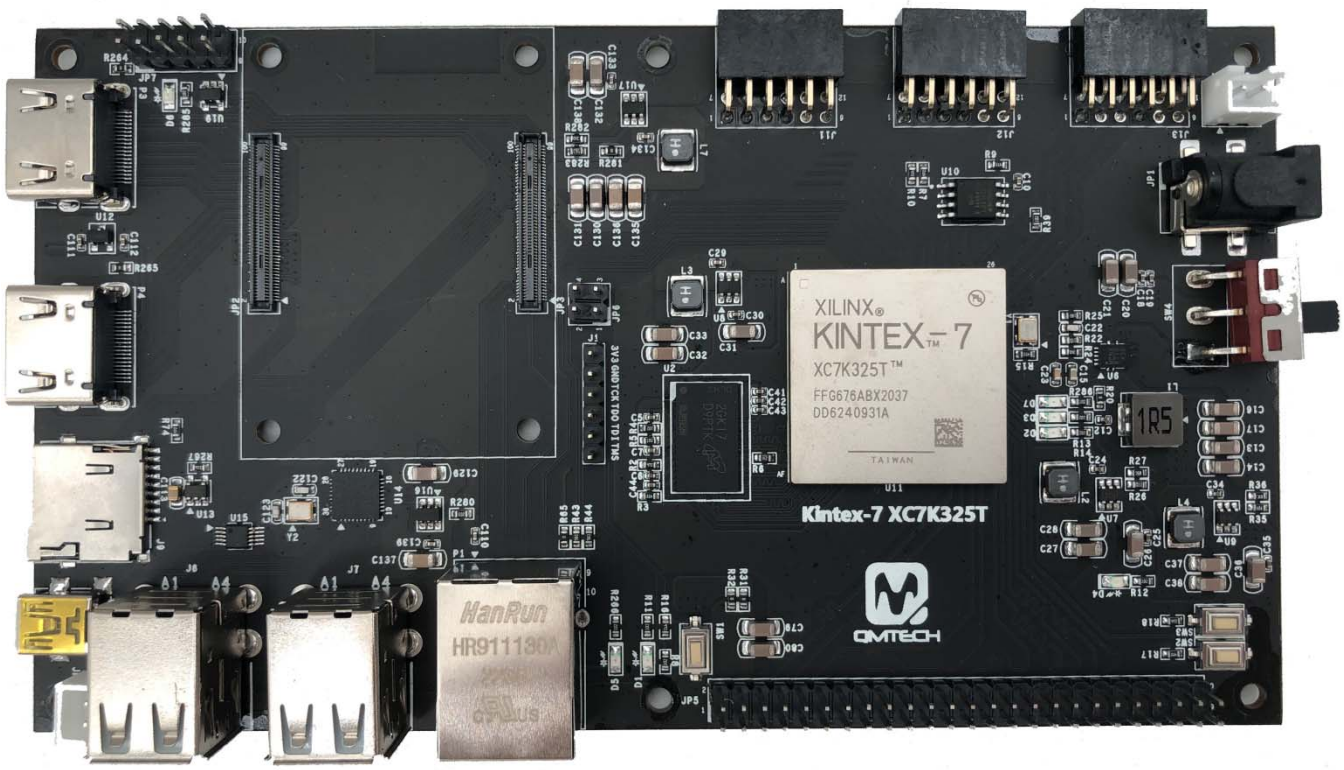
QMTECH XC7K325T DEV BOARD

USER MANUAL



Preface

The QMTECH® XC7K325T development board uses Xilinx Kintex®-7 devices to demonstrate best price/performance/watt at 28nm while giving you high DSP ratios, cost-effective packaging, and support for mainstream standards like PCIe® Gen3 and 10 Gigabit Ethernet. The Kintex-7 family is ideal for applications including 3G and 4G wireless, flat panel displays, and video over IP solutions.

Table of Contents

1. Introduction

1.1 Document Scope

This demo user manual introduces the QMTECH XC7K325T development board and describes how to setup the development board running with application software Xilinx Vivado 2018.3. Users may employee the on board rich logic resource FPGA XC7K325T-1FFG676C and large DDR3 memory MT41K128M16 to implement various applications. The development board also has rich IO resource for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module and computer modules like Raspberry Pi CM4 etc.

1.2 Kit Overview

Below section lists the parameters of the QMTECH XC7K325T development board:

- On-Board FPGA: XC7K325T-1FFG676C;
- On-Board FPGA external crystal frequency: 50MHz;
- XC7K325T-1FFG676C has rich block RAM resource up to 16,020Kb;
- XC7K325T-1FFG676C has 326,080 logic cells;
- On-Board S25FL128L SPI Flash, 16M bytes for user configuration code;
- On-Board 256MB Micron DDR3, MT41K128M16JT-125:K;
- On-Board core power supply for FPGA by using MP8712 wide input range DC/DC, it can provide 12A continuous/15A peak output current;
- XC7K325T development board has one 50p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- XC7K325T development board has 3 user switches;
- XC7K325T development board has 4 user LEDs;
- XC7K325T development board has JTAG interface, by using 6p, 2.54mm pitch header;
- XC7K325T development board PCB size is: 160mm x 90mm;
- Default power source for board is: 2A@6V DC, the DC header type: DC-050, 5.5mm x 2.1mm;

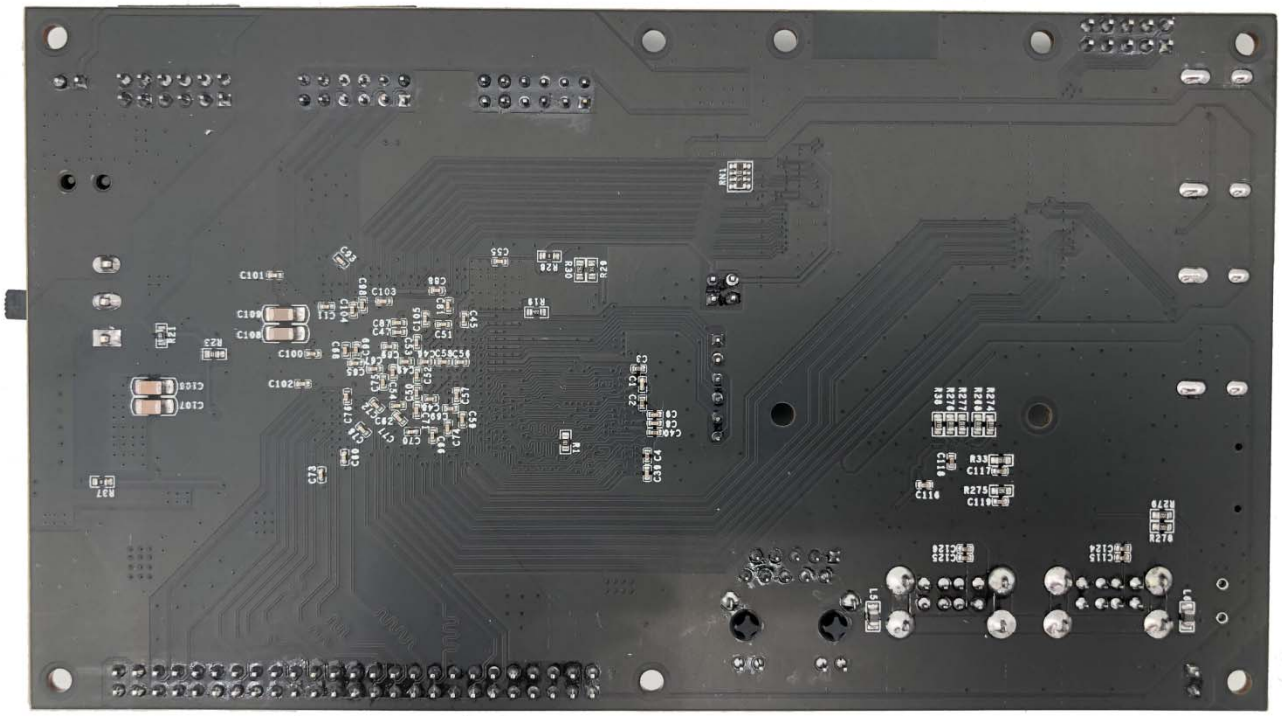


Figure 1-1. QMTECH XC7K325T Development Board Bottom View

2. Getting Started

Below image shows the dimension of the QMTECH XC7K325T development board: 160mm x 90mm. The unit in below image is millimeter(mm).

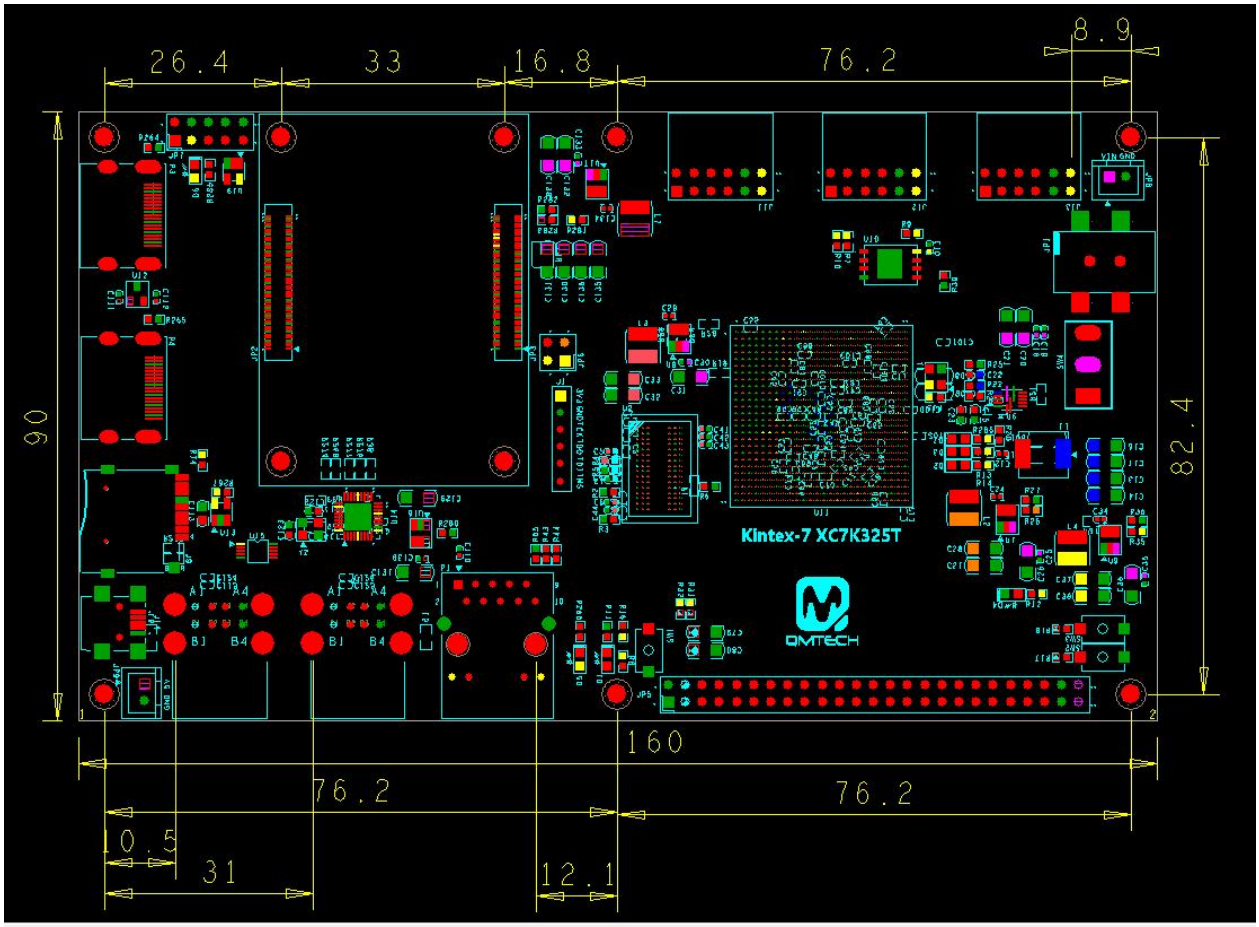


Figure 2-1. QMTECH XC7K325T Development Board Dimension

2.1 Install Development Tools

To develop FPGA applications, users need to prepare Xilinx Vivado 2018.3, Xilinx USB platform cable, XC7K325T development board and 6V DC power supply. Below image shows the Xilinx Vivado 2018.3 development environment which could be downloaded from Xilinx office website:

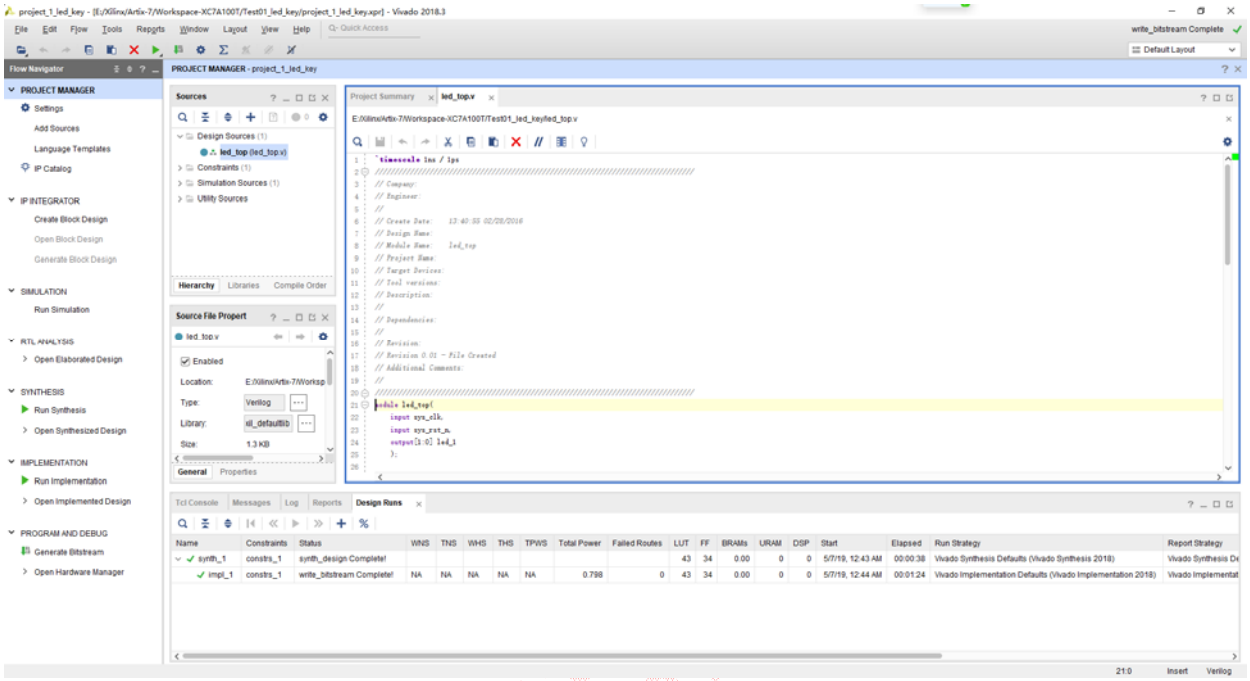


Figure 2-2. Vivado 2018.3

Below image shows the JTAG connection between Xilinx USB platform cable and development board:

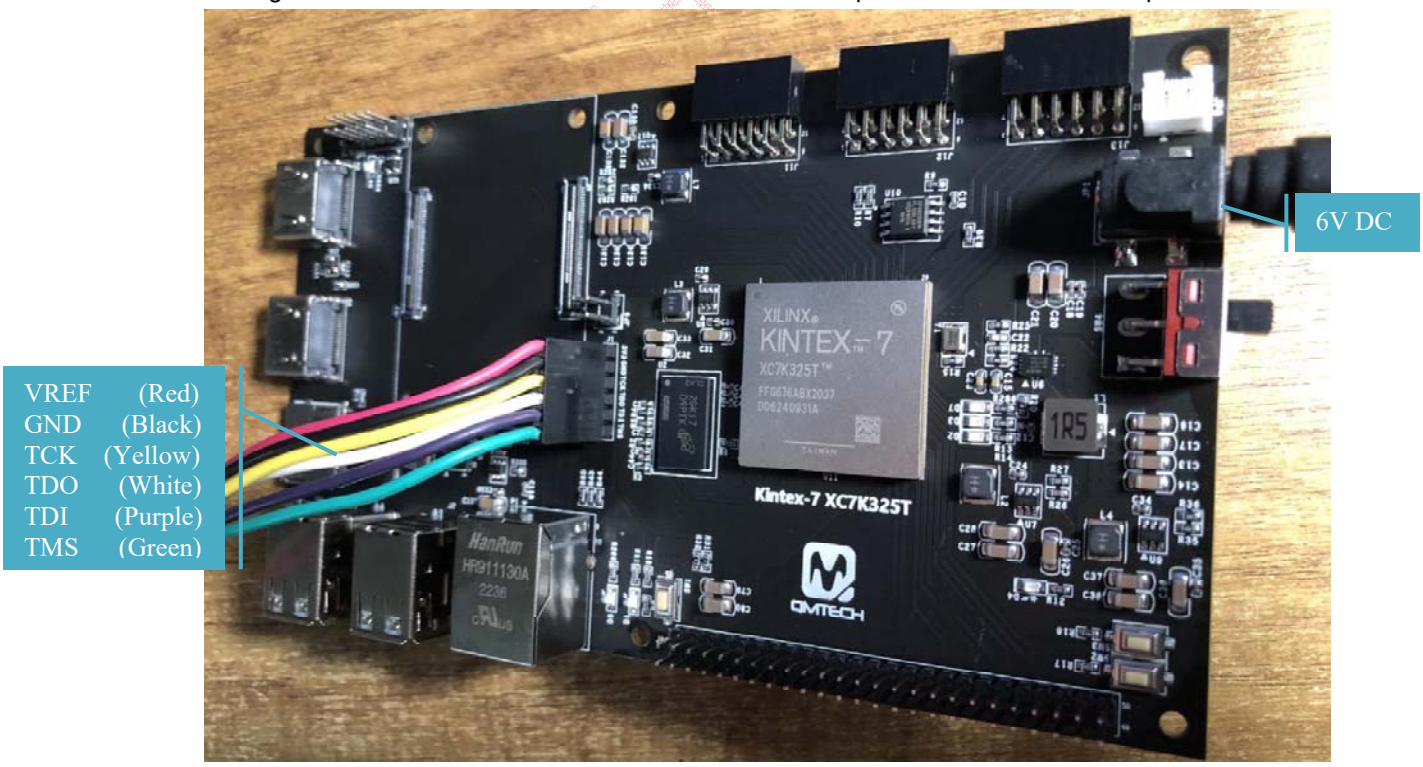
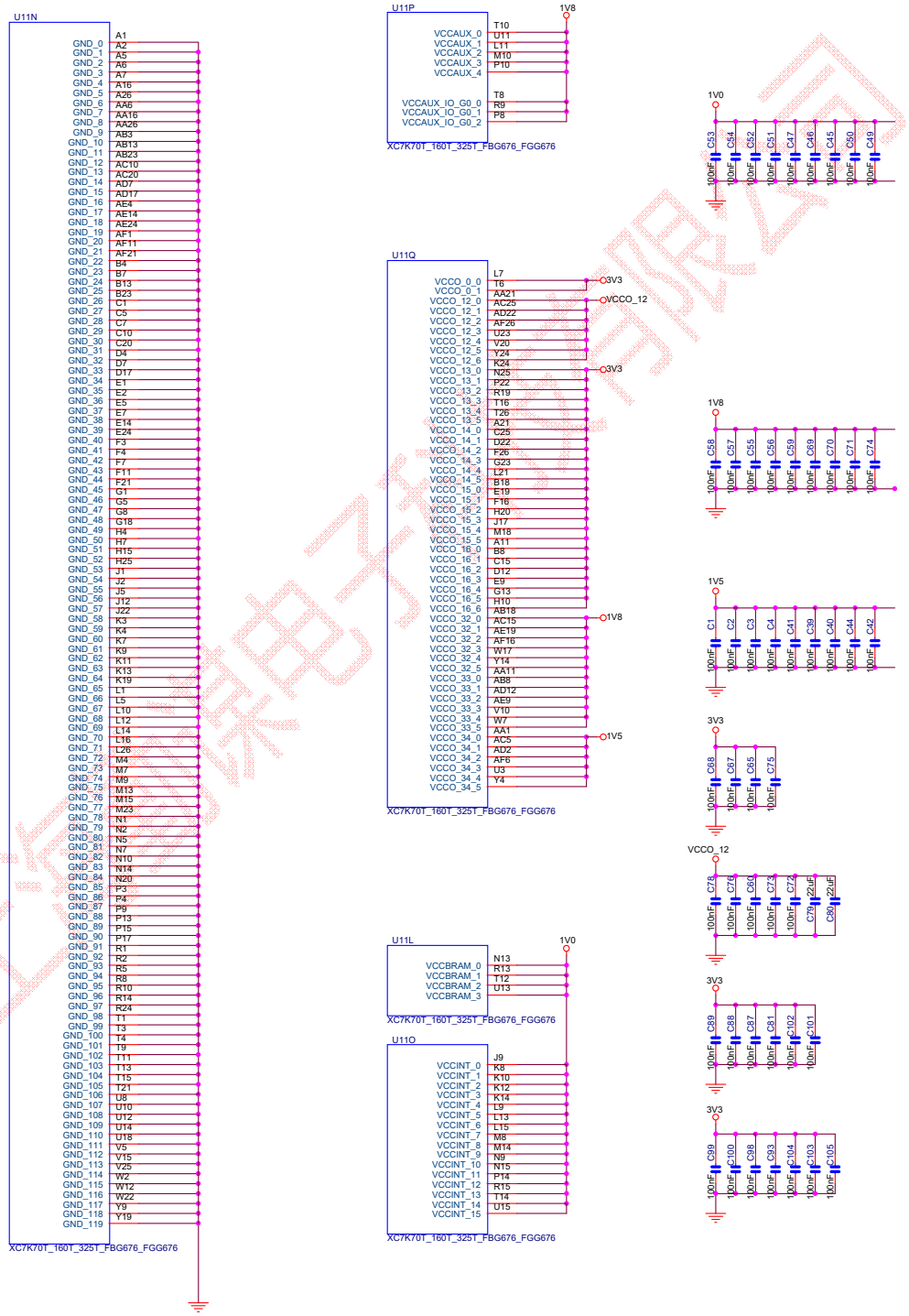


Figure 2-3. JTAG Connection and Power Supply

2.2 QMTECH XC7K325T Development Board Hardware Design

2.2.1 FPGA Power Supply

The development board needs **6V** DC input as power supply which could be directly injected from power header **JP1**. The on board LED D4 indicates the 3.3V supply status, it will be turned on when the **6V** power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V. However, BANK12 IO's voltage level can be changed according to detailed custom requirement. There're two 0 ohm resisters can be removed: R31/R32, and instead the BANK12's power supply can be injected from 50P male header JP5. Detailed design refers to HW schematic.



2.2.1 FPGA 1.0V Core Power Supply

The FPGA's power on sequence is as this: 1.0V -> 1.8V -> 1.5V & 3.3V. The FPGA core voltage 1.0V power supply is using high efficiency DC/DC chip MP8712 provided by MPS Inc. The MP8712 supports wide voltage input range from 3V to 18V. In normal use case, 6V DC power supply is suggested to be applied on the board. Below image shows the MP8712 hardware design:

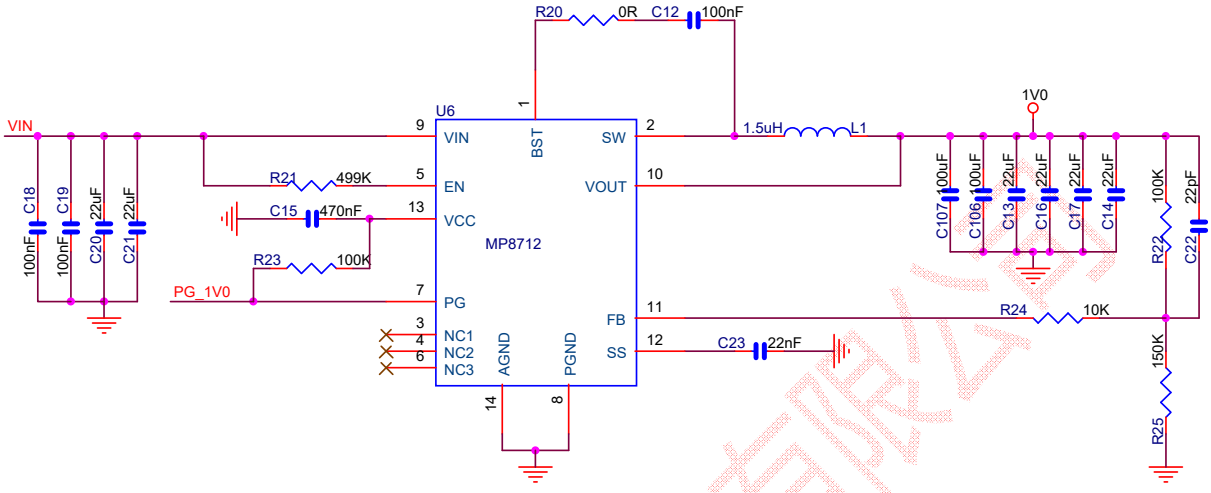


Figure 2-4. MP8712 Hardware Design

2.2.2 System Clock

FPGA chip XC7K325T-1FFG676C has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

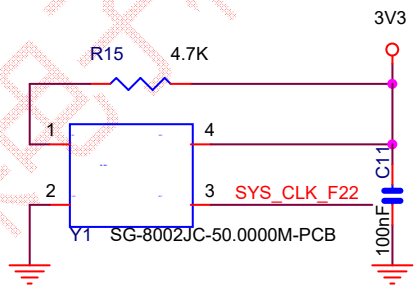


Figure 2-5. 50MHz System Clock

2.2.3 SPI Flash Boot

In default, the FPGA XC7K325T boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using S25FL128L manufactured by Infineon(Spansion), with 128Mbit memory storage.

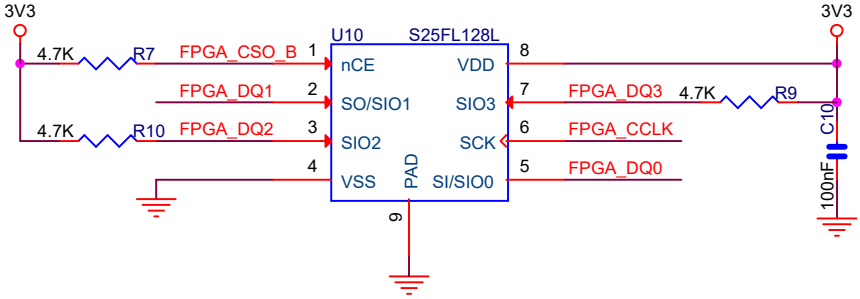


Figure 2-6. SPI Flash

The FPGA boot sequence setting M0:M1:M2 is configured as 1:0:0 which indicates FPGA will boot from SPI Flash after power on.

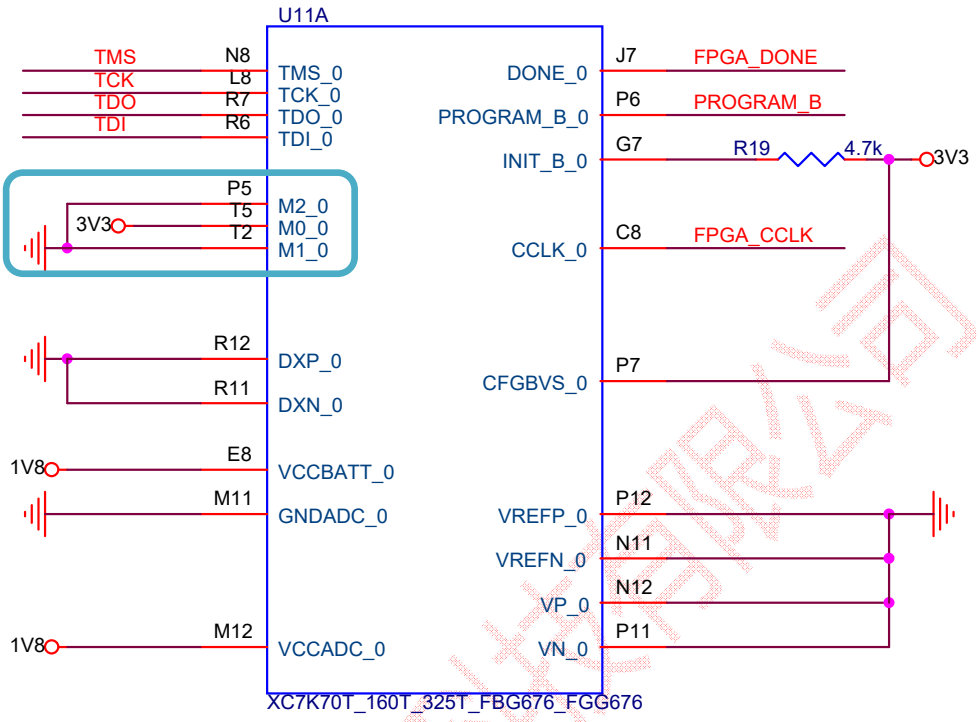


Figure 2-7. M0:M1:M2 Hardware Settings

The LED D1 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D1 could be used as FPGA loading status indicator.

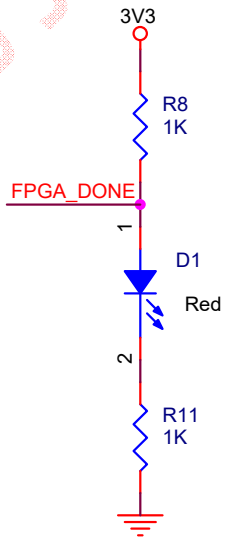


Figure 2-8. FPGA_DONE Status Indicator

2.2.4 User Extension IOs

The development board has one 50P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

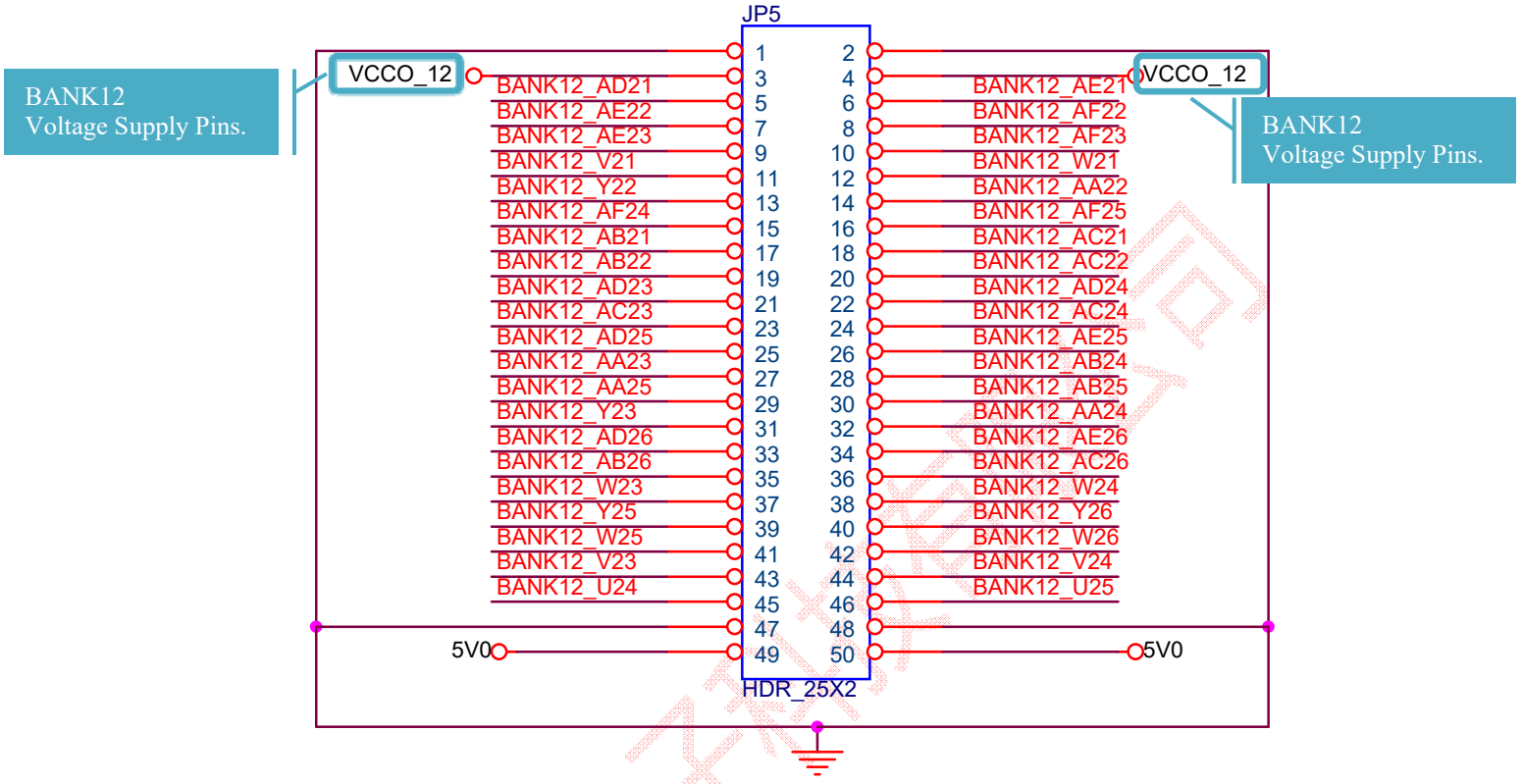


Figure 2-9. Extension IO

2.2.5 JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

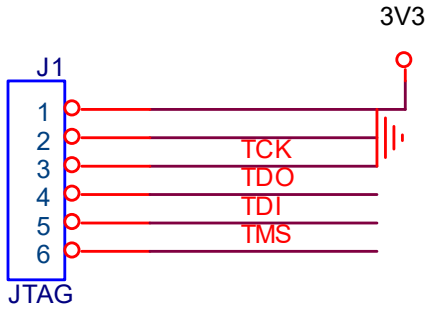


Figure 2-10. JTAG Port

2.2.6 User LEDs

Below image shows three user LEDs:

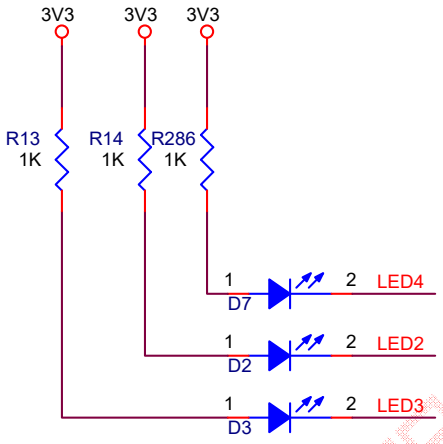


Figure 2-11. User LEDs

Below table shows the connection between XC7K325T and user LEDs.

Number	LED Name	XC7K325T Pin Number
1	D2	R26
2	D3	P26
3	D7	N26

2.2.7 User Keys

Below image shows the PROGRAM_B key and two user keys:

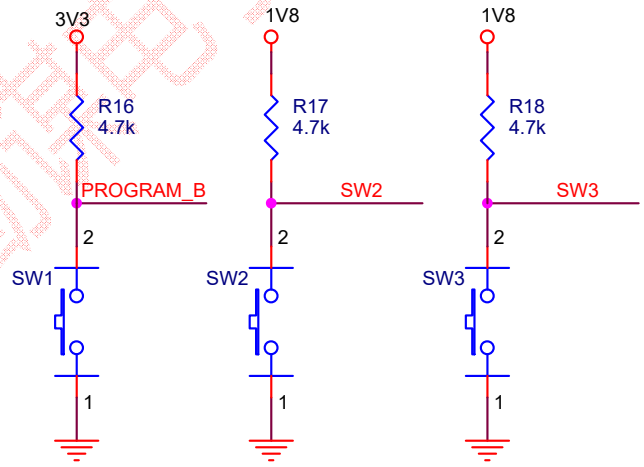


Figure 2-12. Keys

Below table shows the connection between XC7K325T and user keys.

Number	Key Name	XC7K325T Pin Number
1	SW2	V26
2	SW3	U26

2.2.8 DDR3 Memory

The development board has on board 16bit width data bus, 256MB memory size DDR3 MT41K128M16JT-125:K provided by Micron. Below image shows the detailed hardware design:

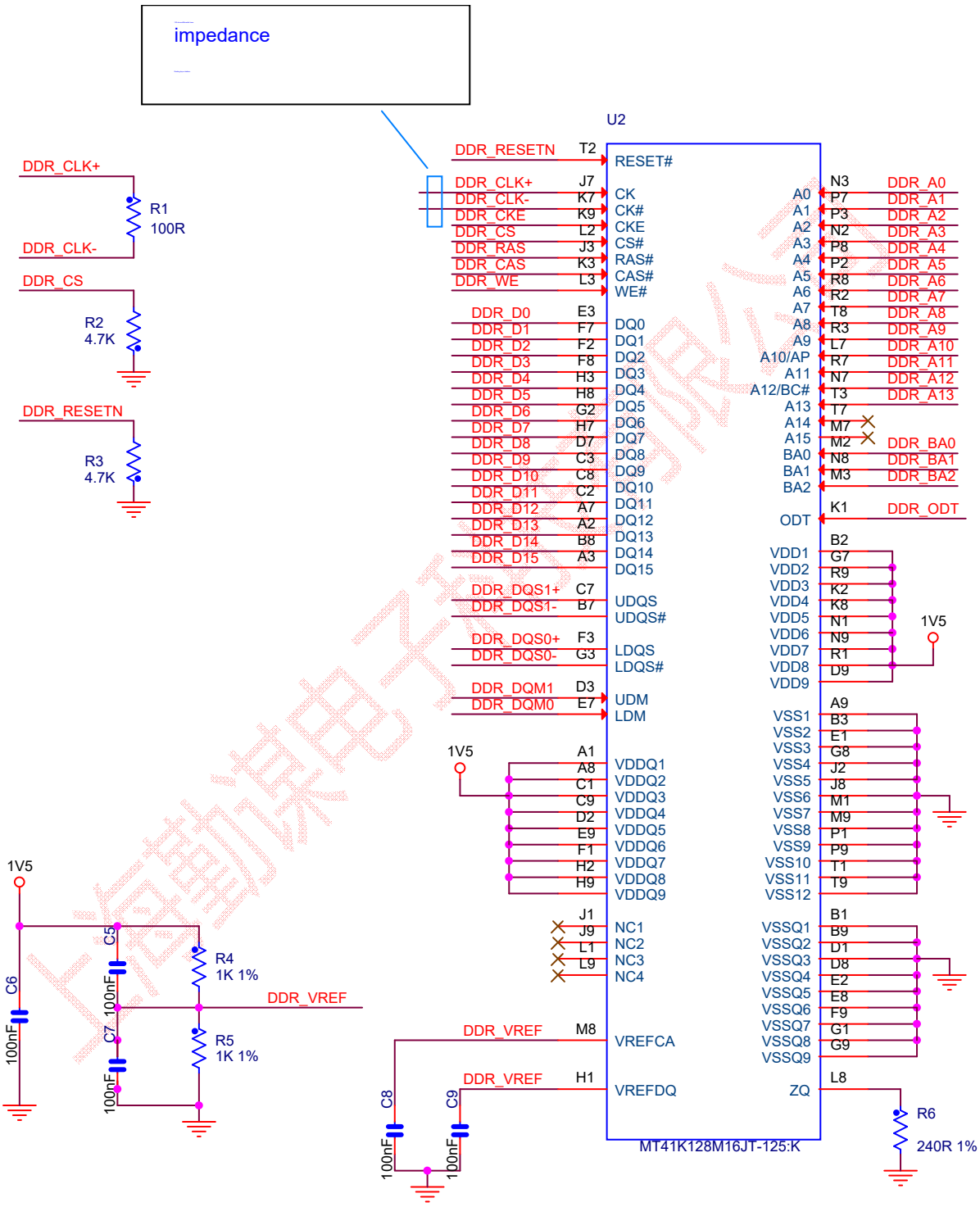


Figure 2-13. DDR3

2.2.9 GPIOs Connected to Computer Module

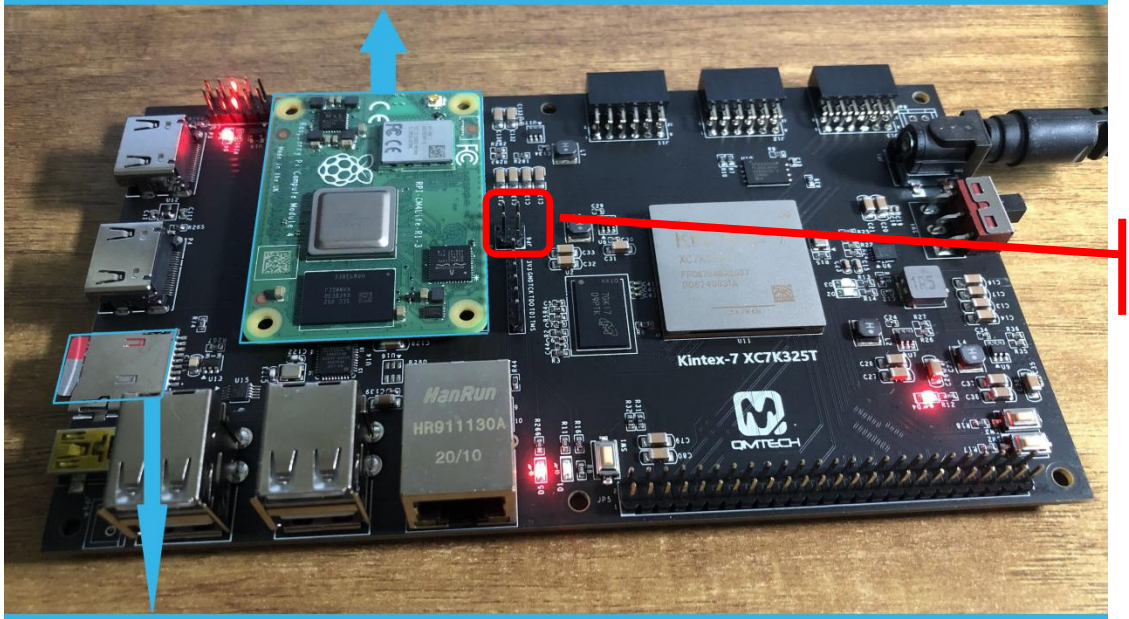
The development board provides connectors that could be used to make use of Raspberry Pi CM4 module or other compatible computer modules. The development board contains many of the interfaces for the Raspberry Pi CM4. Such as HDMI display port, ethernet interface, USB hub, TF card slot, etc.

Below image shows the example setup for the XC7K325T development board and RPi CM4 module. Notifications:

(1). Users need to prepare a TF card. And flash the linux image into the TF card. The linux images can be downloaded from here: http://downloads.raspberrypi.org/nightlies/
(2). Leave the **JP6** open because pin 86 and pin 88 are voltage output pins from RPi CM4.

86	CM4_3.3V (Output)	3.3V +/-2.5% Power Output max 300mA per pin for a total of 600mA. This will be powered down during power off or GLOBAL_EN being set low
87	+5V (Input)	4.75V-5.25V Main power input
88	CM4_1.8V (Output)	1.8V +/-2.5% Power Output max 300mA per pin for a total of 600mA. This will be powered down during power off or GLOBAL_EN being set low

Notice:
The Raspberry Pi CM4 module shown in below image is not sold by QMTECH. It is used for explaining the connection between the CM4 module and XC7K325T board.



Notice:
The TF card shown in the above image is not included in the XC7K325T board. The TF card is used for storing the RPi CM4 linux image. Users need to prepare the TF cards by themselves for RPi CM4 testing.

The GPIOs are used for the communication between XC7K325T and RPi CM4 module. Users may also configure the GPIOs into Secondary mem Address bus at RPi CM4 side to get faster communication speed.
Below table shows the connection between XC7K325T and GPIOs.

Number	GPIO Name(RPi CM4)	XC7K325T Pin Number
1	GPIO0	C12
2	GPIO1	B11
3	GPIO2	C18
4	GPIO3	D18
5	GPIO4	E18
6	GPIO5	C11
7	GPIO6	D10
8	GPIO7	B12
9	GPIO8	A12
10	GPIO9	D14
11	GPIO10	C13
12	GPIO11	D13
13	GPIO12	A10
14	GPIO13	E10
15	GPIO14	C17
16	GPIO15	A15
17	GPIO16	B10
18	GPIO17	D16
19	GPIO18	B15
20	GPIO19	B9
21	GPIO20	A9
22	GPIO21	A8
23	GPIO22	C14
24	GPIO23	A14
25	GPIO24	B14
26	GPIO25	A13
27	GPIO26	C9
28	GPIO27	D15

3. Reference

[1] ug470_7Series_Config.pdf
[2] ds182_Kintex_7_Data_Sheet.pdf
[3] ug475_7Series_Pkg_Pinout.pdf
[4] S25FL128L_S25FL128L_256-MB_32-MB_128-MB_16-MB_3.0_V_FL-L_FLASH_MEMORY.pdf
[5] MT41K128M16.pdf
[6] TPS563201.pdf
[7] MP8712.PDF

4. Revision

Doc. Rev.	Date	Comments
0.1	01/12/2024	Initial Version.
1.0	25/03/2024	V1.0 Formal Release.