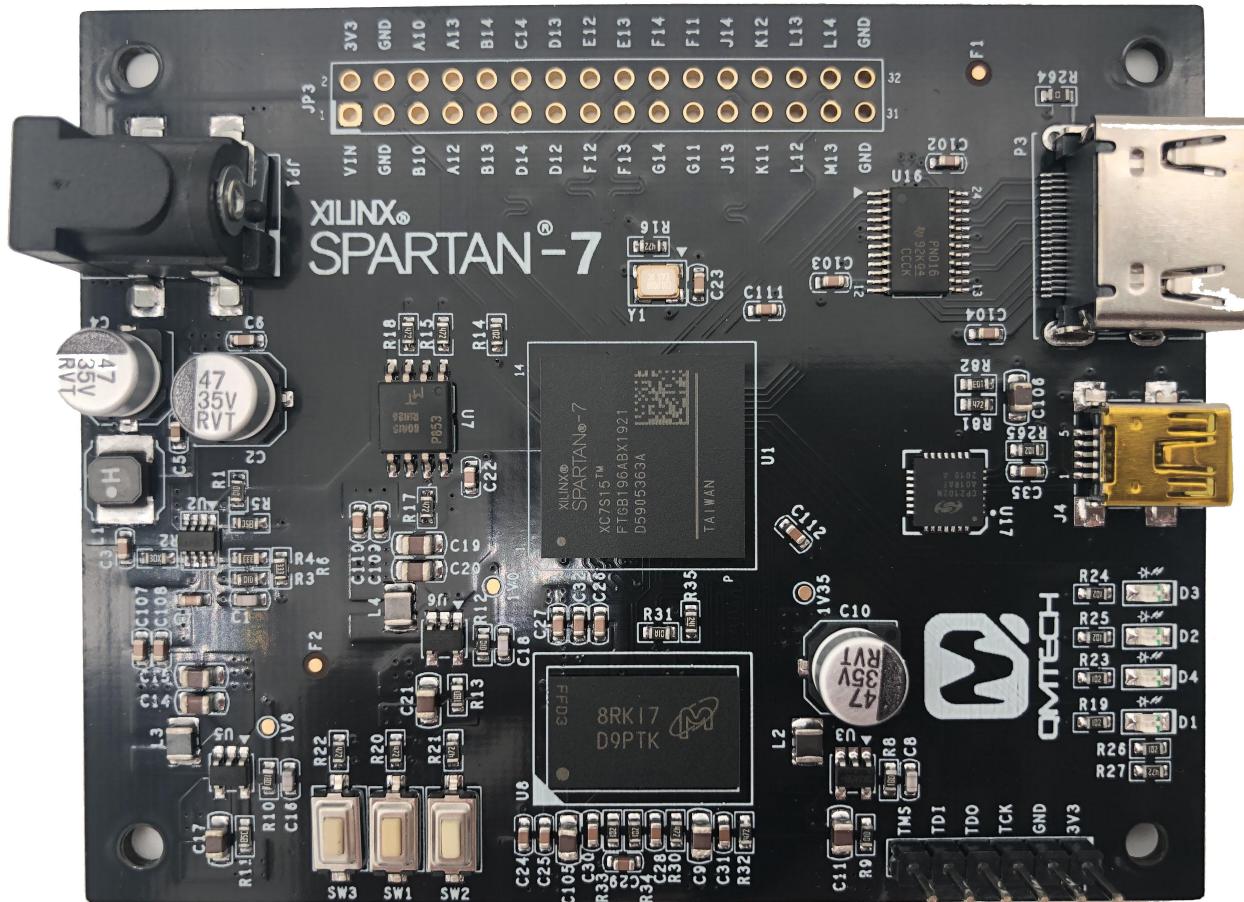


# QMTECH SPARTAN7 STARTER KIT

## USER MANUAL(EXPERIMENTS)



### Preface

The QMTECH® Spartan-7 Starter Kit uses Xilinx XC7S15 device to demonstrate the newest addition to the Cost-Optimized Portfolio, offer the best in class performance per watt, along with small form factor packaging to meet the most stringent requirements. These devices feature a MicroBlaze™ soft processor running over 200 DMIPs with 800Mb/s DDR3 support built on 28nm technology. Additionally, Spartan-7 devices offer an integrated ADC, dedicated security features, and Q-grade (-40 to +125°C) on all commercial devices. These devices are ideally suited for industrial, consumer, and automotive applications including any-to-any connectivity, sensor fusion, and embedded vision.



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QMTECH Spartan-7 Starter Kit

User Manual V01

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## 1. Experiment (1): USB to Serial Port

The CP2102N is a USB 2.0 to serial port bridge chip designed by Silicon Labs. The CP2102N includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components are required for development. Below figure shows the hardware design of CP2102N on the QMTECH Spartan7 Starter Kit.

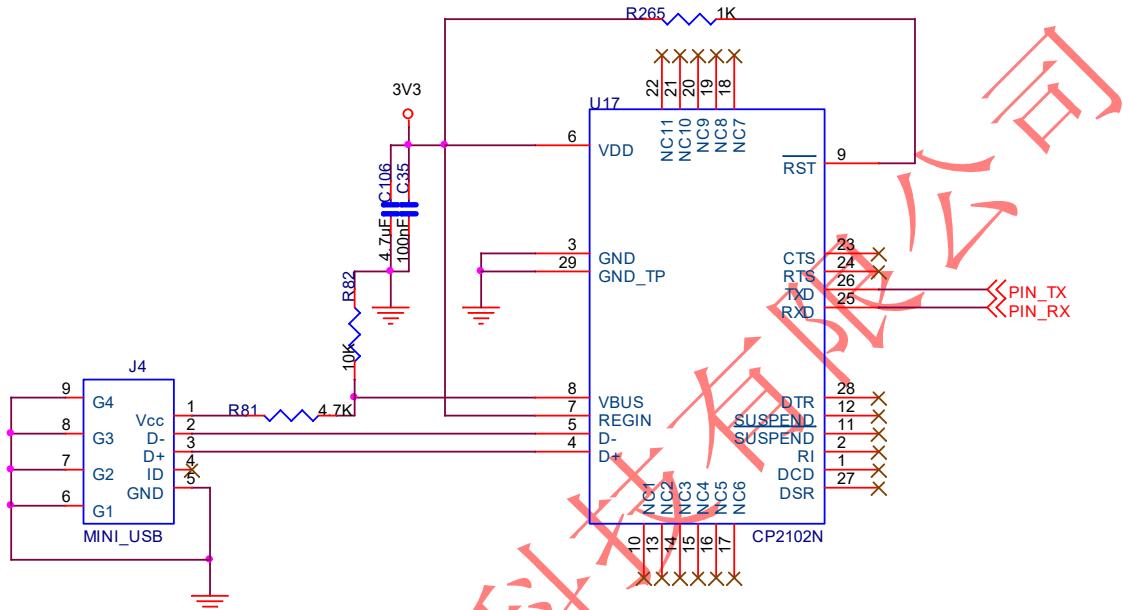
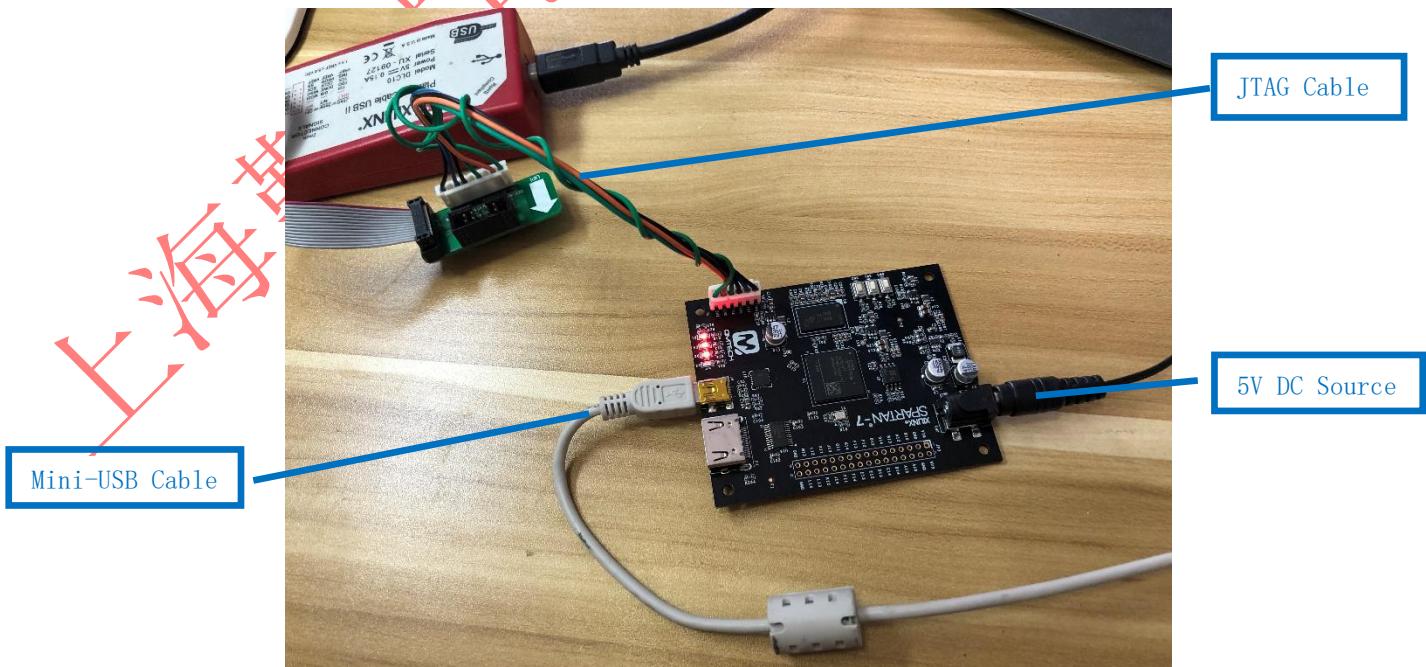
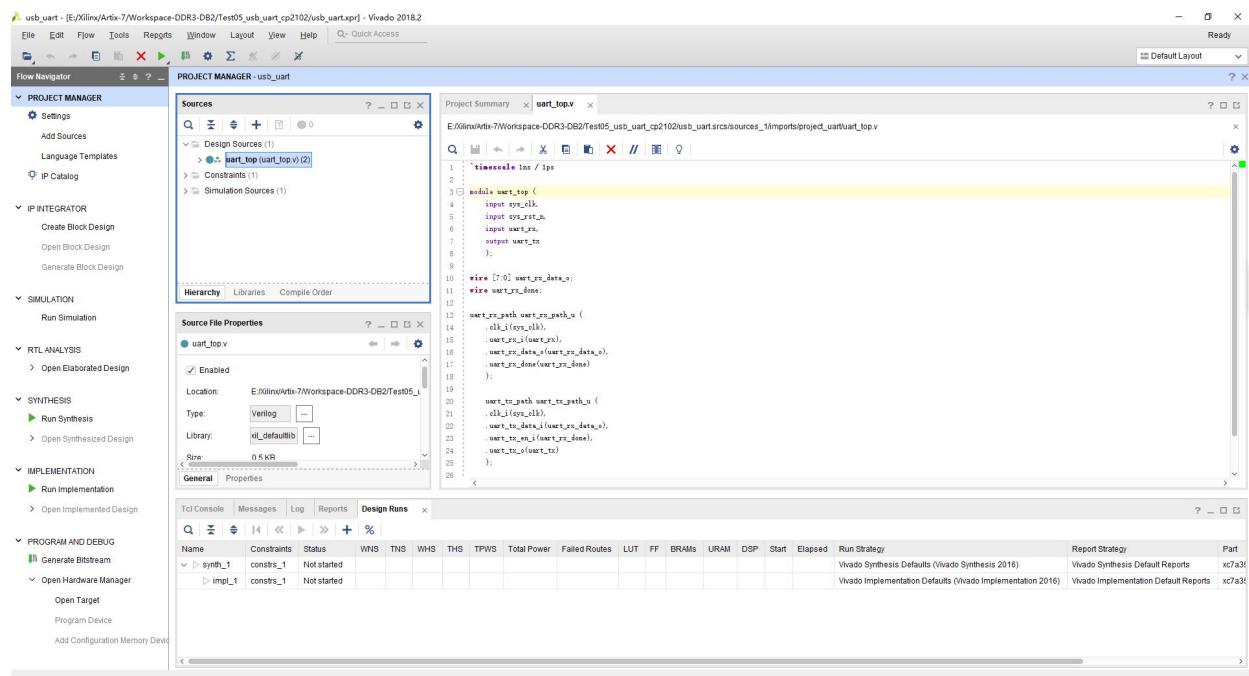


Figure 1-1. CP2102N Hardware Design

Before start to test the CP2102N's USB to UART serial communication function, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB platform cable's VREF, GND, TDI, TMS, TCK, TDO pins shall be connected to development board's JTAG interface. Then power on the development kit with 5V DC power source. Xilinx USB platform cable's indicator LED's color will turn from brown into green. At the same time, the Mini-USB cable shall also be plugged in the board, below figure shows an example hardware setup:



All the test examples are developed in the Vivado2018.3 environment. Open the CP2102 test project located in this release folder: /Software/project\_04\_UART. Below figure shows the project of [uart\\_top](#):



**Figure 1-2. CP2102 UART Communication Test Example**

In this example project, the default communication parameters are: 9600bps, 8 data bit, No Parity Check, 1 stop bit. If users want to test other communication parameters, change the source code accordingly.

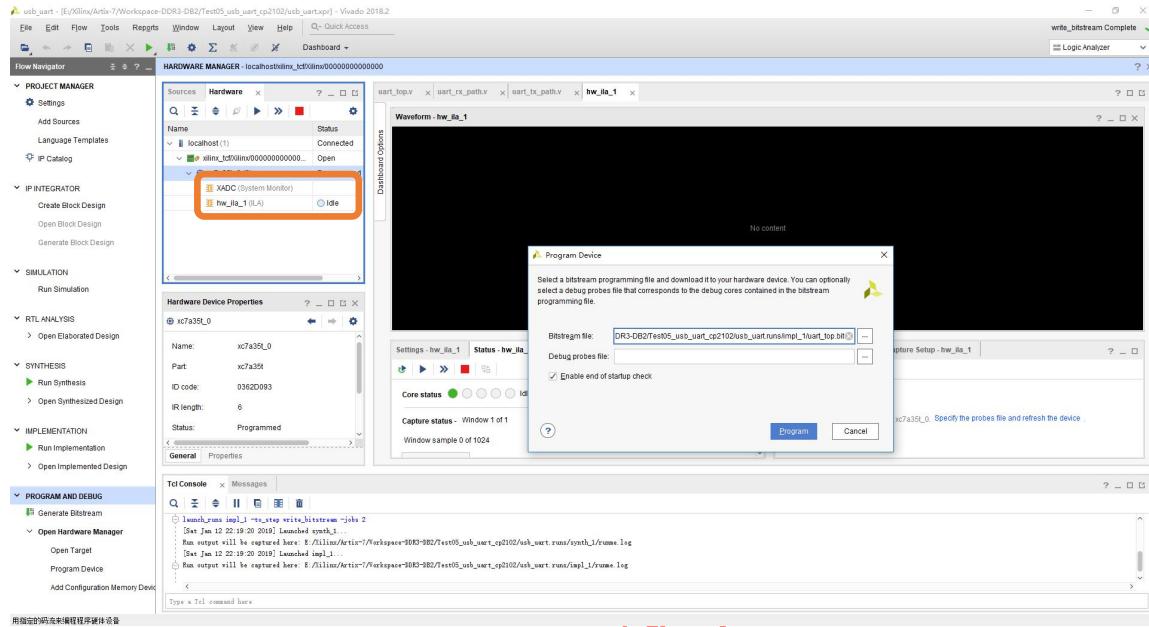
```

1 `timescale 1ns / 1ps
2
3 module uart_rx_path(
4     input clk_i,
5     input uart_rx_i,
6
7     output [7:0] uart_rx_data_o,
8     output uart_rx_done,
9     output baud_bps_tb           //for simulation
10 );
11
12 parameter [12:0] BAUD_DIV      = 13'd5208;    //波特率时钟, 9600bps, 50Mhz/9600=5208
13 parameter [12:0] BAUD_DIV_CAP = 13'd2604;    //波特率时钟中间采样点, 50Mhz/9600/2=2604
14
15 reg [12:0] baud_div=0;          //波特率设置计数器
16 reg baud_bps=0;                //数据采样点信号
17 reg bps_start=0;               //波特率启动标志
18 always@(posedge clk_i)
19 begin
20     if(baud_div==BAUD_DIV_CAP)   //当波特率计数器计数到采样点时, 产生采样信号baud_bps
21
22 module uart_tx_path(
23     input clk_i,
24
25     input [7:0] uart_tx_data_i,        //待发送数据
26     input uart_tx_en_i,              //发送使能信号
27
28     output uart_tx_o
29 );
30
31 parameter BAUD_DIV      = 13'd5208;    //波特率时钟, 9600bps, 50Mhz/9600=5208, 波特率可调
32 parameter BAUD_DIV_CAP = 13'd2604;    //波特率时钟中间采样点, 50Mhz/9600/2=2604, 波特率可调
33
34 reg [12:0] baud_div=0;          //波特率设置计数器
35 reg baud_bps=0;                //数据发送信号, 高有效
36 (* MARKDEBUG = "TRUE" *)reg [9:0] send_data=10'b1111111111;    //待发送数据寄存器, 1bit起始信号+8bit有效信号+1bit结束信号
37 (* MARKDEBUG = "TRUE" *)reg [3:0] bit_num=0;                   //发送数据个数计数器
38 reg uart_send_flag=0;          //数据发送标志位
39 reg uart_tx_o_r=1;             //发送数据寄存器, 初始状态位高
40
41 endmodule

```



After the CP2102N communication test project correctly synthesized, implemented and generated \*.bit file, users could use Vivado 2018.3 program tool to program the generated \*.bit file into FPGA. Below image shows the FPGA program status with program tool.



**Figure 1-3. Program \*.bit File**

The CP2102N example test project's main functionality is performing an UART loopback communication. The FPGA program will send the received UART data back to the PC. Below figure shows user employees some PC based UART test tool to send data to FPGA: <http://www.cmssoft.cn> QQ:10865600. After a short while the PC UART test tool will receive the same data stream from FPGA, which means the CP2102N loopback test program is running correctly.



**Figure 1-4. UART Loopback Test**

## 2. Experiment (2): HDMI Displays

Transition Minimized Differential Signaling (TMDS) is used for transmitting video data over the High-Definition Multimedia Interface (HDMI). The Spartan7 Starter Kit uses TI's TPD12S016 chip, which is a single-chip High Definition Multimedia Interface (HDMI) device with auto-direction sensing I2C voltage level shift buffers, a load switch, and integrated low capacitance high-speed electrostatic discharge (ESD) transient voltage suppression (TVS) protection diodes. Below image shows the hardware design.

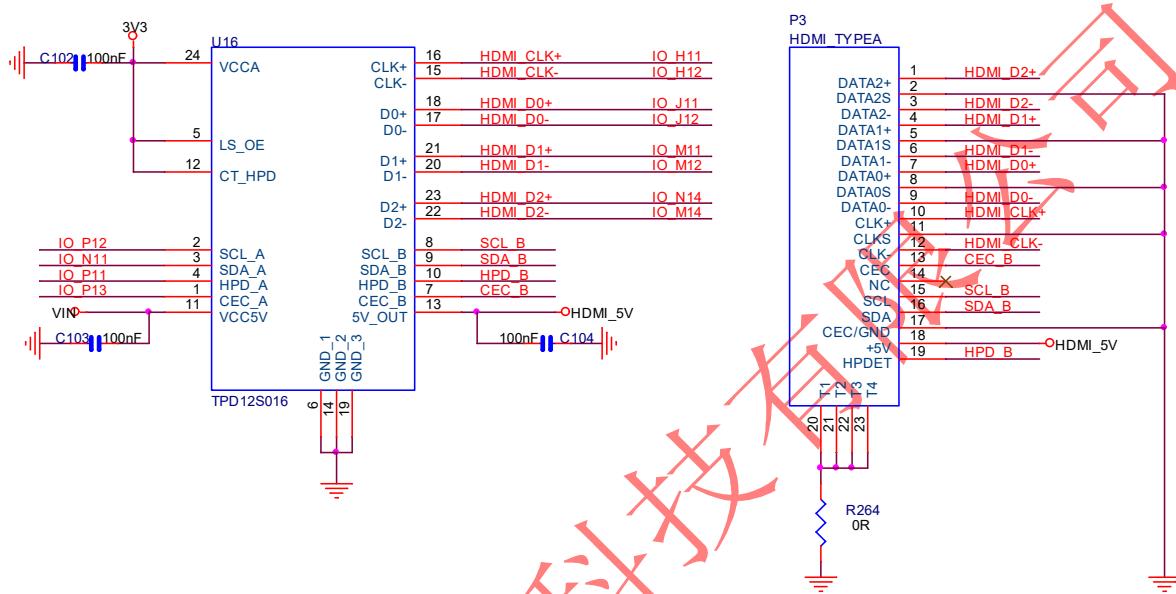
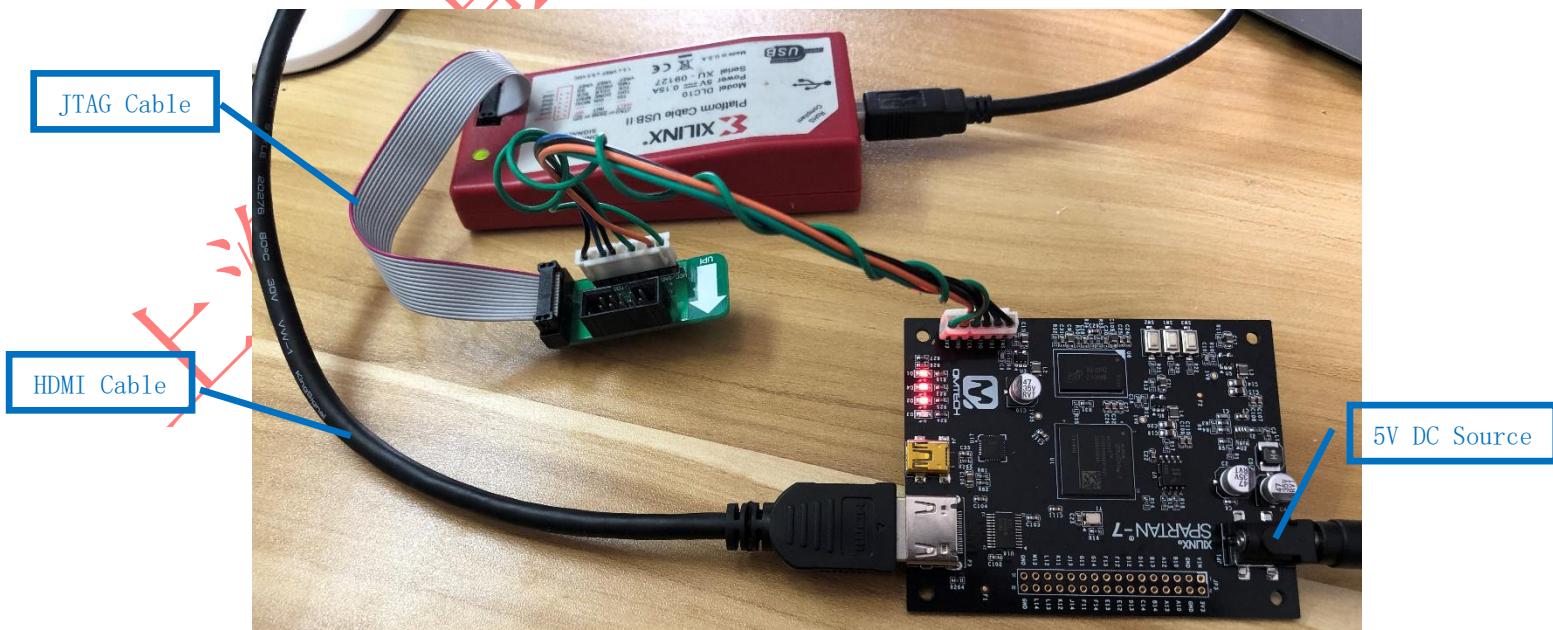
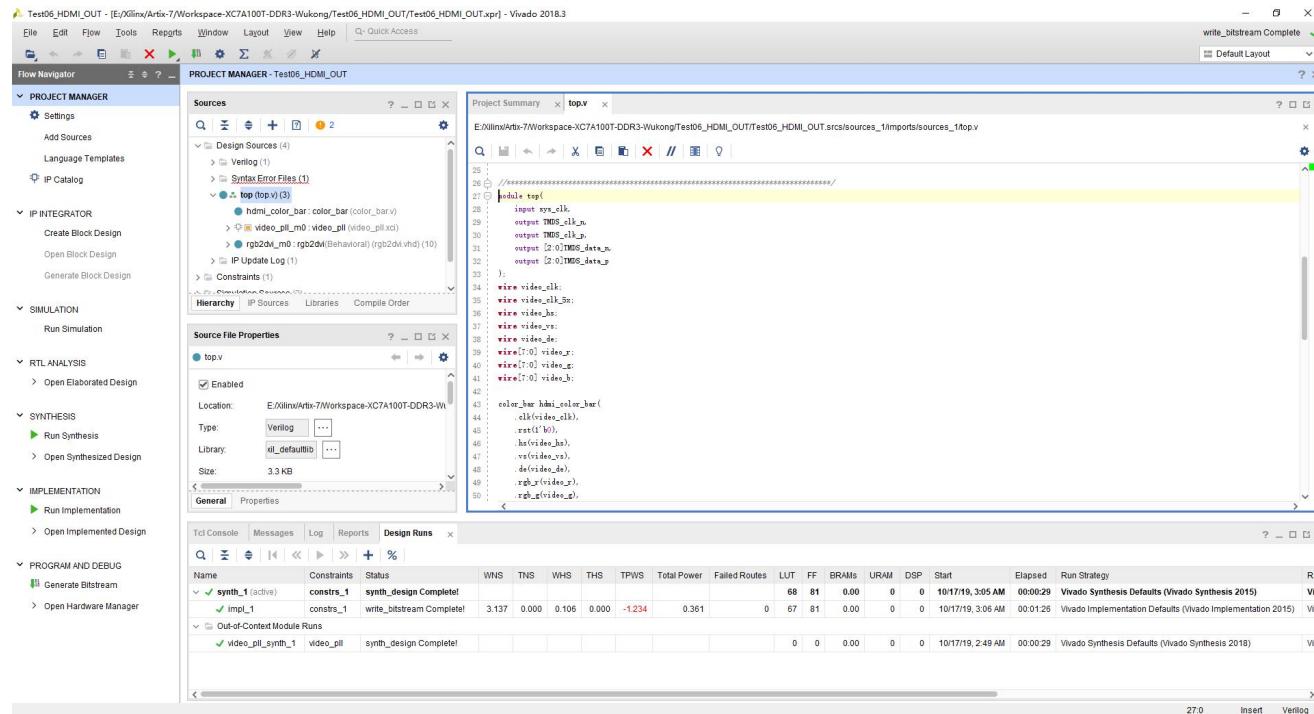


Figure 2-1. HDMI Display Hardware Designs

Before start to test the HDMI display function, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB platform cable's VREF, GND, TDI, TCK, TDO pins shall be connected to development board's JTAG interface. Then power on the development kit with 5V DC power source. Xilinx USB platform cable's indicator LED's color will turn from brown into green. At the same time, the HDMI cable shall also be plugged into the board, below figure shows an example hardware setup:

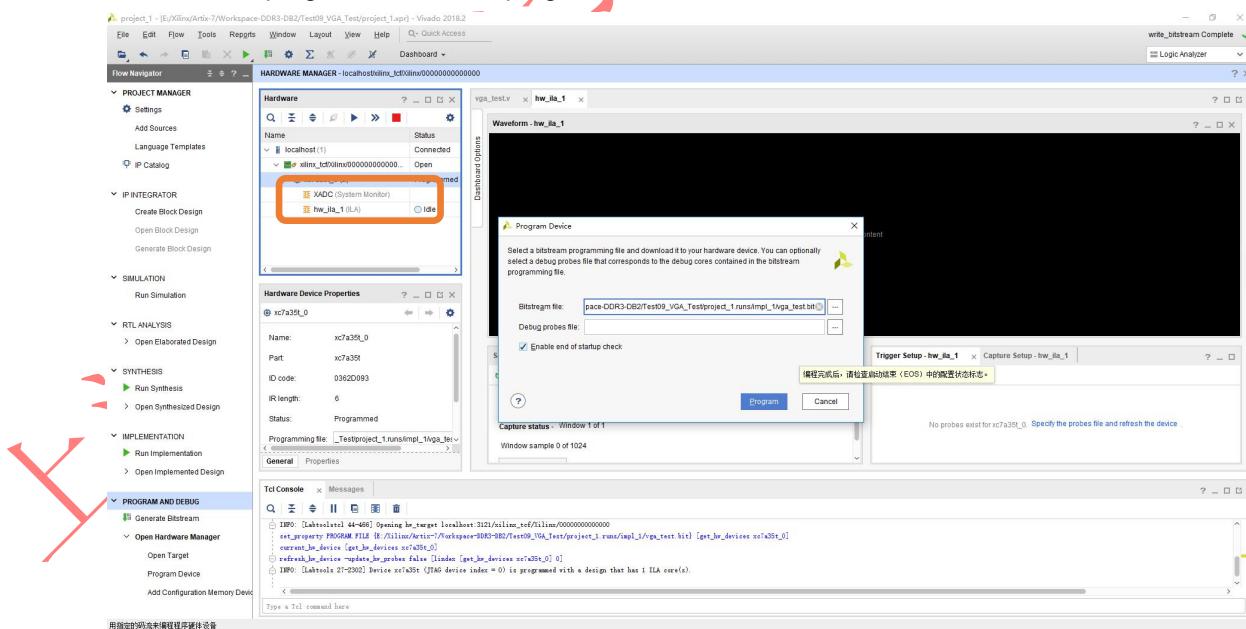


Open the HDMI test project located in this release folder: /Software/project\_06\_HDMI\_OUT. Below figure shows the example project of **project\_06\_HDMI\_OUT**:



**Figure 2-2. HDMI Display Function Test**

After the HDMI display test project correctly synthesized, implemented and generated \*.bit file, users could use Xilinx Vivado 2018.3 program tool to program the generated \*.bit file into FPGA. Below image shows the FPGA program status with program tool.



**Figure 2-3. Program FPGA**



After the FPGA correctly loaded the top.bit file, the HDMI monitor will display color bar pattern. Below image shows the example color bar pattern.

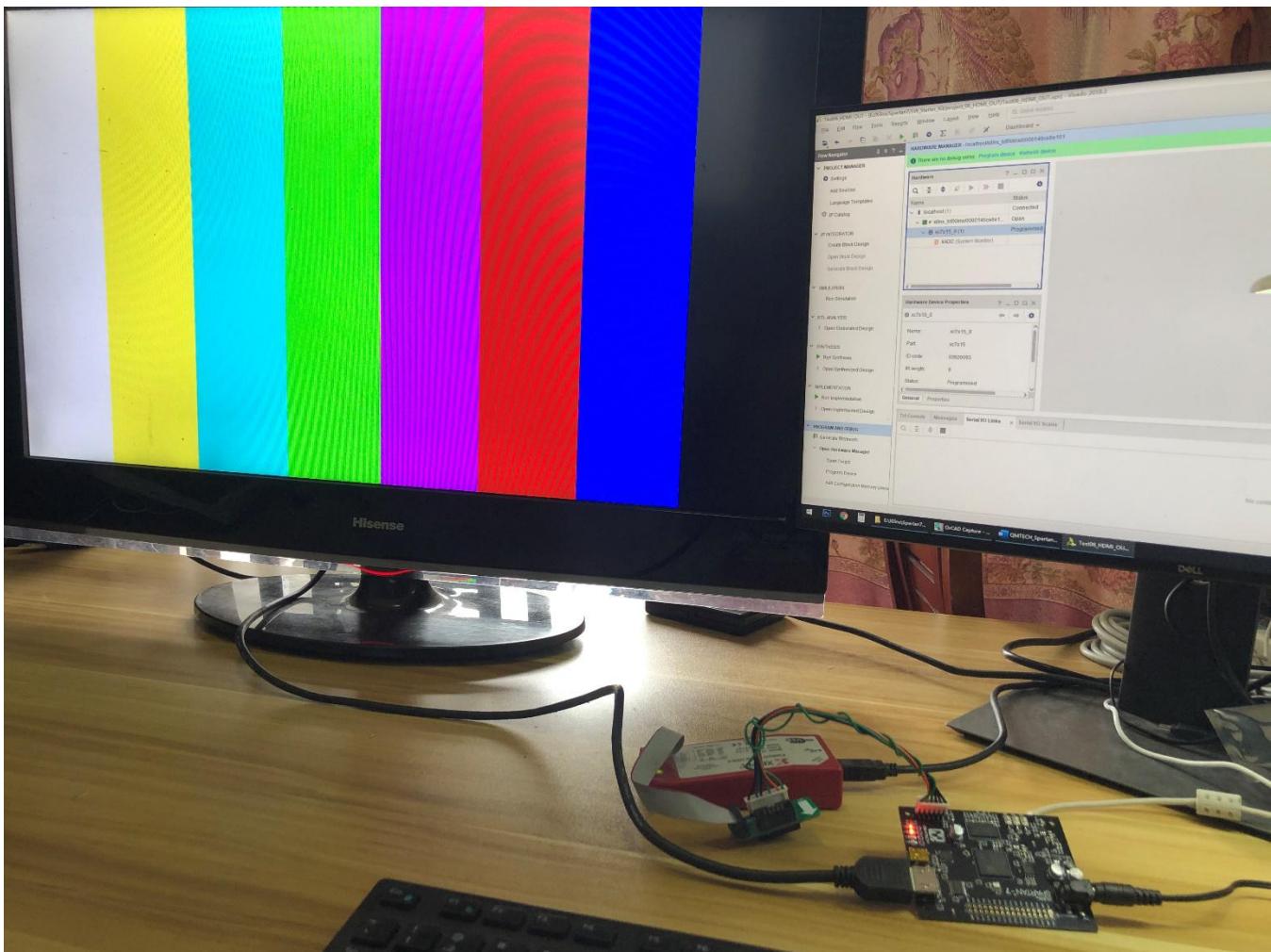


Figure 2-4. HDMI Display Test

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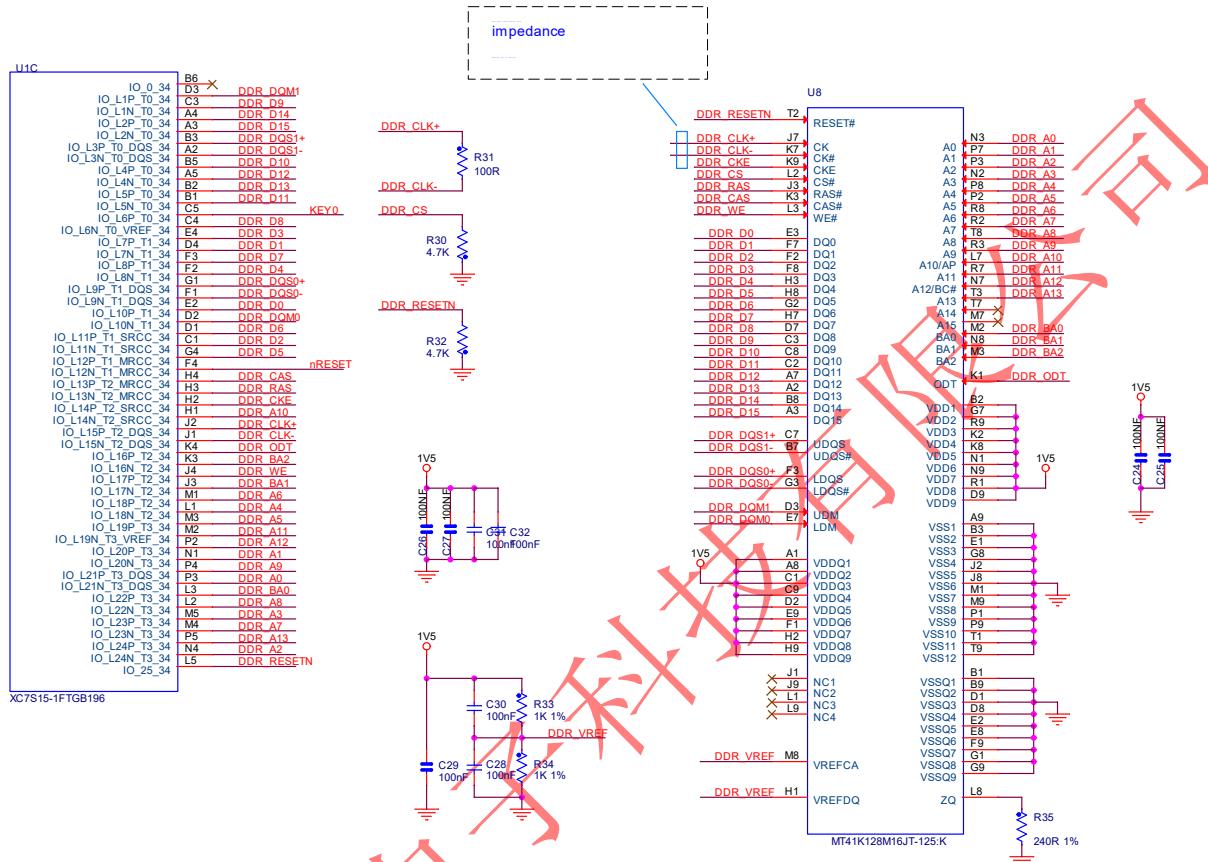
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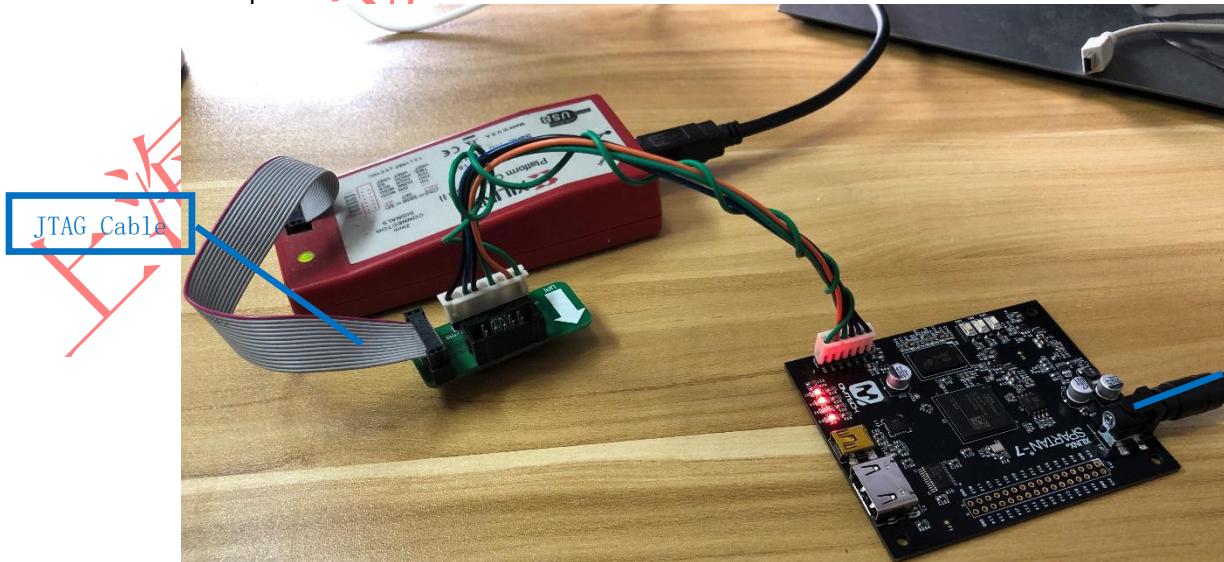
### 3. Experiment (3): DDR3 Memory Test

The Starter Kit has on board 16bit width data bus, 256MB memory size DDR3 MT41K128M16JT-125:K provided by Micron. Below image shows the detailed hardware design:

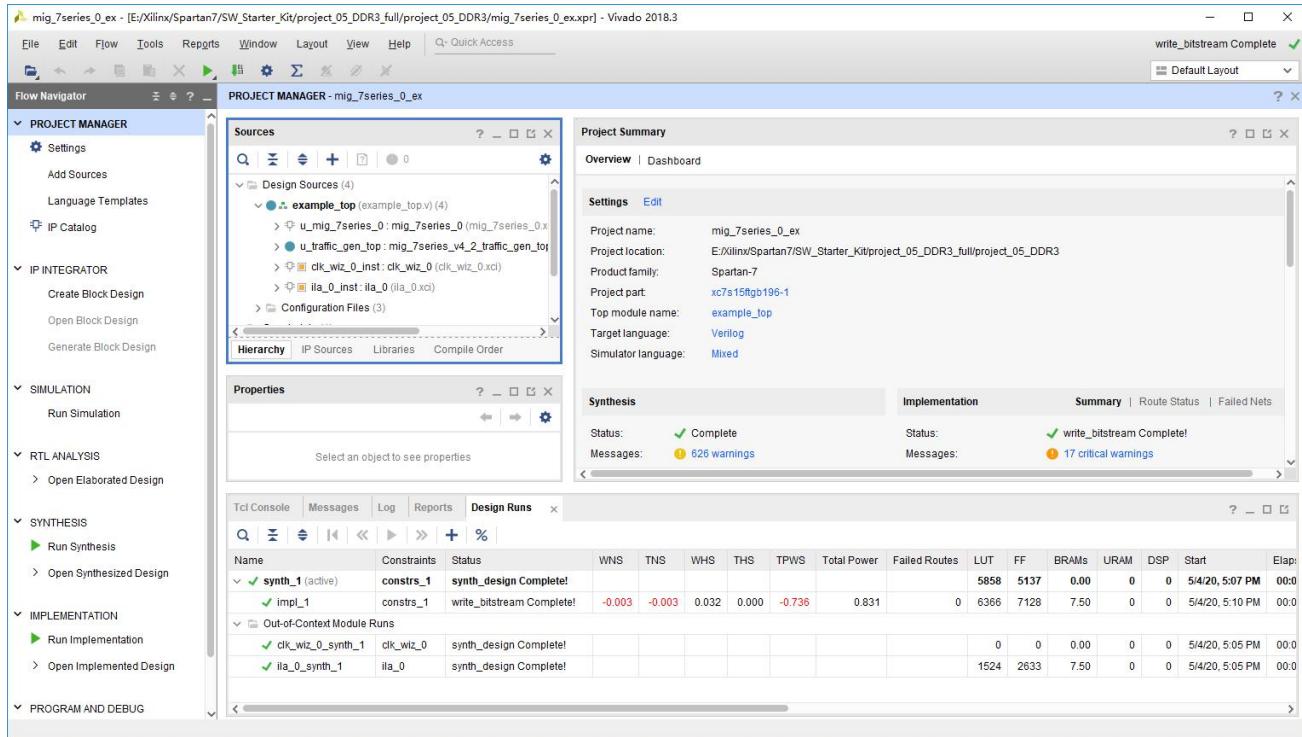


## Figure 3-1. RTL8211 Hardware Design

~~Before start to test the DDR3 memory, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB Platform cable shall be connected to development board's JTAG interface. Then power on the development kit with 5V DC power source. Below figure shows an example hardware setup:~~

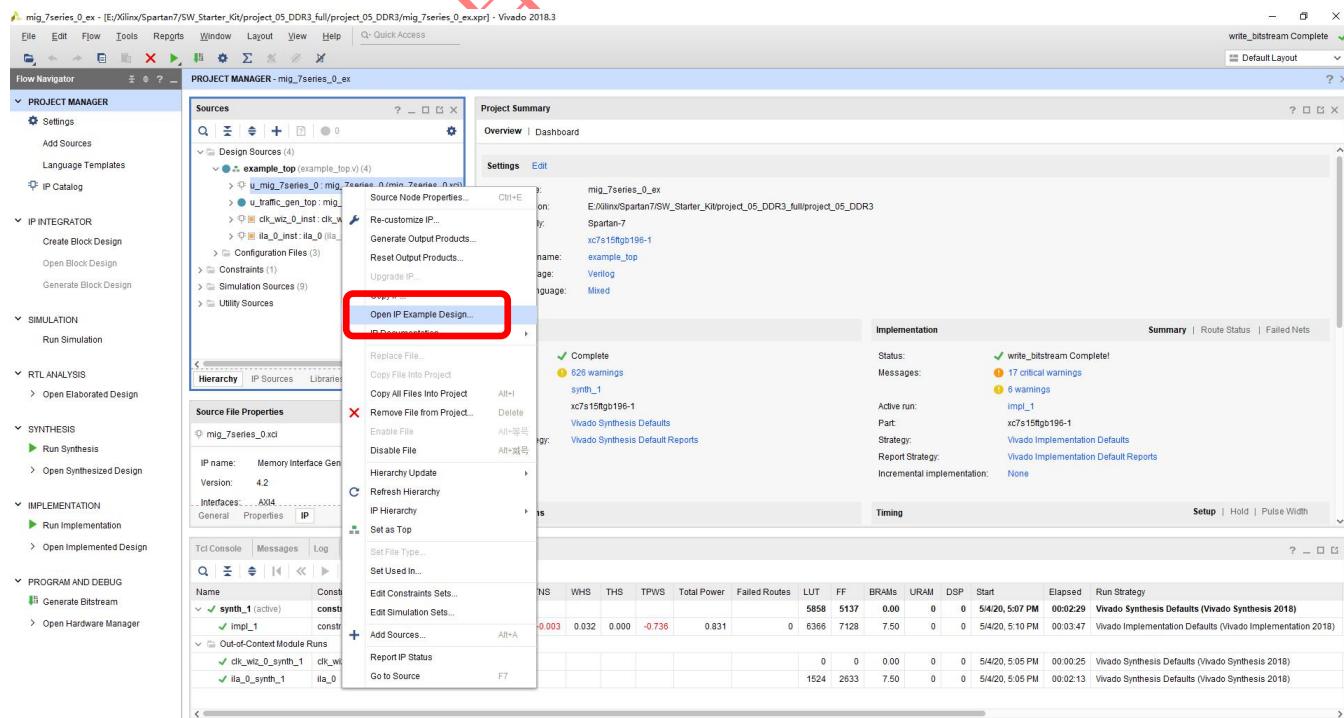


Use Vivado2018.3 to open the DDR3 memory test project located in this release folder: /Software/project\_05\_DDR3. Below figure shows the example project of [example\\_top](#):

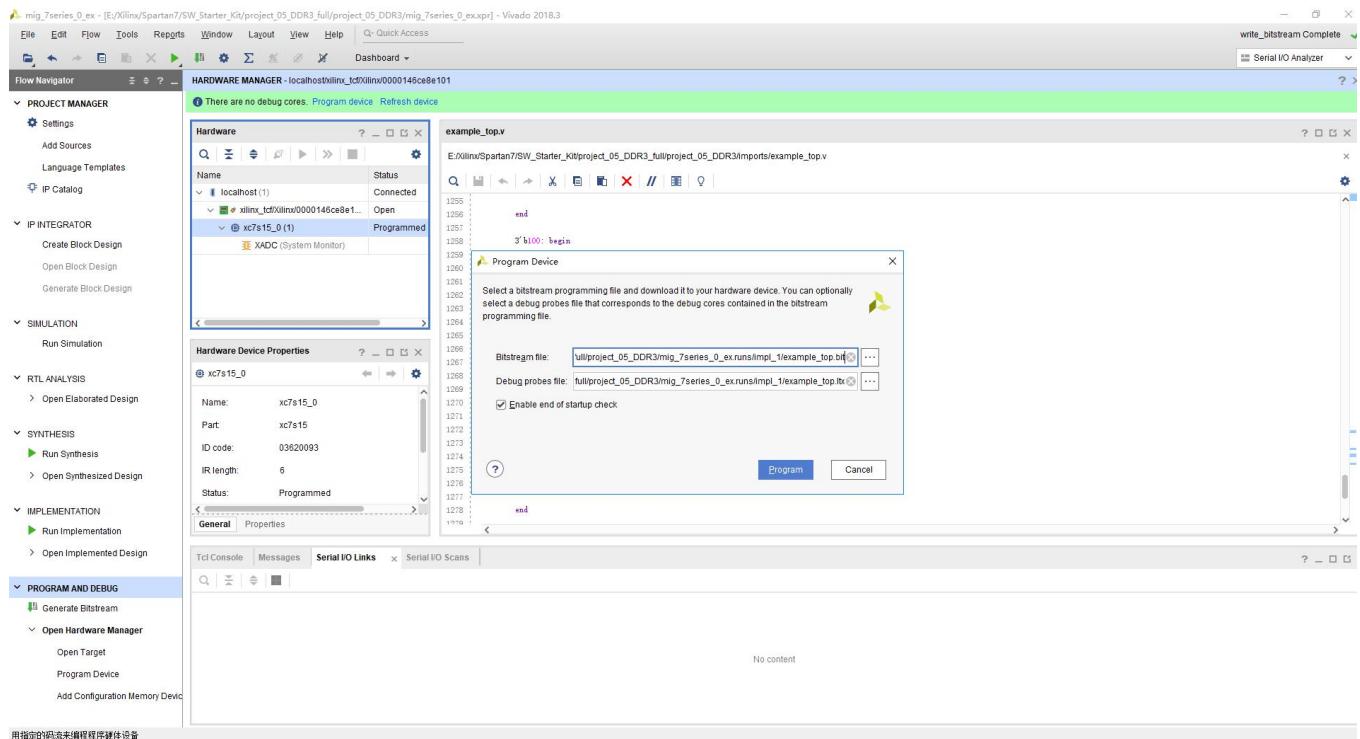


**Figure 3-2. FPGA Program**

This DDR3 test project is originally created by the Xilinx MIG IP tools. Users could create the test project by right click the **【mig\_7series\_0】** IP and select **【Open IP Example Design】**. Since the original ILA debug core takes too much RAM resources, there are many debug signals are deleted in this DDR3 test project. Users may add the necessary debug signals back by themselves.

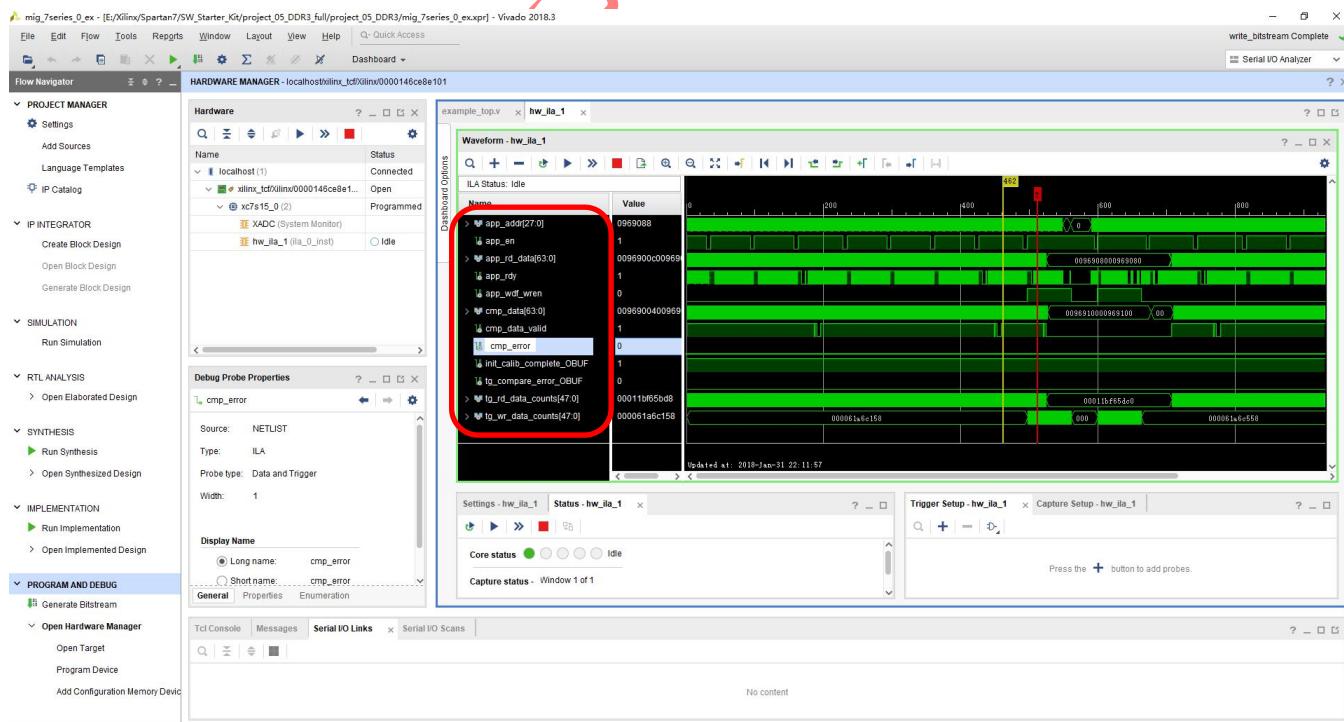


After the DDR3 memory test project correctly synthesized, implemented and generated \*.bit file, users could use Vivado 2018.3 program tool to program the generated \*.bit file into FPGA. Below image shows the FPGA program status with program tool.

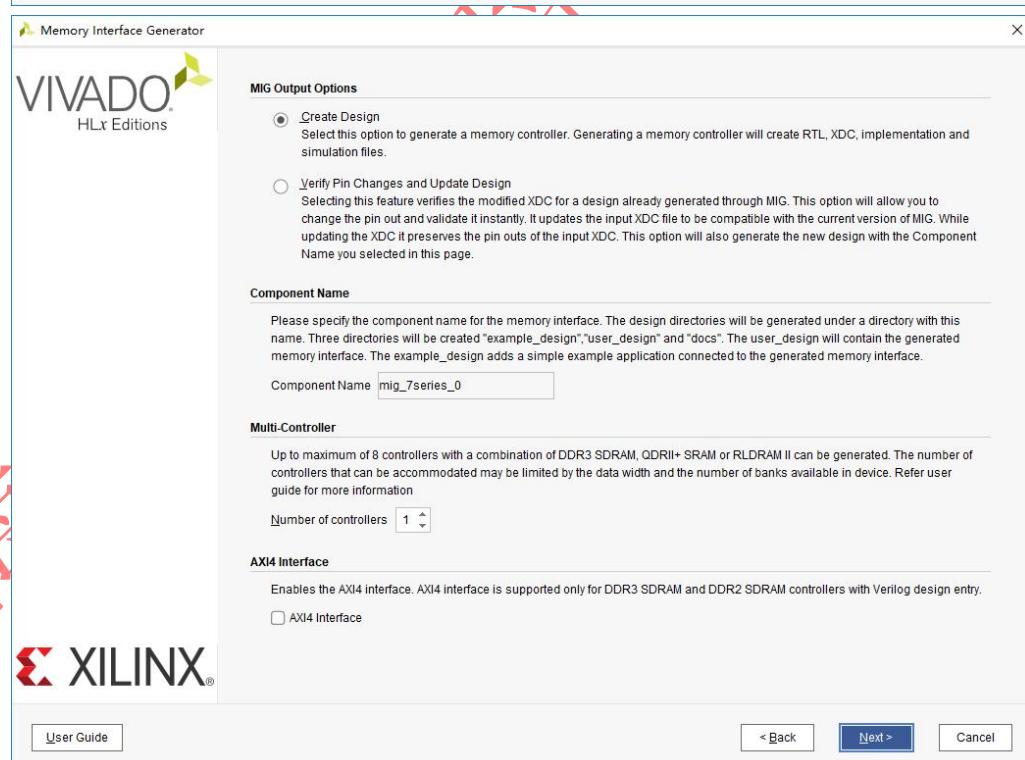
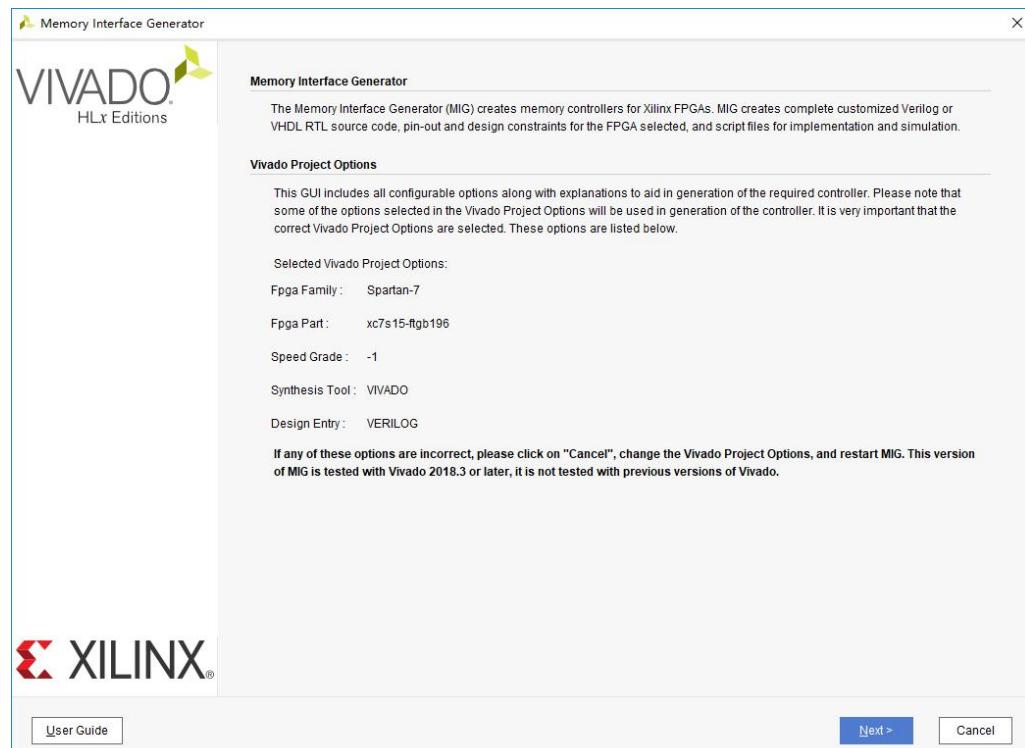


**Figure 3-3. FPGA Program**

Users could check the signals like init\_calib\_complete, cmp\_error etc in the ILA waveform window.



Below images list the example configurations for this MIG IP. Users may customize it if needed.



**Memory Interface Generator**

**VIVADO**  
HLx Editions

**Pin Compatible FPGAs**

Memory Selection  
Controller Options  
AXI Parameter  
Memory Options  
FPGA Options  
Extended FPGA Options  
IO Planning Options  
Pin Selection  
System Signals Selection  
Summary  
Simulation Options  
PCB information  
Design Notes

**Pin Compatible FPGAs**

Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default XDC in the par folder for the target part. If the target part is changed, use the appropriate XDC in the compatible\_xdc folder. If a Pin Compatible FPGA is not chosen now and later a different FPGA is used, the generated XDC may not work for the new device and a board spin may be required. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.

A blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.

Note that different parts in the same package will have different internal package skew values. De-rate the minimum period appropriately in the Controller Options page when different parts in the same package are used. Consult the User Guide for more information.

Target FPGA: xc7s15-ftgb196 -1

**Pin Compatible FPGAs**

spartan7

7s

- xc7s25-ftgb196
- xc7s50-ftgb196
- xc7s6-ftgb196

User Guide      < Back      Next >      Cancel

**Memory Interface Generator**

**VIVADO**  
HLx Editions

**Memory Selection**

Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA, speed grade and design entry chosen.

Select the controller type:

DDR3 SDRAM

DDR2 SDRAM

LPDDR2 SDRAM

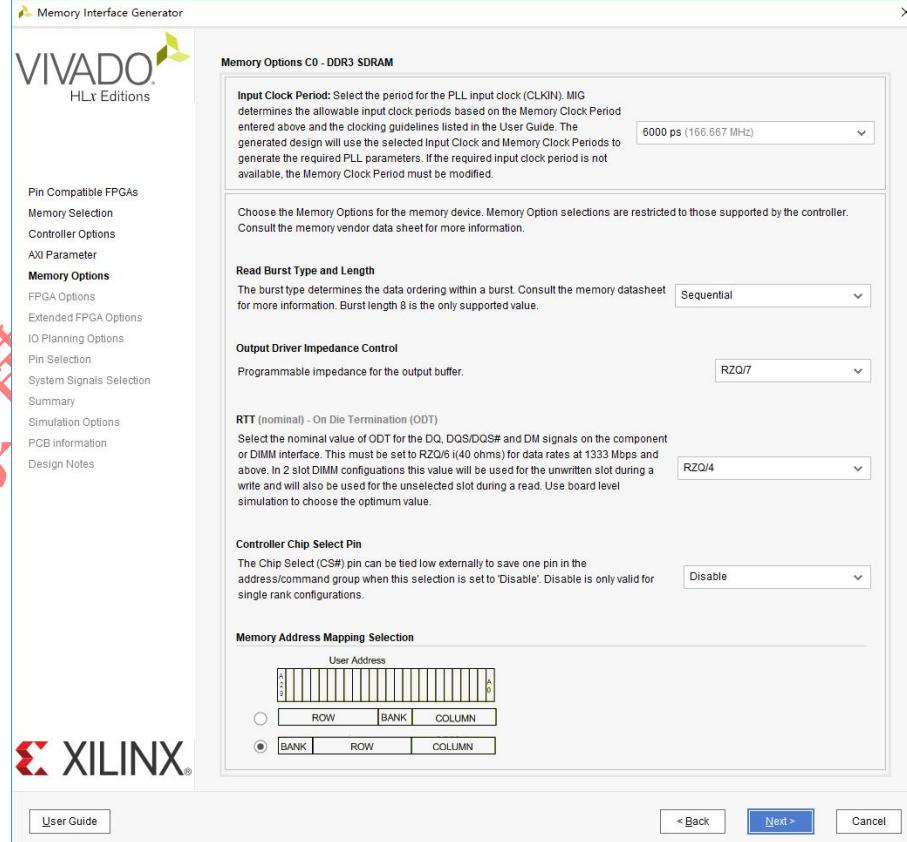
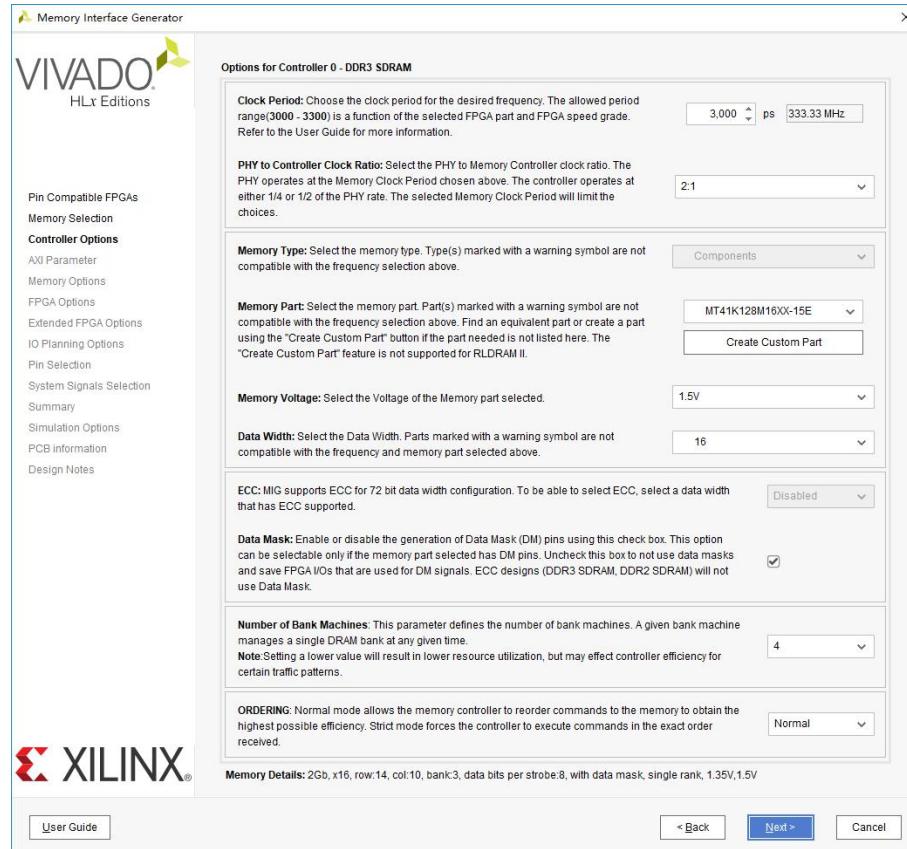
**Memory Selection**

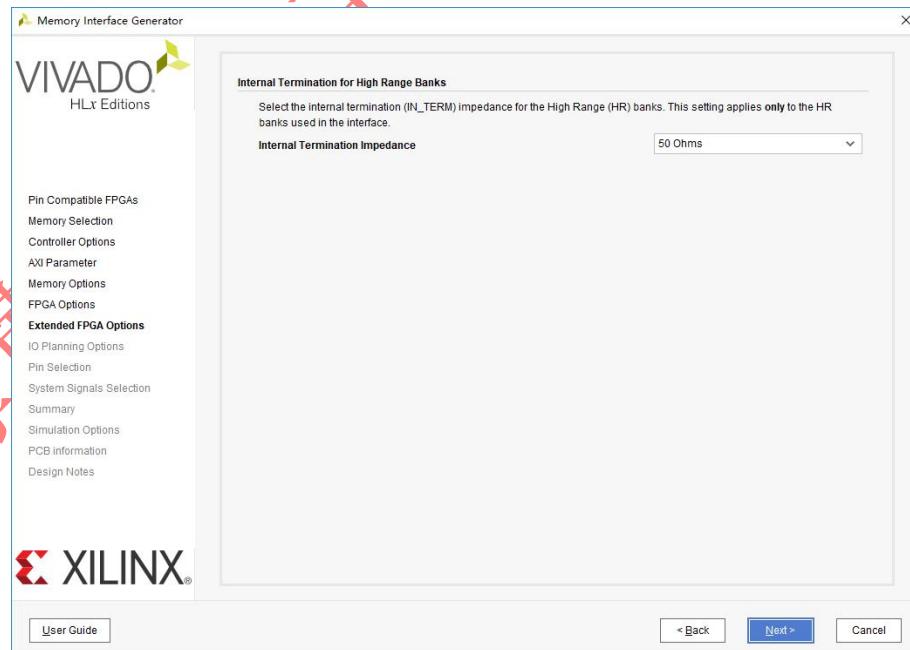
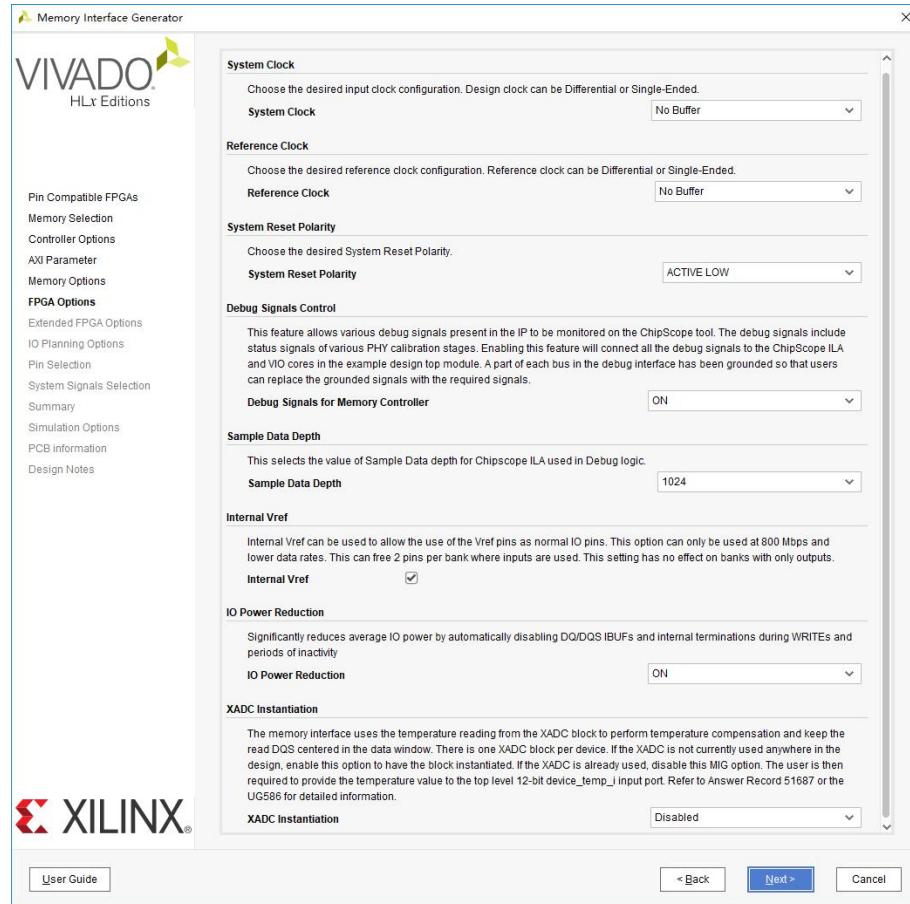
Memory Options  
FPGA Options  
Extended FPGA Options  
IO Planning Options  
Pin Selection  
System Signals Selection  
Summary  
Simulation Options  
PCB information  
Design Notes

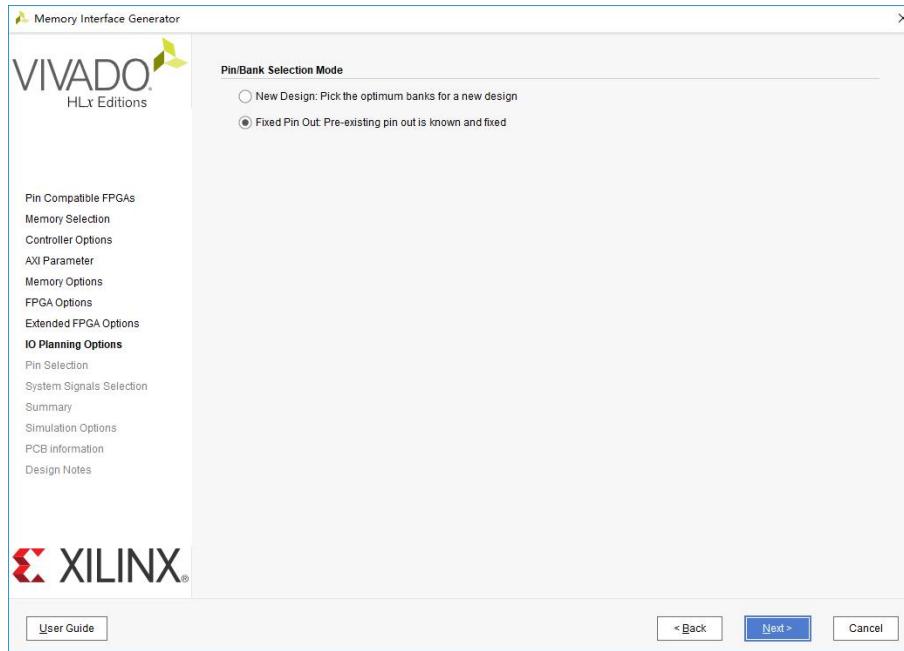
**XILINX**

User Guide      < Back      Next >      Cancel

**Figure 3-4. MIG Configuration**







**Pin Selection For Controller 0 - DDR3 SDRAM**

Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1 ddr3_dq[0]	34	▼ T1	▼ E2	▼
2 ddr3_dq[1]	34	▼ T1	▼ D4	▼
3 ddr3_dq[2]	34	▼ T1	▼ C1	▼
4 ddr3_dq[3]	34	▼ T1	▼ E4	▼
5 ddr3_dq[4]	34	▼ T1	▼ F2	▼
6 ddr3_dq[5]	34	▼ T1	▼ G4	▼
7 ddr3_dq[6]	34	▼ T1	▼ D1	▼
8 ddr3_dq[7]	34	▼ T1	▼ F3	▼
9 ddr3_dq[8]	34	▼ T0	▼ C4	▼
10 ddr3_dq[9]	34	▼ T0	▼ C3	▼
11 ddr3_dq[10]	34	▼ T0	▼ B5	▼
12 ddr3_dq[11]	34	▼ T0	▼ B1	▼
13 ddr3_dq[12]	34	▼ T0	▼ A5	▼
14 ddr3_dq[13]	34	▼ T0	▼ B2	▼
15 ddr3_dq[14]	34	▼ T0	▼ A4	▼
16 ddr3_dq[15]	34	▼ T0	▼ A3	▼
17 ddr3_dm[0]	34	▼ T1	▼ D2	▼
18 ddr3_dm[1]	34	▼ T0	▼ D3	▼
19 ddr3_dqs_p[0]	34	▼ T1	▼ G1	▼
20 ddr3_dqs_n[0]	34	▼ T1	▼ F1	▼
21 ddr3_dqs_p[1]	34	▼ T0	▼ B3	▼
22 ddr3_dqs_n[1]	34	▼ T0	▼ A2	▼
23 ddr3_addr[13]	34	▼ T3	▼ P5	▼
24 ddr3_addr[12]	34	▼ T3	▼ P2	▼
25 ddr3_addr[11]	34	▼ T3	▼ M2	▼
26 ddr3_addr[10]	34	▼ T2	▼ H1	▼
27 ddr3_addr[9]	34	▼ T3	▼ P4	▼
28 ddr3_addr[8]	34	▼ T3	▼ L2	▼
29 ddr3_addr[7]	34	▼ T3	▼ M4	▼
30 ddr3_addr[6]	34	▼ T2	▼ M1	▼
31 ddr3_addr[5]	34	▼ T3	▼ M3	▼
32 ddr3_addr[4]	34	▼ T2	▼ L1	▼

Validation successful. Press Next to proceed.

User Guide | < Back | **Next >** | Cancel

**System Signals Selection**

Select the system pins below appropriately for the interface. Customization of these pins can also be made in the XDC after the design is generated. For more information see [UG586 Bank and Pin rules](#).

System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.

**System Signals**

These signals may be connected internally to other logic or brought out to a pin.

- **sys\_rst**: This input signal is used to reset the interface.
- **init\_calib\_complete**: This signal indicates that the interface has completed calibration and memory initialization and is ready for commands. LOC constraint will be generated in XDC for Example design only based on "Pin Number" selection below.
- **error**: This output signal indicates that the traffic generator in the Example Design has detected a data mismatch. This signal does not exist in the User Design.

Signal Name	Bank Number	Pin Number
sys_rst	Select Bank	No connect
init_calib_complete	Select Bank	No connect
tg_compare_error	Select Bank	No connect

All pins must be constrained to specific locations in order to generate a bit file in the implementation phase (this is not required for simulation).

**Vivado Project Options:**

```

Target Device          : xc7s15-ftgb196
Speed Grade           : -1
HDL                  : verilog
Synthesis Tool        : VIVADO

```

If any of the above options are incorrect, please click on "Cancel", change the CORE Generation Options and try again.

**MIG Output Options:**

```

Module Name            : mig_7series_0
No of Controllers      : 1
Selected Compatible Device(s) : xc7s25-ftgb196, xc7s50-ftgb196, xc7s6-ftgb196

```

**FPGA Options:**

```

System Clock Type     : No Buffer
Reference Clock Type  : No Buffer
Debug Port             : ON
Internal Vref          : enabled
IO Power Reduction     : ON
XADC Instantiation in MIG : Disabled

```

**Extended FPGA Options:**

```

DCI for DQ,DQS#_DM    : enabled
Internal Termination (HR Banks) : 50 Ohms

```

---

```

/*
 * Controller 0
 */
Controller Options :
Memory                 : DDR3_SDRAM
Interface               : NATIVE
Design Clock Frequency : 3000 ps (333.33 MHz)
Phy to Controller Clock Ratio : 2:1
Input Clock Period     : 5999 ps
CLKFBOUT_MULT (PLL)   : 8
DIVCLK_DIVIDE (PLL)   : 1
VCC_AUX IO             : 1.8V
Memory Type            : Components
Memory Part            : MT41K128M16XX-15E
Equivalent Part(s)     : --
Data Width              : 16
ECC                    : Disabled
Data Mask               : enabled
ORDERING               : Normal

```

**Figure 3-5. MIG Configuration**

#### 4. Reference

- [1] ug470\_7Series\_Config.pdf
- [2] ds181\_Artix\_7\_Data\_Sheet.pdf
- [3] ug475\_7Series\_Pkg\_Pinout.pdf
- [4] n25q\_64a\_3v\_65nm.pdf
- [5] MT41J128M16JT-125K.pdf

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## 5. Revision

Doc. Rev.	Date	Comments
0.1	25/06/2020	Initial Version.
1.0	30/06/2019	V1.0 Formal Release.

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