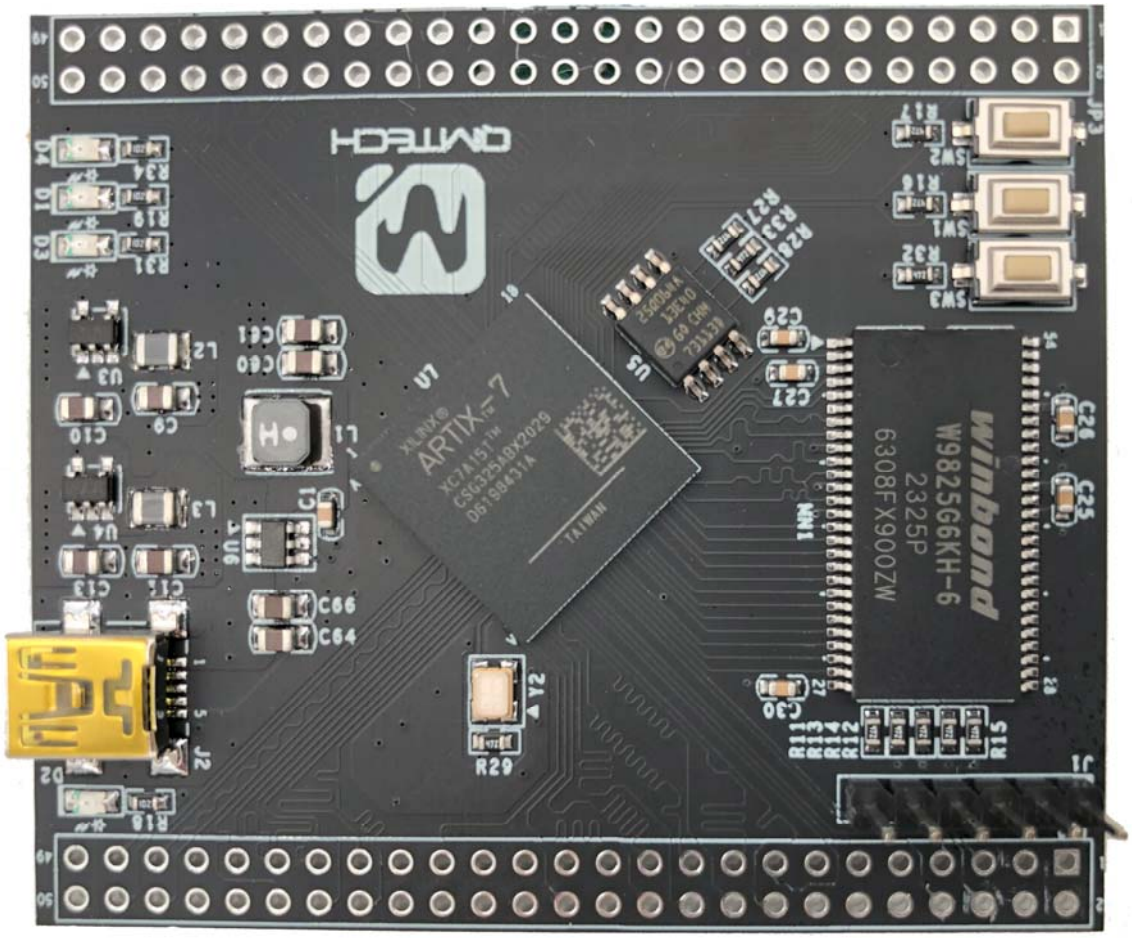
XILINX XC7A15T CORE BOARD

USER MANUAL



Preface

The QMTECH® XC7A15T core board uses Xilinx Artix®-7 devices to demonstrate tM he highest performance-per-watt fabric, transceiver line rates, DSP processing, and AMS integration in a cost-optimized FPGA. Featuring the MicroBlaze™ soft processor and 1,066Mb/s DDR3 support, the family is the best value for a variety of cost and power-sensitive applications including software-defined radio, machine vision cameras, and low-end wireless backhaul.

Table of Contents

1. Introduction

1.1 Document Scope

This demo user manual introduces the QMTECH XC7A15T core board and describes how to setup the development board running with application software Xilinx Vivado 2018.2. Users may employee the on board rich logic resource FPGA XC7A15T to implement various applications. The core board has 88 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the QMTECH XC7A15T core board:

- On-Board FPGA: XC7A15T-1CSG325C;
- On-Board FPGA external crystal frequency: 50MHz;
- XC7A15T-1CSG325C has rich block RAM resource up to 900Kb;
- XC7A15T-1CSG325C has 16,640 logic cells;
- On-Board Micron N25Q064A SPI Flash, 8M bytes for user configuration code;
- On-Board 3.3V power supply for FPGA by using TPS563201 wide input range DC/DC;
- QMTECH XC7A15T core board has two 50p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- QMTECH XC7A15T core board has 3 user switches;
- QMTECH XC7A15T core board has 4 user LEDs;
- QMTECH XC7A15T core board has JTAG interface, by using 6p, 2.54mm pitch header;
- QMTECH XC7A15T core board PCB size is: 66.2mm x 57.0mm;
- Default power source for board is from Mini USB: 1A@5V DC;

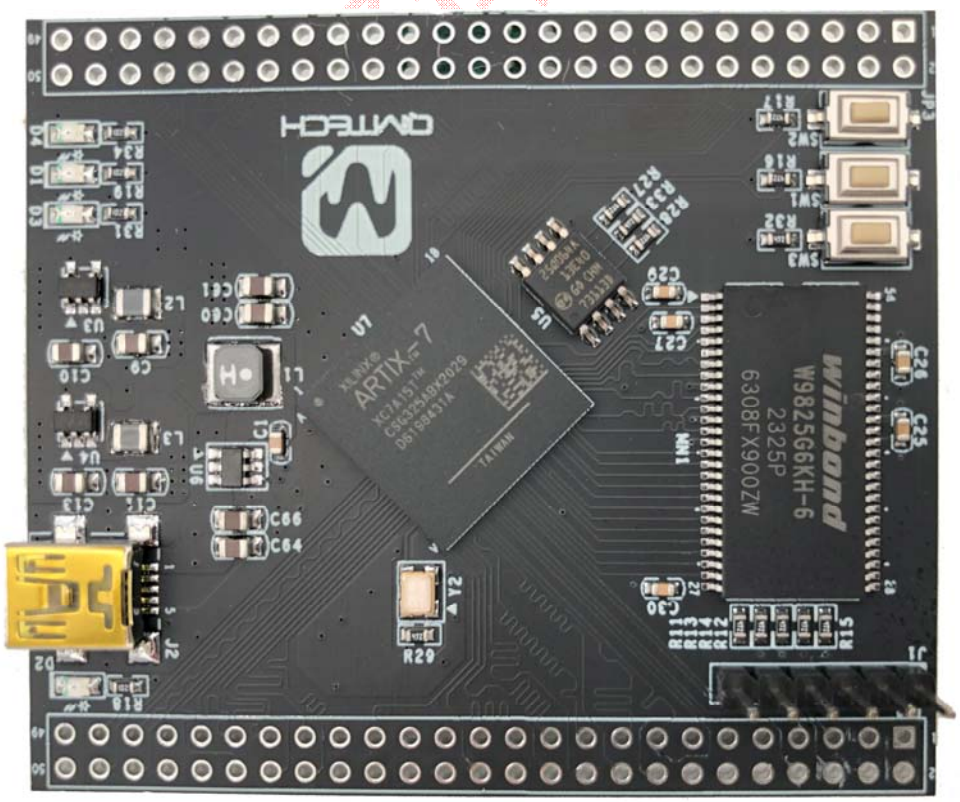


Figure 1-1. QMTECH XC7A15T Core Board Overview

2. Getting Started

Below image shows the dimension of the QMTECH XC7A15T core board: 66.2mm x 57.0mm. The unit in below image is millimeter(mm).

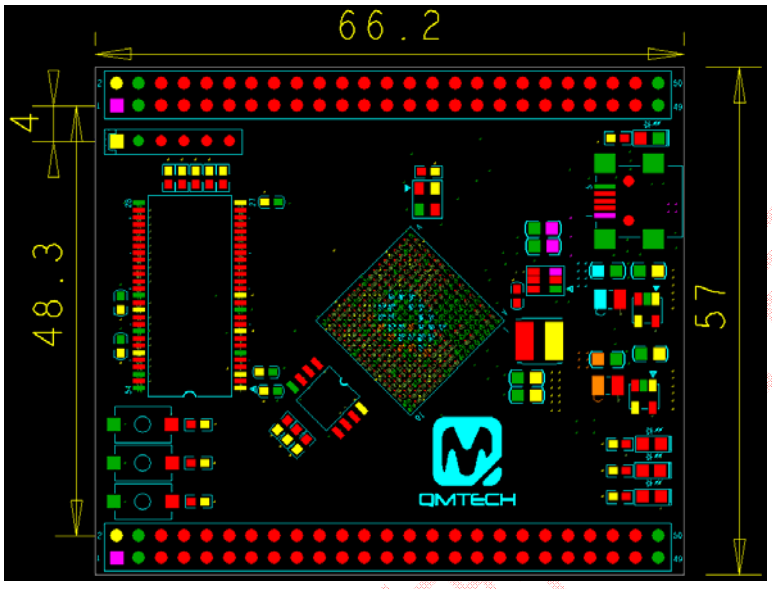


Figure 2-1. QMTECH XC7A15T Core Board Dimension

2.1 Install Development Tools

To develop FPGA applications, users need to prepare Xilinx Vivado 2018.2 or newer versions, Xilinx USB platform cable, Mini USB cable for power supply. Below image shows the Xilinx Vivado 2018.2 development environment which could be downloaded from Xilinx office website:

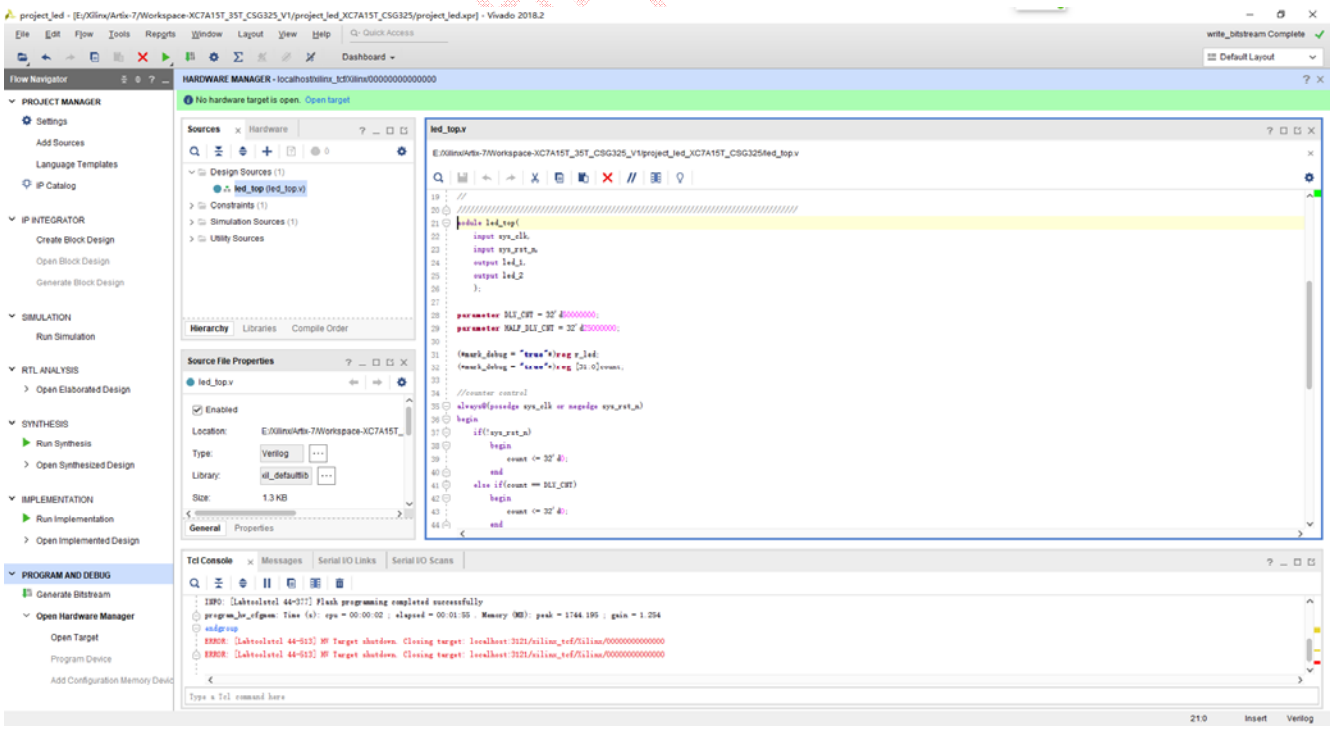


Figure 2-2. Vivado 2018.2

Below image shows the JTAG connection between Xilinx USB platform cable and QMTECH XC7A15T core board:

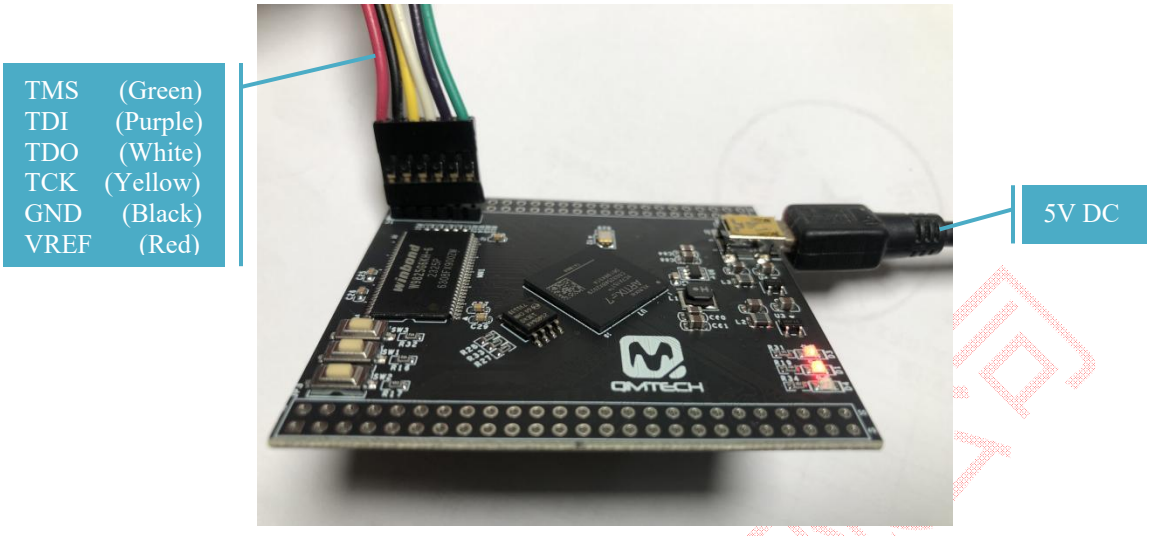


Figure 2-3. JTAG Connection and Power Supply

Once the FPGA test program is correctly 【Synthesized】, 【Implemented】 and 【Generated with Bitstream】, users may click the 【Open Target】 option to connect the XC7A15T FPGA.

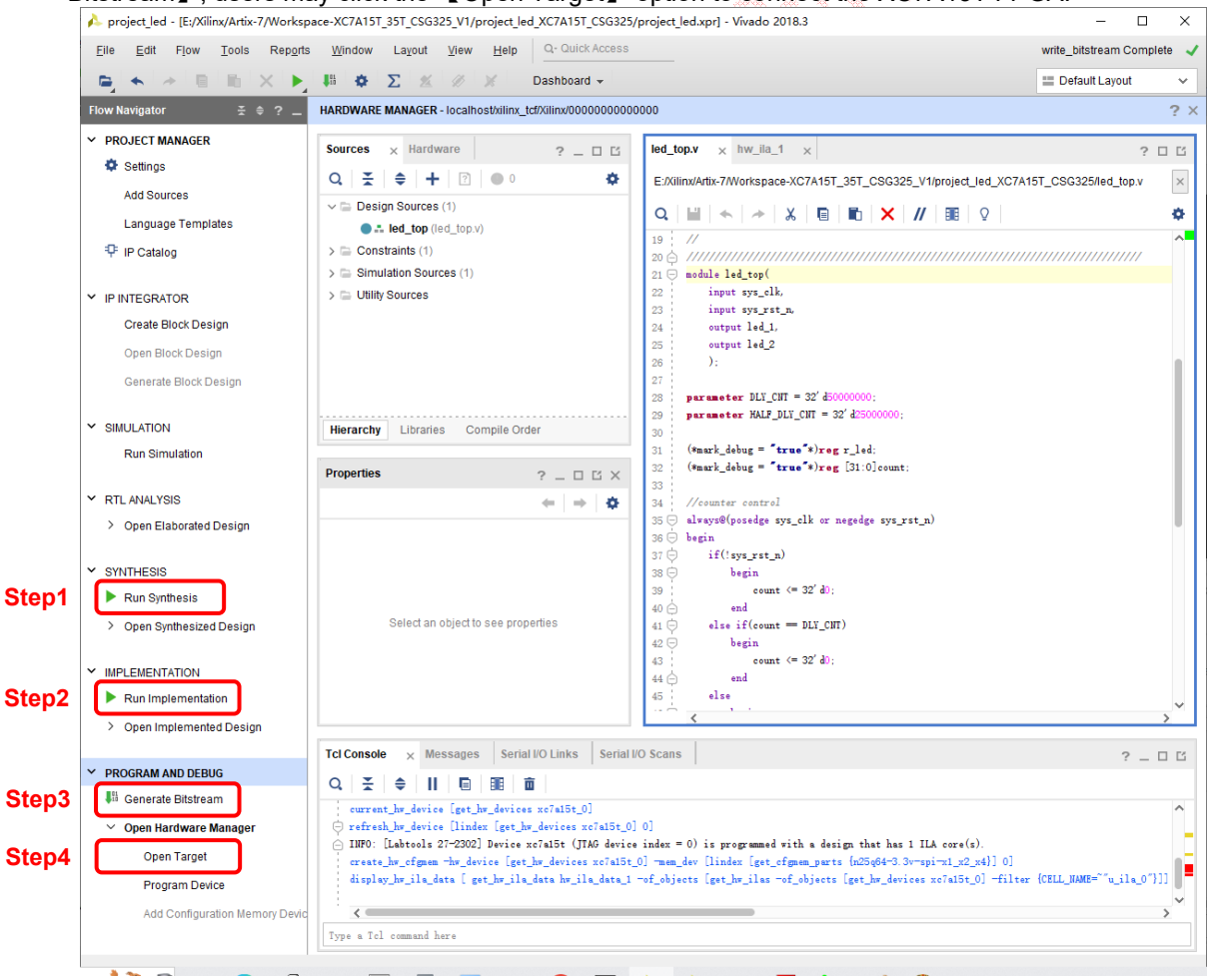


Figure 2-4. Vivado to Connect FPGA

Chip info like xc7a15t_0 is shown in Hardware Manager as below image. Users then could right click the device to choose 【Program Device】to load the Bitstream *.bit into FPGA or to choose【Add Configuration Memory Device】to program the *.mcs file into on-board SPI flash.

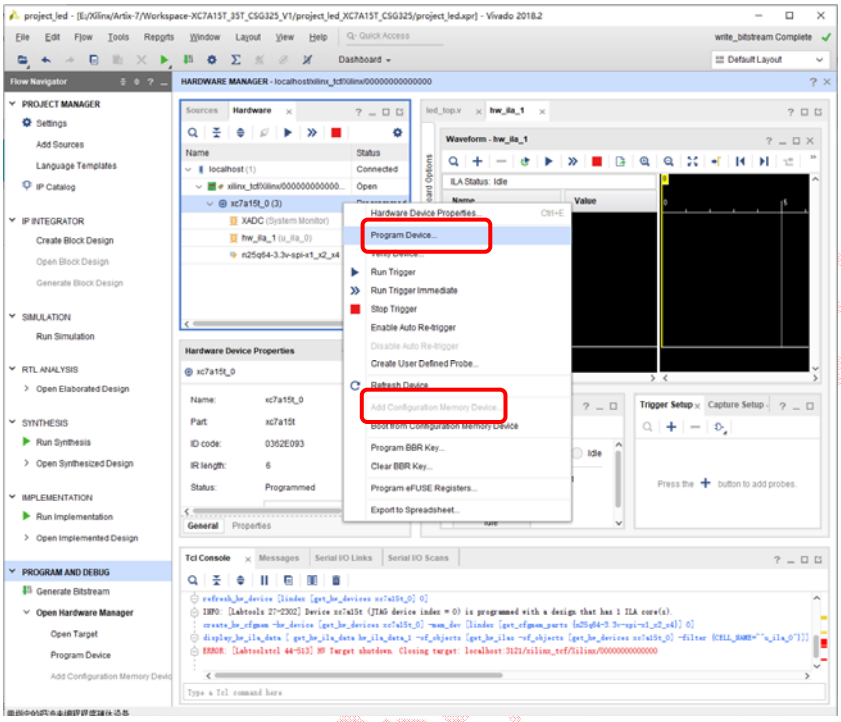


Figure 2-5. Program FPGA

Users could convert the *.bit file into the *.mcs file by using the Vivado tool. Choose the 【Tools】on the menu bar and then select 【Generate Memory Configuration File】, and then configure the parameters shown in below image:

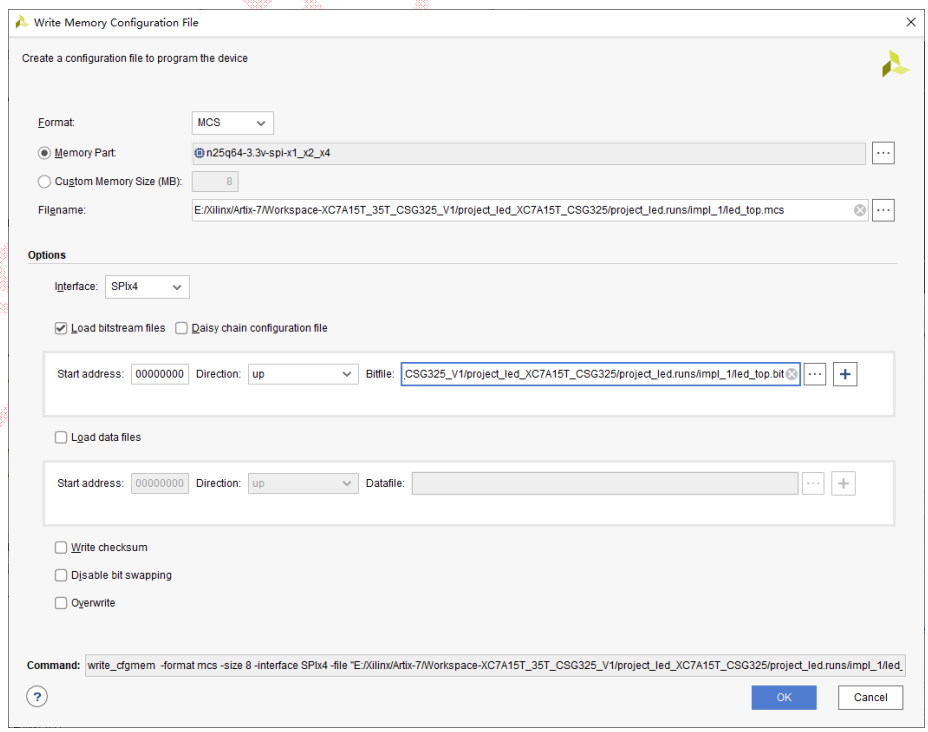


Figure 2-6. Generate *.mcs File

2.2 XC7A15T Core Board Hardware Design

2.2.1 Power Supply

The core board needs 5V DC input as power supply which could be directly injected from JP2/JP3 header or the Mini USB connector. Users may refer to the hardware schematic for the detailed design. The on board LED D2 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V. Detailed design refer to hardware schematic.

Note: FPGA core supply 1.0V is regulated by On-Semi DC/DC chip NCP1529 which could output maximum 1A current.

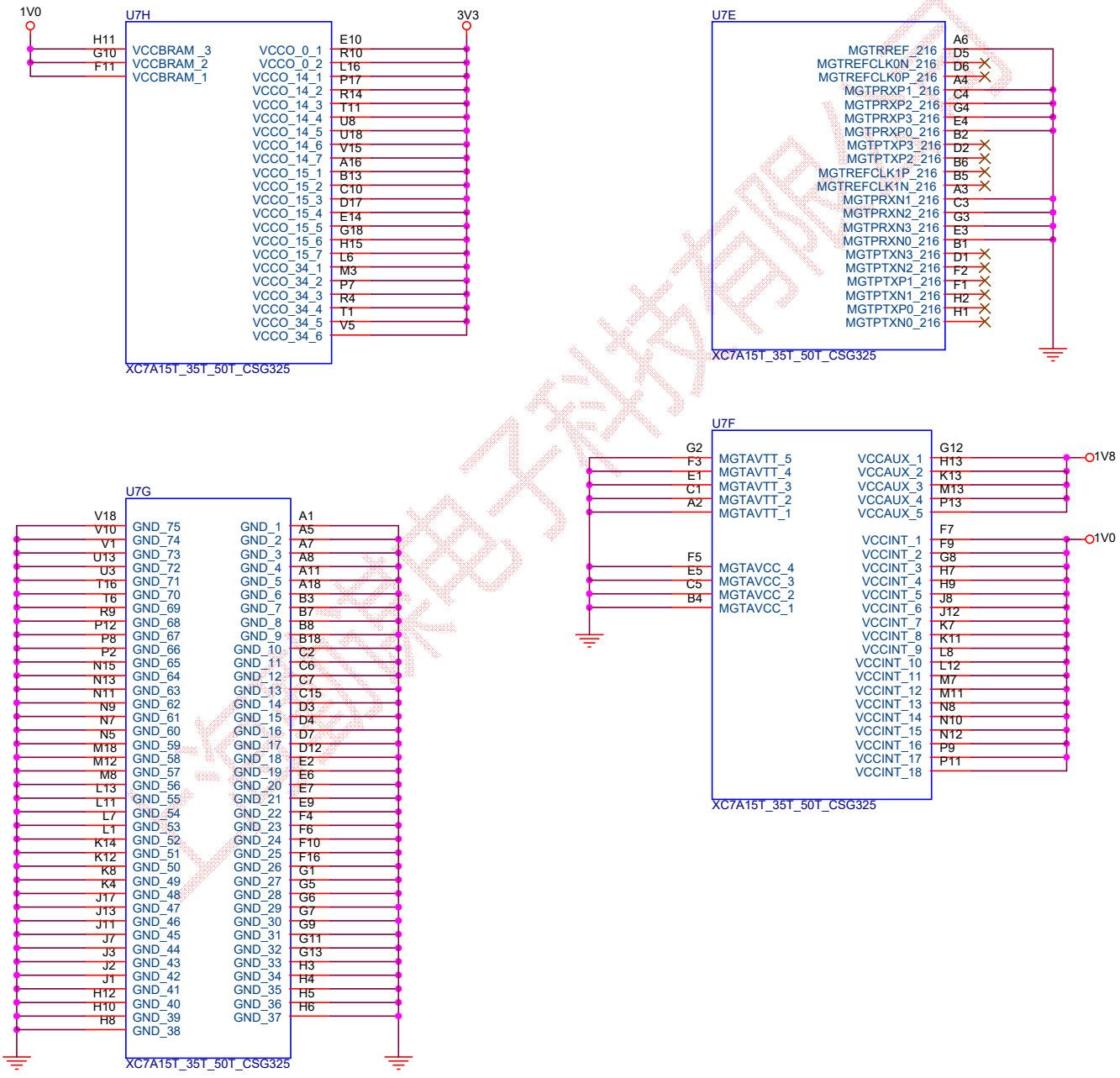


Figure 2-7. Power Supply for the FPGA

2.2.1 XC7A15T Power Supply

The core board's 3.3V power supply is using high efficiency DC/DC chip TPS563201 provided by TI Inc. The TPS563201 supports wide voltage input range from 4.5V to 17V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the TPS563201 hardware design:

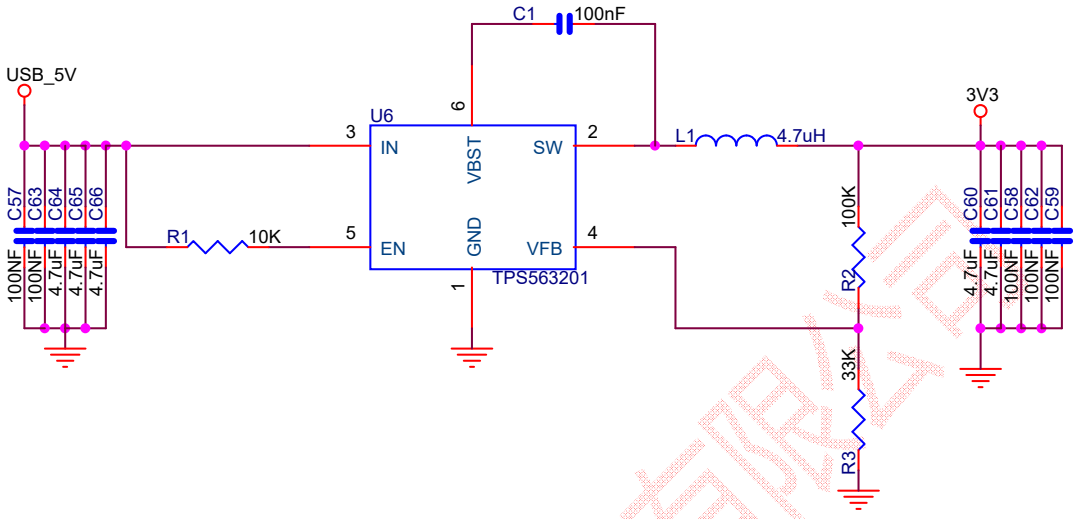


Figure 2-8. TPS563201 Hardware Design

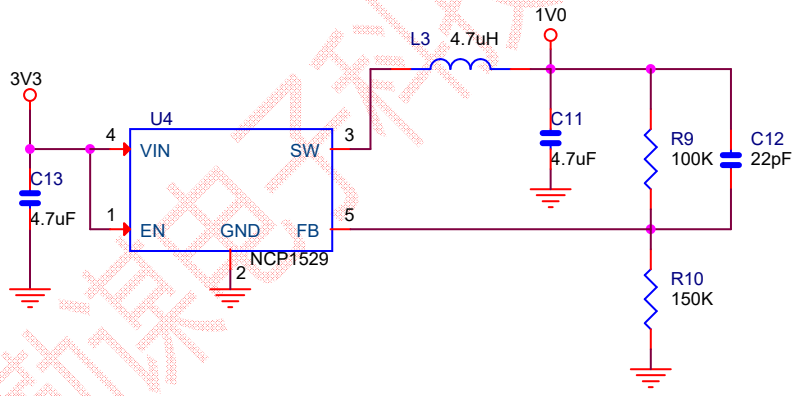


Figure 2-9. 1.0V Core Voltage DC/DC

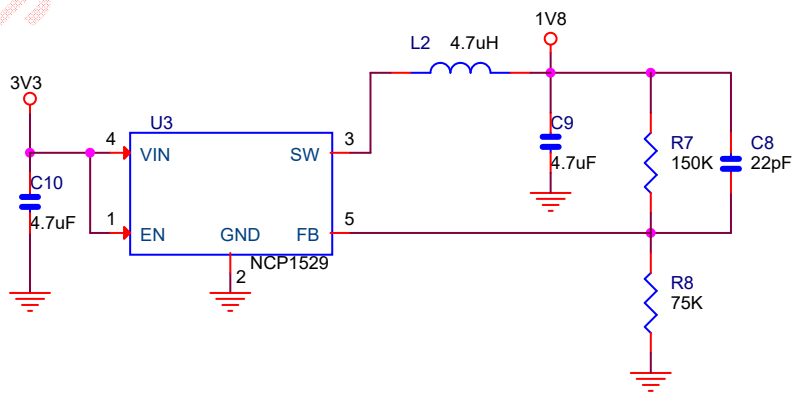


Figure 2-10. 1.8V AUX Voltage DC/DC

2.2.2 XC7A15T SPI Boot

In default, XC7A15T boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using N25QL064A manufactured by Micron, with 64Mbit memory storage.

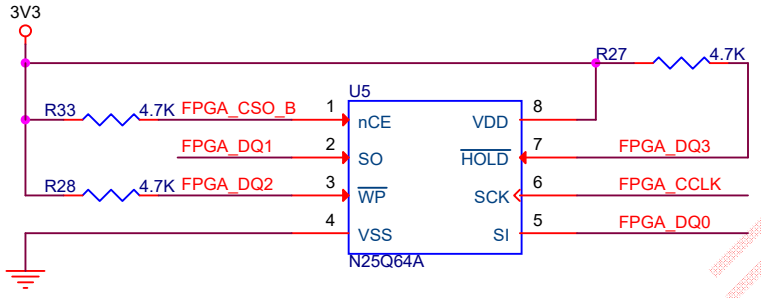


Figure 2-11. SPI Flash

The FPGA boot sequence setting M0:M1:M2 is configured as 1:0:0 which indicates FPGA will boot from SPI Flash after power on.

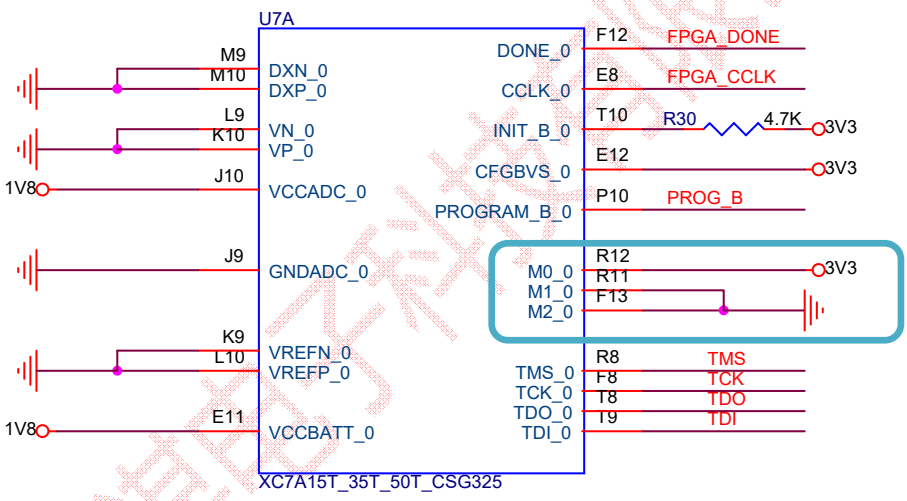


Figure 2-12. M0:M1 Hardware Settings

The LED D3 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D3 could be used as FPGA loading status indicator.

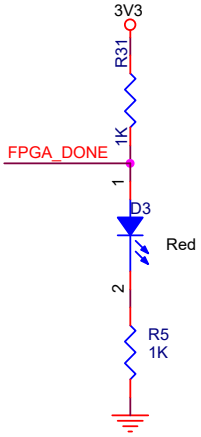


Figure 2-13. FPGA_DONE Status Indicator

2.2.3 XC7A15T System Clock

FPGA chip XC7A15T has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

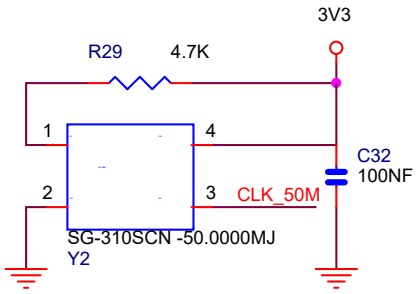


Figure 2-14. 50MHz System Clock

2.2.4 XC7A15T JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

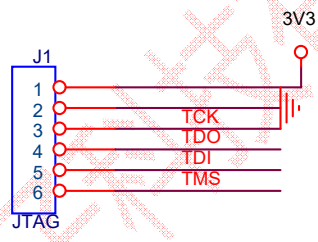


Figure 2-15. JTAG Port

2.2.5 XC7A15T User LEDs

Below image shows two user LEDs and one LED for 3.3V power supply indicator:

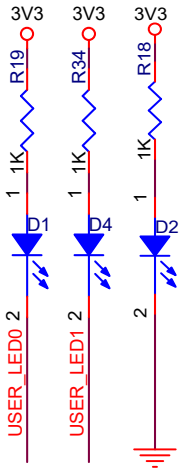


Figure 2-16. LEDs

2.2.6 XC7A15T Extension IOs

The core board has two 50P 2.54mm pitch headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

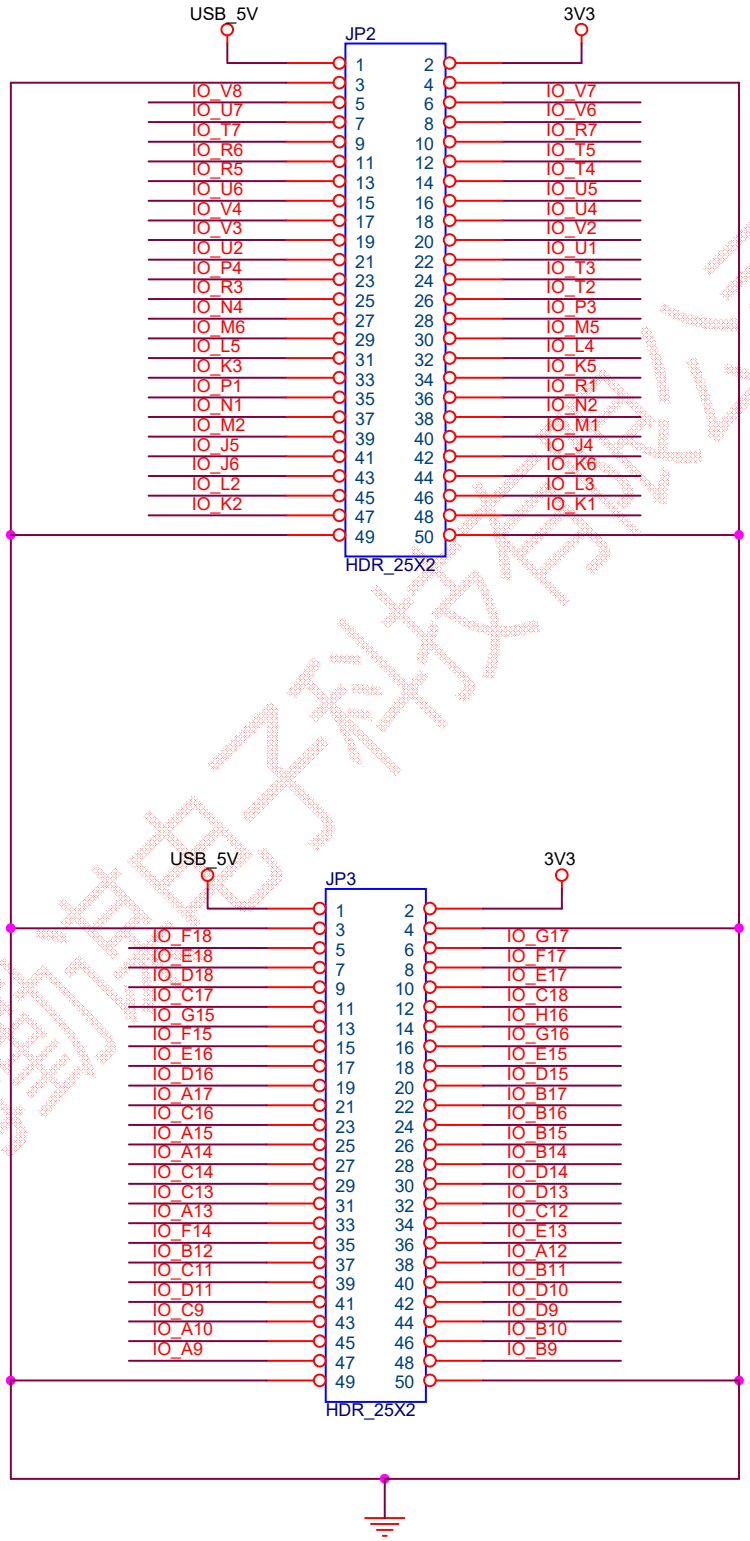


Figure 2-17. Extension IOs

2.2.7 XC7A15T User Keys

Below image shows the PROGRAM_B key and two user keys:

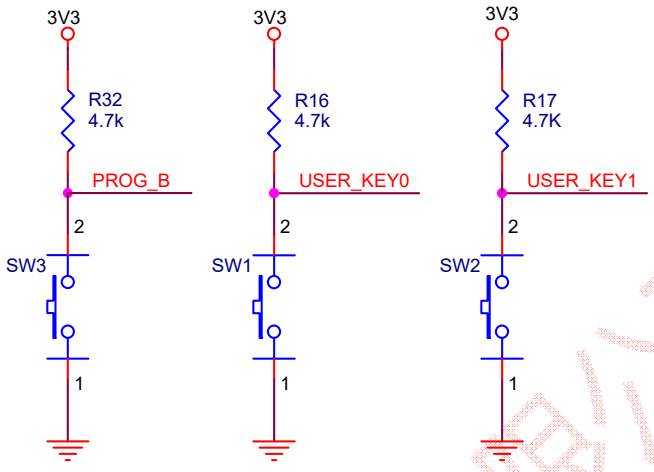


Figure 2-18. Keys

2.2.8 SDRAM Memory

The core board has on board 16bit width data bus, 32MB memory size W9825G6KH-6 SDRAM provided by Winbond. Below image shows the detailed hardware design:

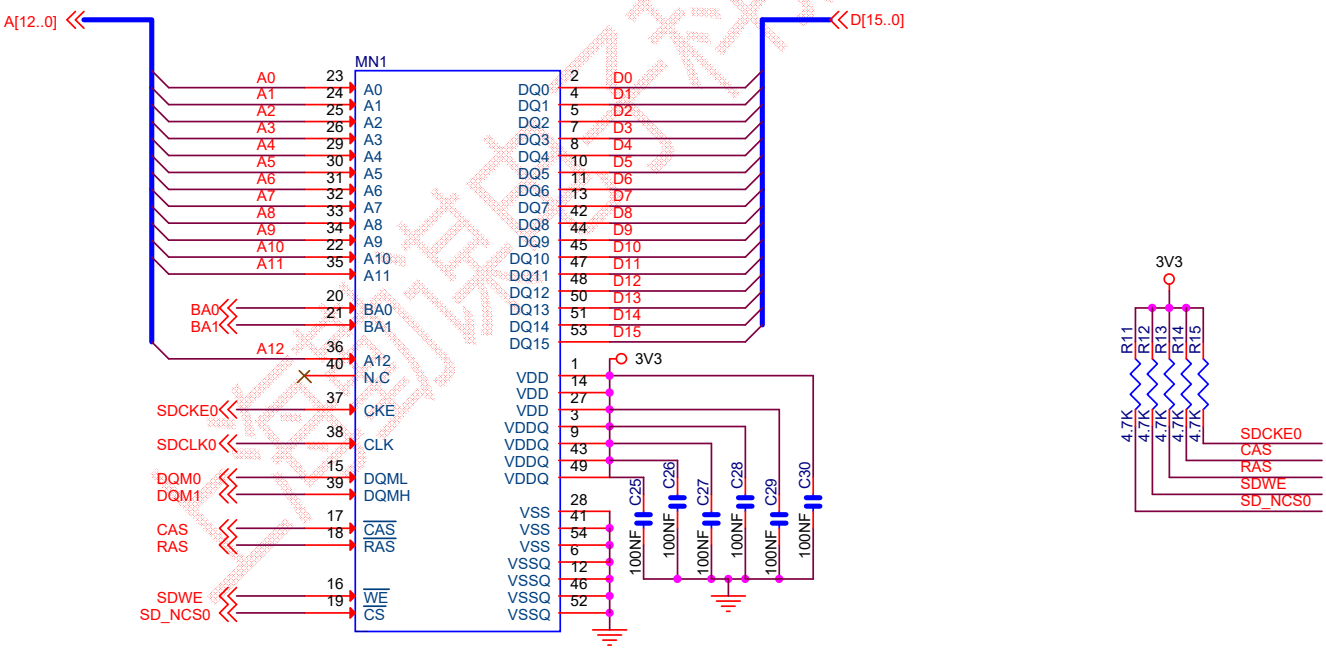


Figure 2-19. SDRAM Memory

3. Reference

[1] ug470_7Series_Config.pdf
[2] ds181_Artix_7_Data_Sheet.pdf
[3] ug475_7Series_Pkg_Pinout.pdf
[4] N25QL064A.pdf
[5] TPS563201.df
[6] NCP1529-D.PDF

4. Revision

Doc. Rev.	Date	Comments
0.1	09/08/2023	Initial Version.
1.0	19/08/2023	V1.0 Formal Release.