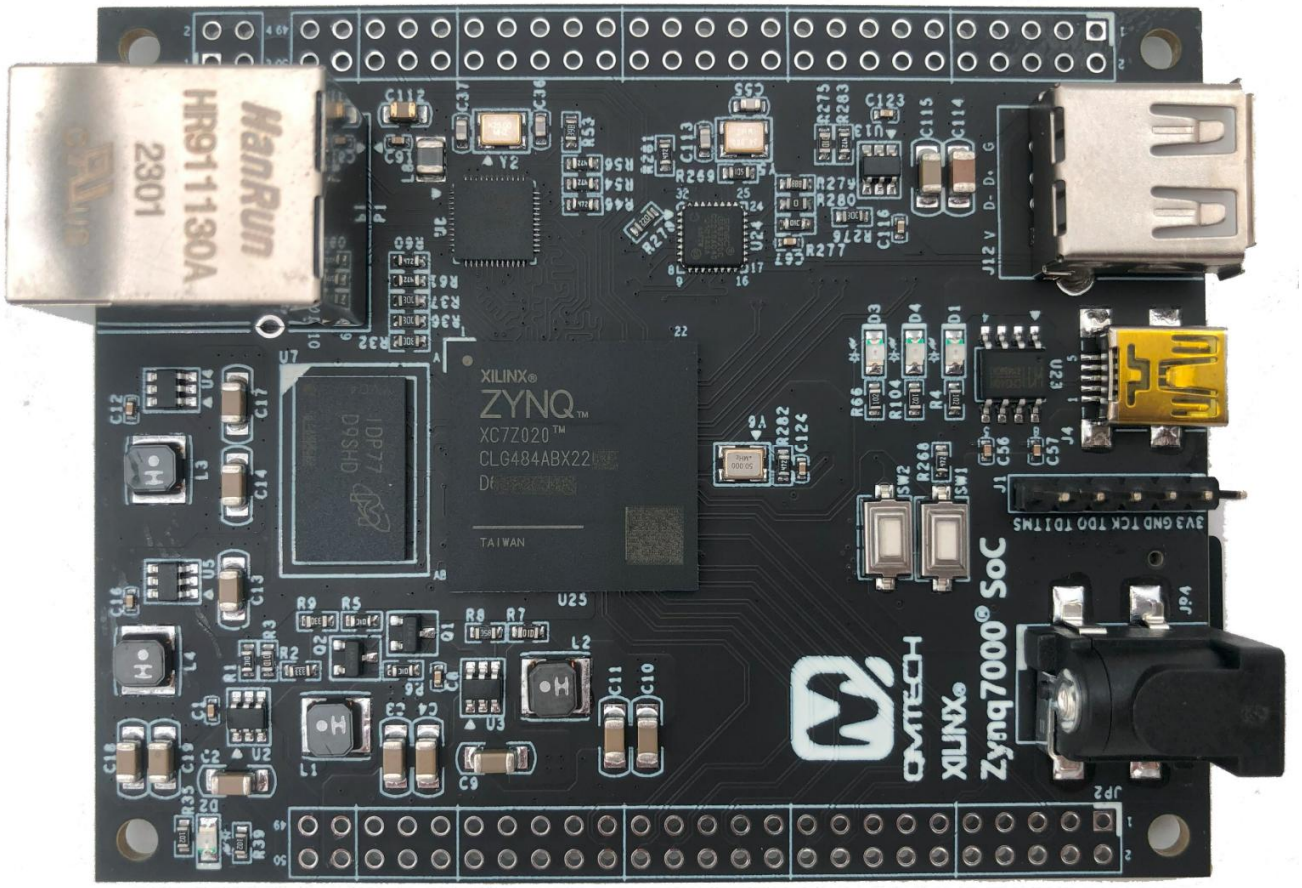
QMTECH ZYNQ XC7Z020 STARTER KIT

USER MANUAL



Preface

The QMTECH® ZYNQ XC7Z020 Starter Kit uses Xilinx Zynq®-7000 device which integrates the software programmability of an ARM®-based processor with the hardware programmability of an FPGA, enabling key analytics and hardware acceleration while integrating CPU, DSP, ASSP, and mixed signal functionality on a single device. Consisting of single-core Zynq-7000S and dual-core Zynq-7000 devices, the Zynq-7000 family is the best price to performance-per-watt, fully scalable SoC platform for your unique application requirements.

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1. Introduction

1.1 Document Scope

This demo user manual introduces the QMTECH ZYNQ XC7Z020 Starter Kit hardware design and describes how to setup the Start Kit running with environment Xilinx Vivado 2018.3. Users may employee the PL side's rich logic resource up to 85K Logic Cells to implement various applications. The Starter Kit also has 84 non-multiplexed PL IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the Starter Kit:

- On-Board SoC: XC7Z020-1CLG484C;
- On-Board PS side external crystal frequency: 33.333MHz;
- On-Board PL side external crystal frequency: 50.000MHz;
- XC7Z020-1CLG484C has rich block RAM resource up to 4.9Mb;
- XC7Z020-1CLG484C has 85K logic cells;
- On-Board 512MB Micron DDR3, MT41K256M16TW-107:P;
- On-Board micro SD slot;
- On-Board USB 2.0 host port connected to PS side by using Microchip ULPI PHY USB3320C.
- On-Board power supply for FPGA by using TI TPS563201 wide input range DC/DC;
- Two on-Board 50p, 2.54mm pitch headers for extending user IOs.
- On-Board RGMII ethernet interface connected to PS side by using RTL8211E-VL-CG;
- Two on-board user switchs, one connected to PS logical reset and the other connected to PL;
- Two on-board user LEDs, one connected to PS and the other connected to PL;
- On-Board JTAG interface, by using 6p, 2.54mm pitch header;
- PCB size is: 67.6mm x 85.9mm;

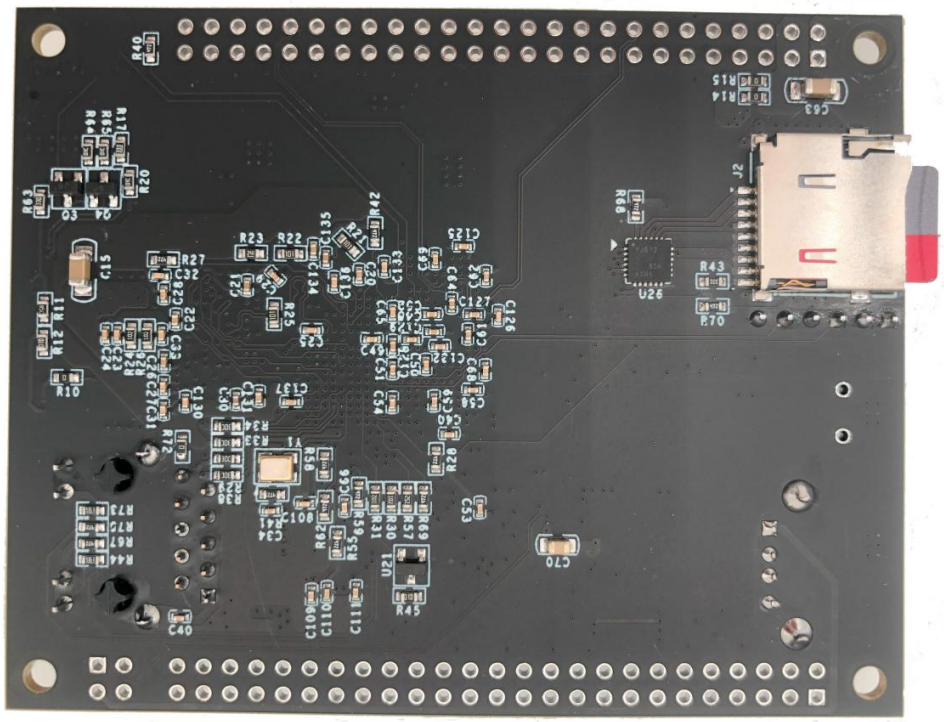

Figure 1-1. QMTECH ZYNQ XC7Z020 Starter Kit Bottom View

2. Getting Started

Below image shows the dimension of the QMTECH ZYNQ XC7Z020 Starter Kit: 67.6mm x 85.9mm. The unit in below image is millimeter(mm).

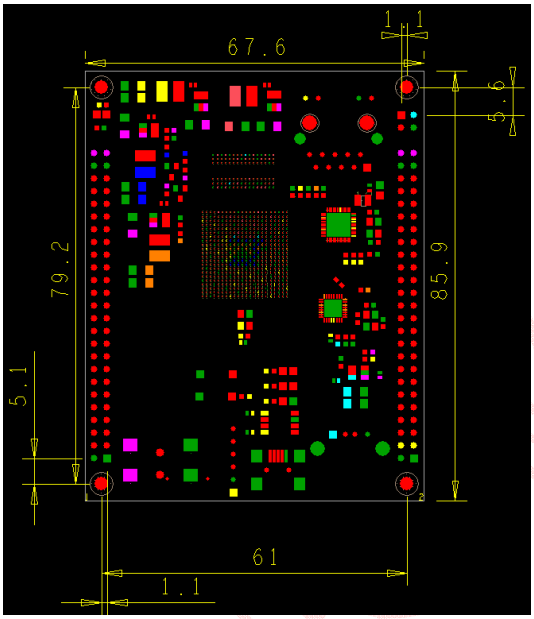

Figure 2-1. QMTECH ZYNQ XC7Z020 Starter Kit Dimension

2.1 Install Development Tools

To develop QMTECH XC7Z020 SoC, users need to prepare Xilinx Vivado 2018.3 or newer versions, Xilinx USB platform, VMware virtual machine installed with Ubuntu 18.04 or newer versions, ZYNQ Starter Kit and mini USB cable. Below image shows the Xilinx Vivado 2018.3 development environment which could be downloaded from Xilinx office website:

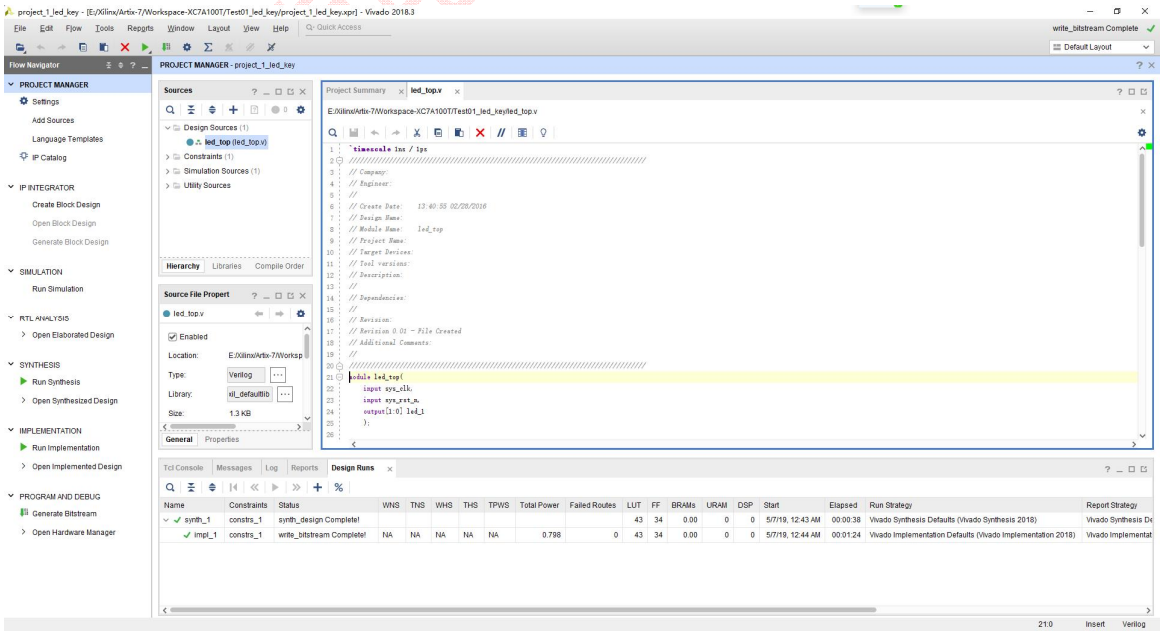

Figure 2-2. Vivado 2018.3

Below image shows the JTAG connection between Xilinx USB platform cable and ZYNQ Starter Kit:

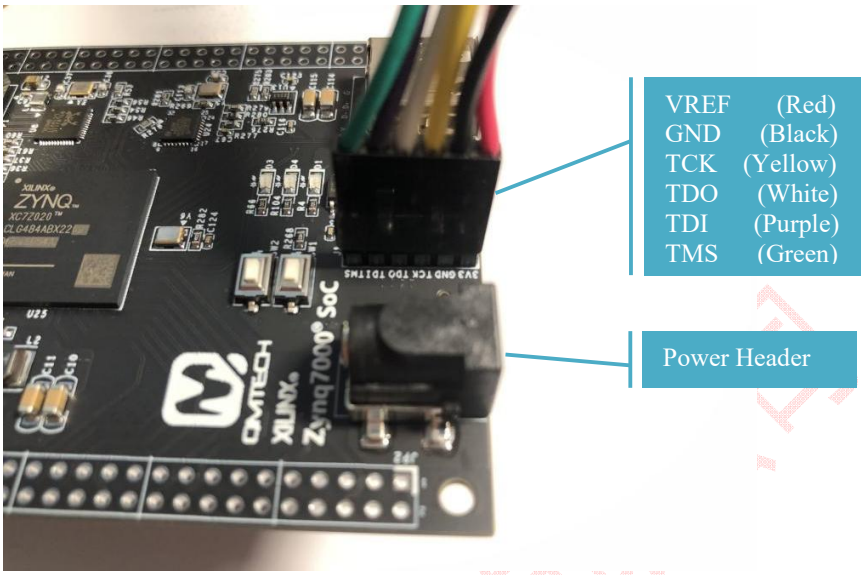

Figure 2-3. JTAG Connection and Power Supply

Below image shows the Ubuntu 18.04 OS:

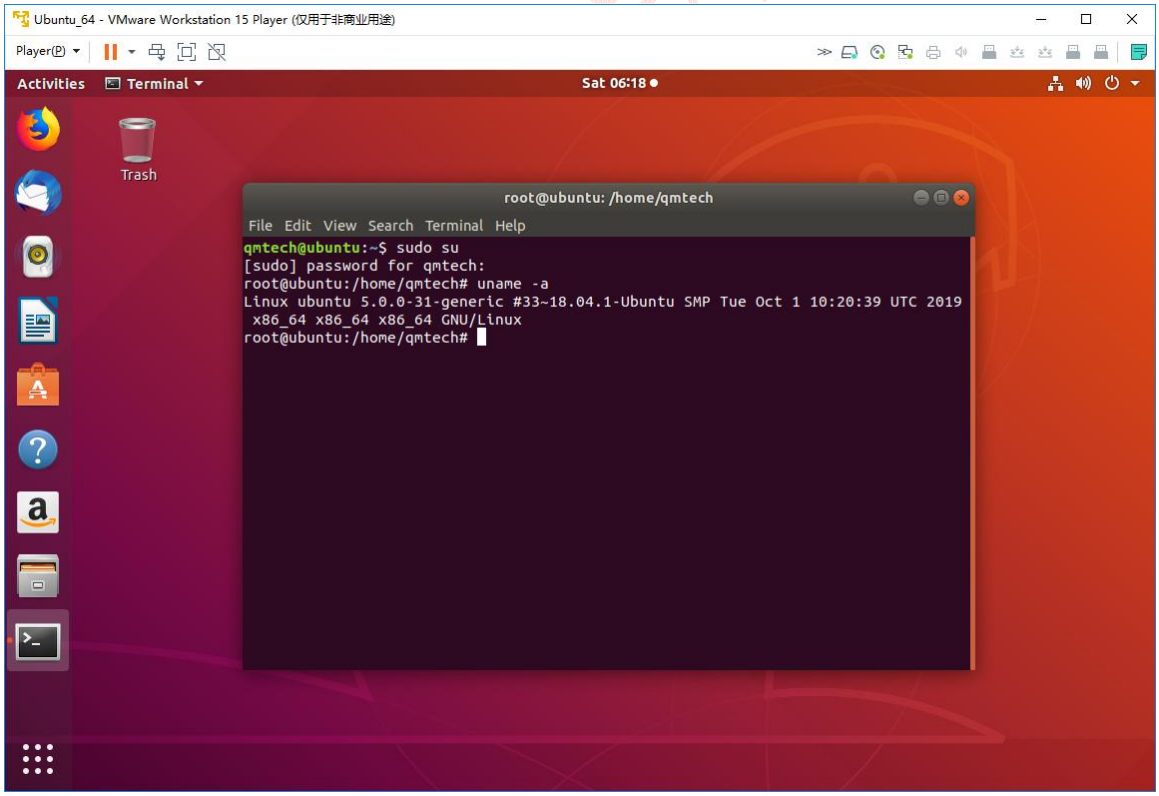

Figure 2-4. Ubuntu 18.04

2.2 QMTECH ZYNQ XC7Z020 Starter Kit Hardware Design

2.2.1 Zynq7000 SoC Power Supply

The Starter Kit needs 5V DC input as power supply which could be directly injected from power header JP4 or the 50P headers JP2 or JP5. Users may refer to the hardware schematic for the detailed design. The on-board LED D1 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the PL banks' IO power level is 3.3V because bank power supply is 3.3V. However, BANK33 IOs' power level could be changed according to detailed custom requirement. There are two 0 ohm resisters could be removed: R14/R15, and instead the BANK33's power supply could be injected from 50P female header JP2. Detailed design refers to hardware schematic.

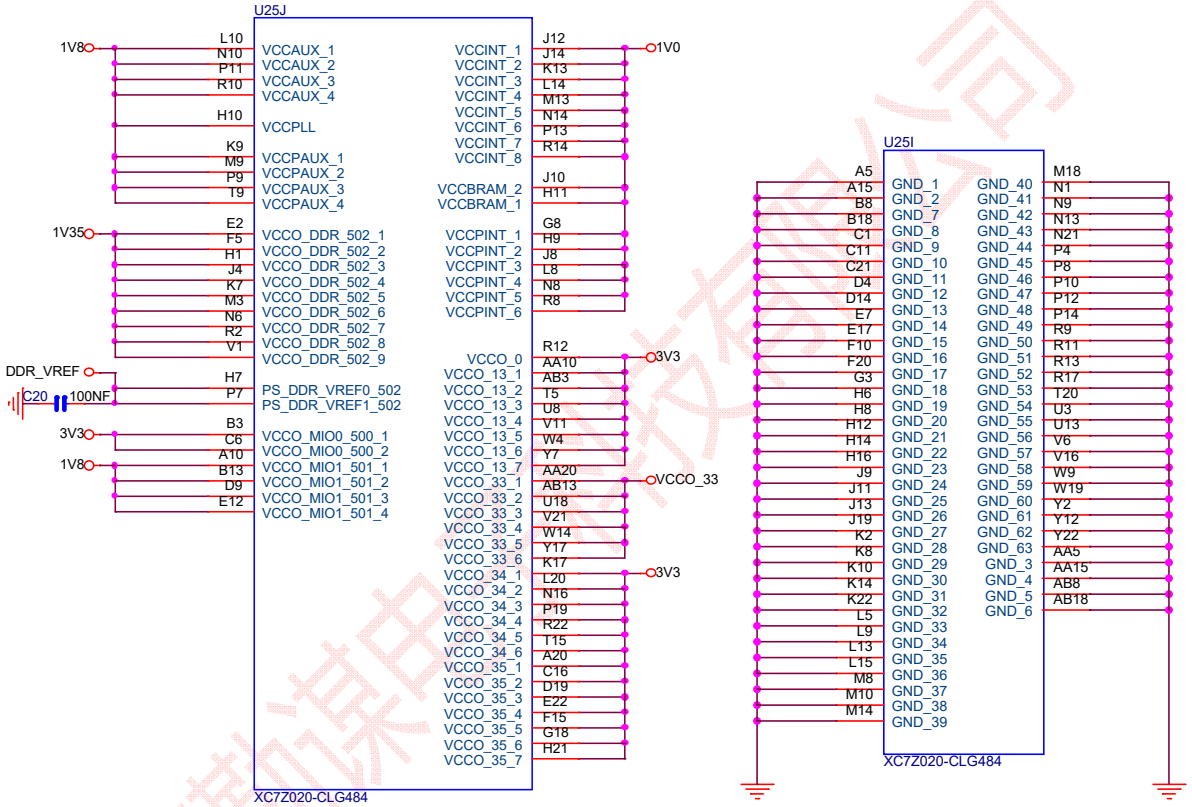

Figure 2-5. Power Supply for the FPGA

2.2.2 Zynq7000 SoC Power Supply Sequencing

The XC7Z020's power supply are all using high efficiency DC/DC chip TPS563201 provided by TI. The TPS563201 supports wide voltage input range from 4.5V to 17V. In normal use case, 5V DC power supply is suggested to be applied on the board. The power on sequence for the Zynq7000 SoC is 1.0V → 1.8 → 1.35V → 3.3V. Below image shows the TPS563201 hardware design for these power supplies.

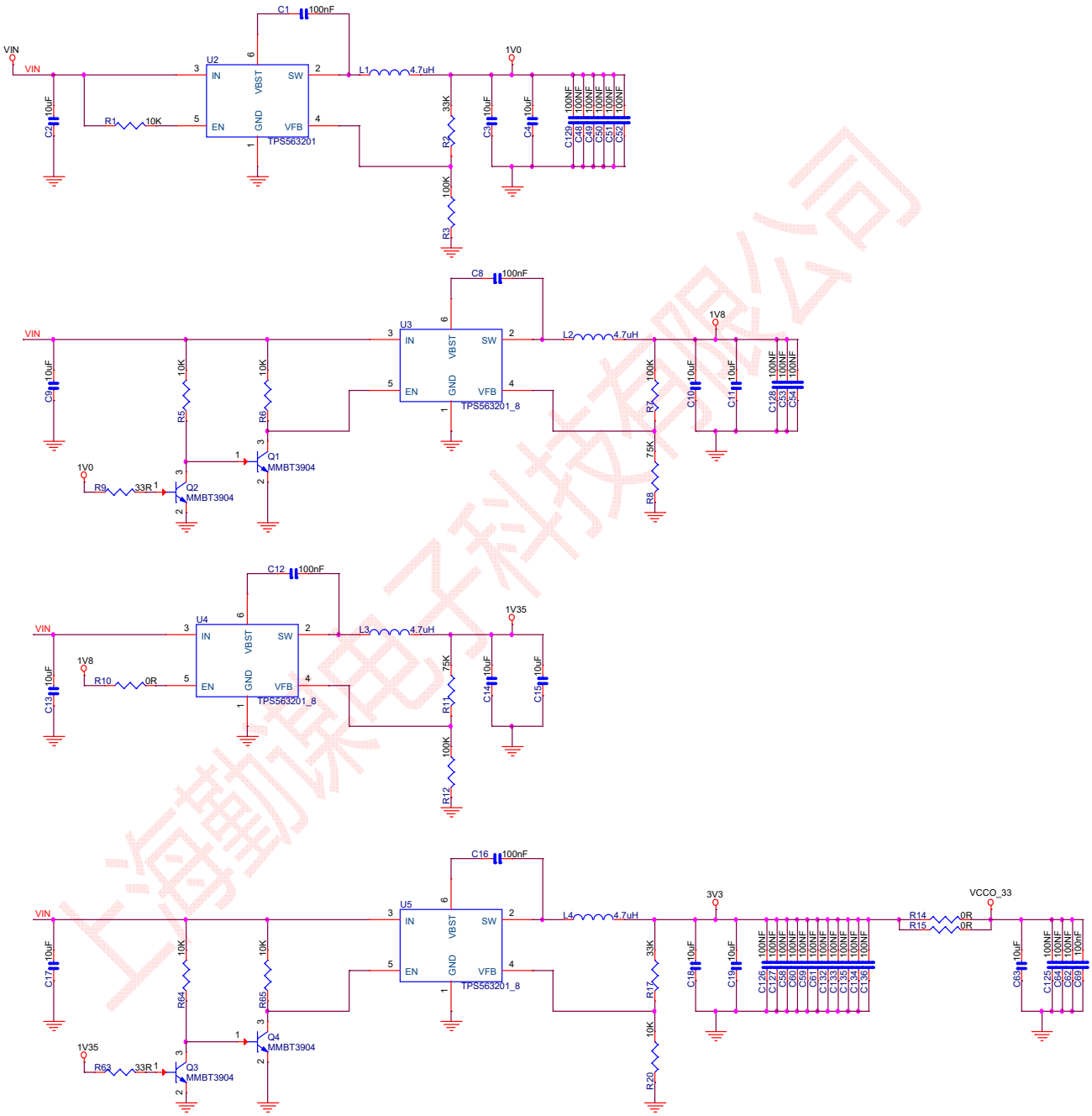

Figure 2-6. Power Supply Sequencing Design

2.2.3 Boot Mode

In default, the PS side ARM core boots from external SD card through SDIO 0 interface, detailed hardware design is shown in below figure.

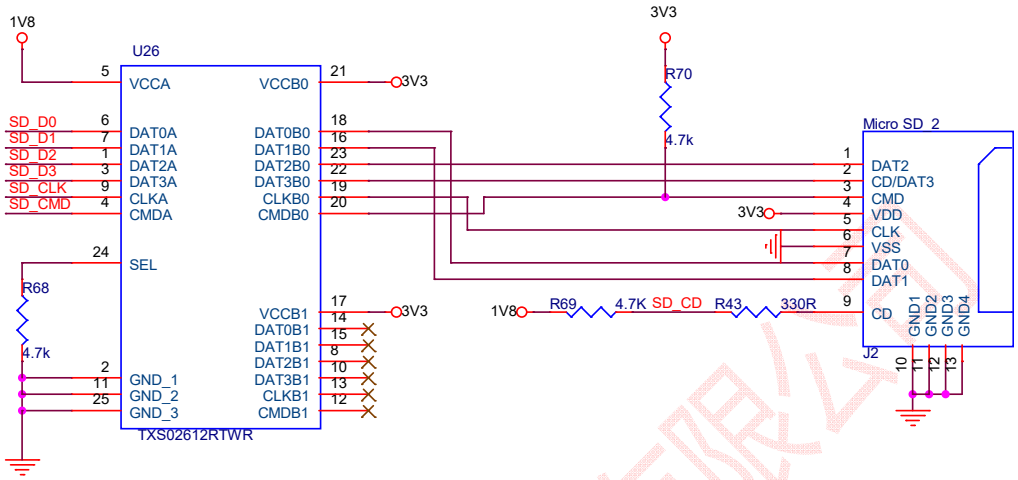

Figure 2-7. Micro SD Card Slot

The boot sequence setting MIO[2:8] is configured as below image.

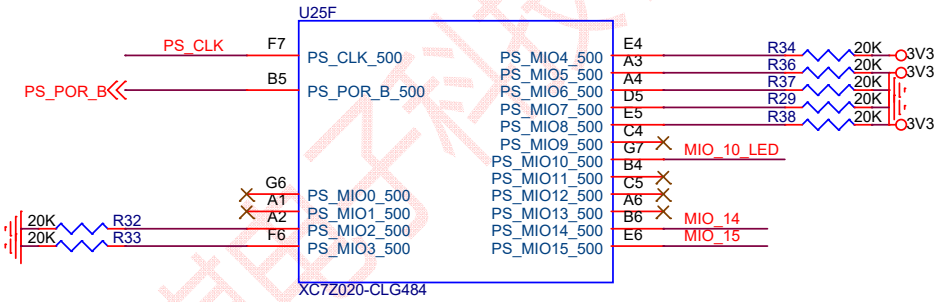

Figure 2-8. MIO[2:8] Hardware Settings

Below image copied from ug585-Zynq-7000-TRM.pdf shows the detailed hardware settings for the boot mode:

Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common(1)				0	0	0	JTAG Chain Routing(2) 0: Cascade mode 1: Independent mode
NOR Boot(3)				0	0	1	
NAND				0	1	0	
Quad-SPI(3)				1	0	0	
SD Card				1	1	0	
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage(4)							
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.				
2.5 V, 3.3 V	0	0					
1.8 V	1	1					

Figure 2-9. MIO[2:8] Hardware Settings

2.2.4 System Clock

The PS side has system clock frequency 33.333MHz which is directly provided by external crystal. And the PL side also has its own system clock with frequency 50.000MHz. Below image shows the detailed hardware design:

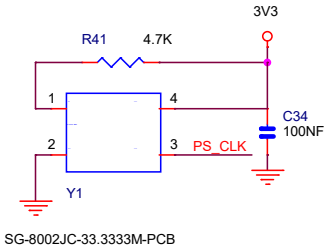

Figure 2-10. 33.333MHz PS Clock

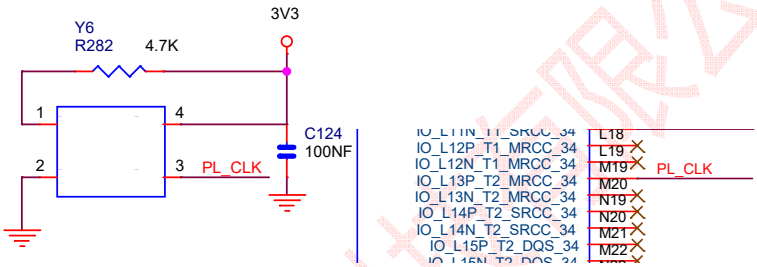

Figure 2-11. 50.000MHz PL Clock

2.2.5 User Keys

Below image shows the PS_RST reset key:

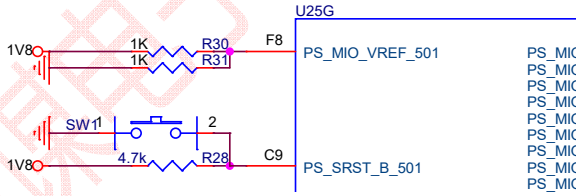

Figure 2-12. PS_SRST Key

Below image shows the PL user key:

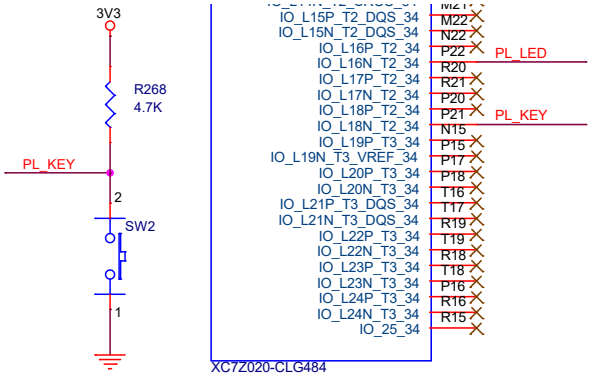

Figure 2-13. PL User Key Connected to PL PIN P21

2.2.6 User Extension IOs

The Starter Kit has two 50P 2.54mm pitch headers which could be used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc. All these IOs are extended from PL IOs.

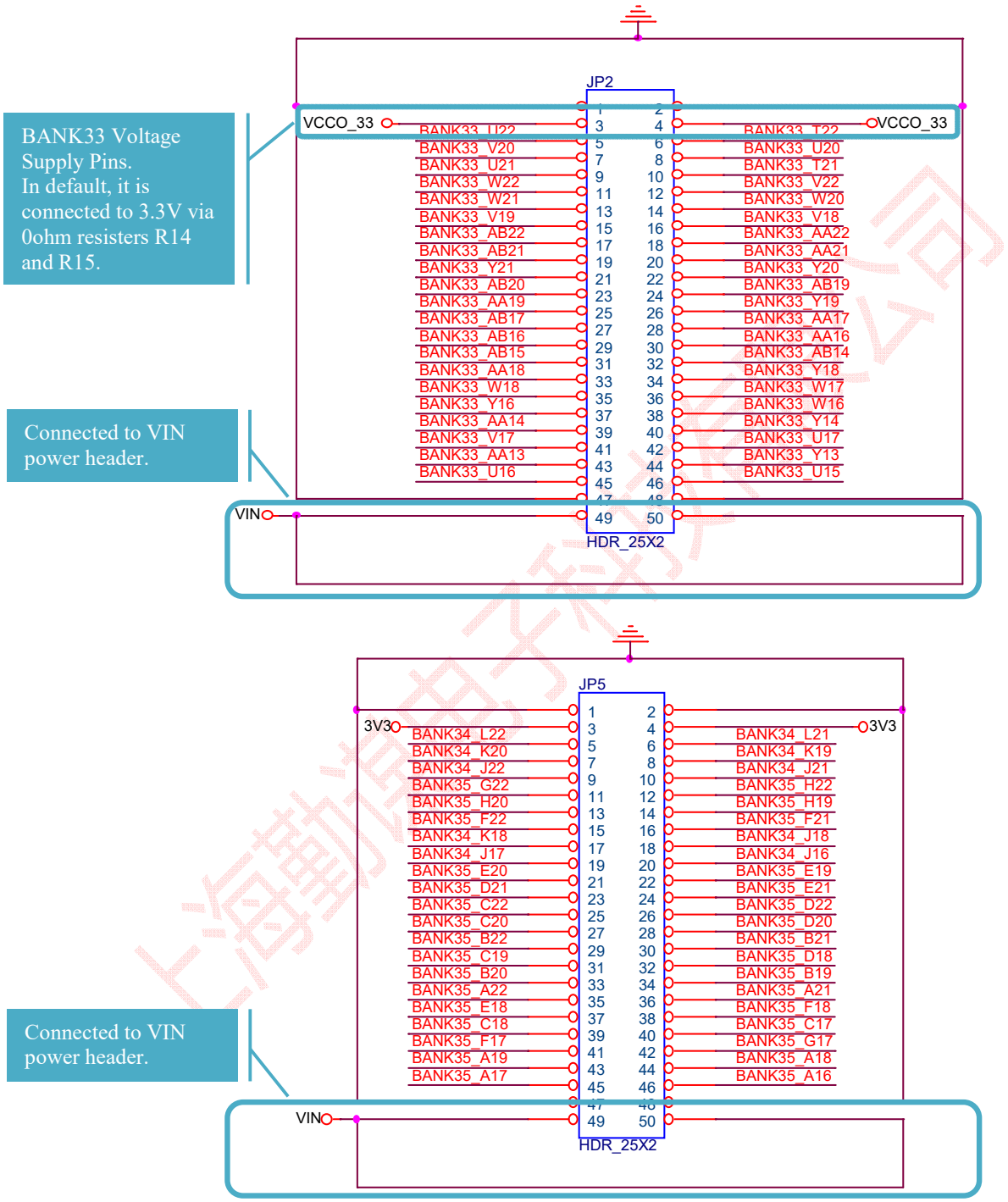

Figure 2-14. Extension IO

2.2.7 User LEDs

Below image shows two user LEDs and 3.3V power supply indicator:

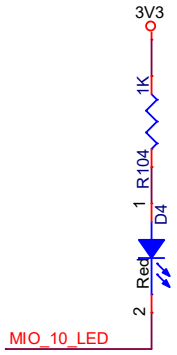

Figure 2-15. LED Connected to PS MIO[10]

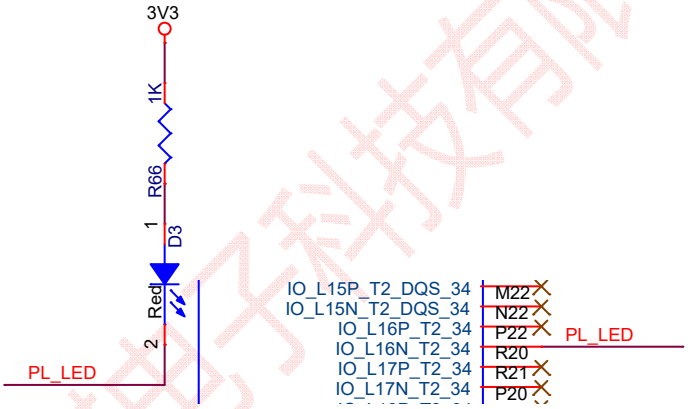

Figure 2-16. LED Connected to PL PIN P22

Figure 2-17. 3.3V Power Supply Status Indicator

The LED D2 will be turned on after the PL successfully loading configuration file from SD card during power on stage. In this case, LED D2 could be used as PL loading status indicator.

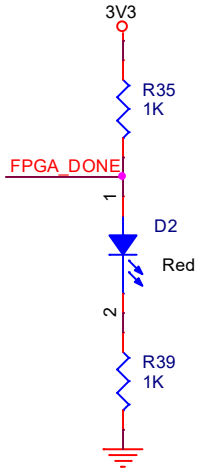

Figure 2-18. FPGA_DONE Status Indicator

2.2.8 JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

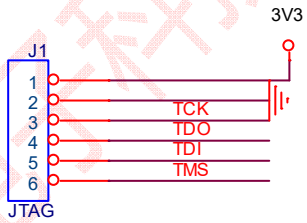

Figure 2-19. JTAG Port

2.2.1 USB to UART Interface

The CH340N is a USB to serial port bridge chip designed by WCH. The CH340N includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components are required for development. Below figure shows the hardware design of CH340N.

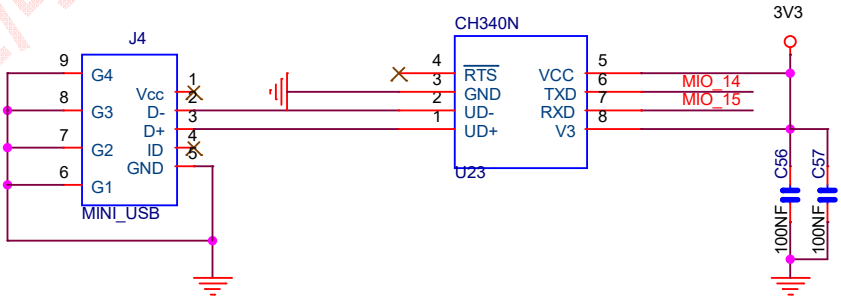

Figure 2-20. CH340N Hardware Design

2.2.2 DDR3 Memory

The Starter Kit has on board 16bit width data bus, 512MB memory size DDR3 MT41K256M16TW-107:P provided by Micron. Below image shows the detailed hardware design:

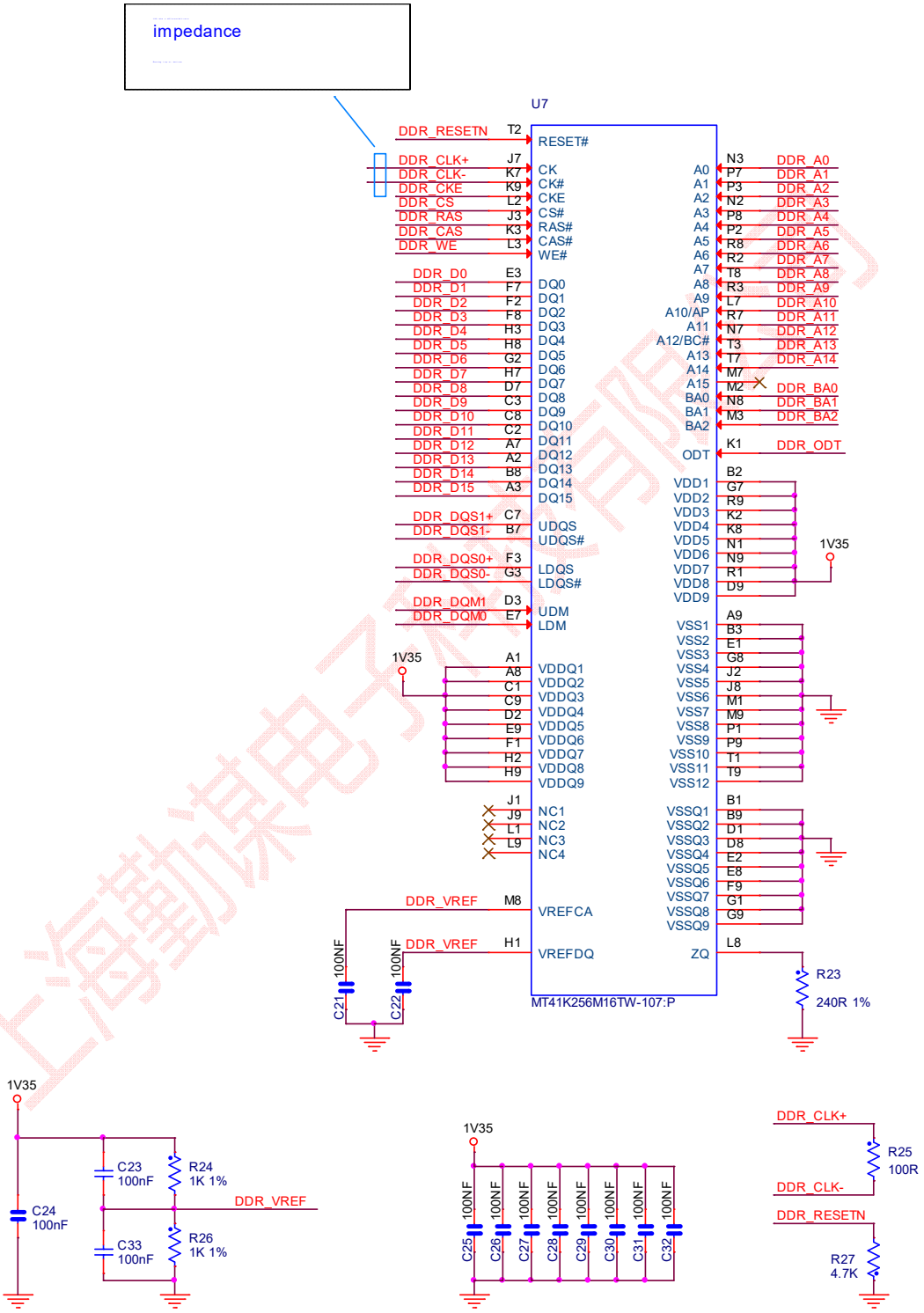

Figure 2-21. DDR3 Memory

2.2.3 RGMII Ethernet Interface

The Starter Kit provides RGMII ethernet interface by using RealTek's RTL8211E-VL. The RTL8211E-VL is connected to ZYNQ SoC's PS side. In default hardware design, it is working under 1000Mbps, RGMII mode. Detailed hardware design refers to below image.

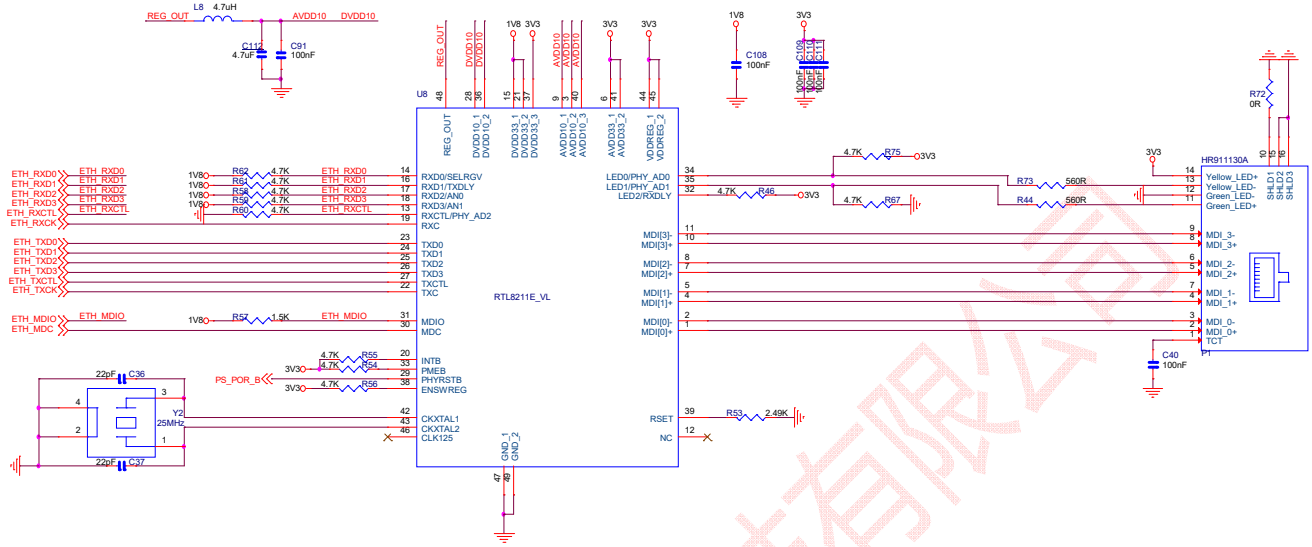

Figure 2-22. RGMII Ethernet

2.2.4 USB Host Port

The Starter Kit provides USB host port by using Microchip's ULPI PHY USB3320C. The USB3320C is connected to ZYNQ SoC's PS side. Detailed hardware design refers to below image.

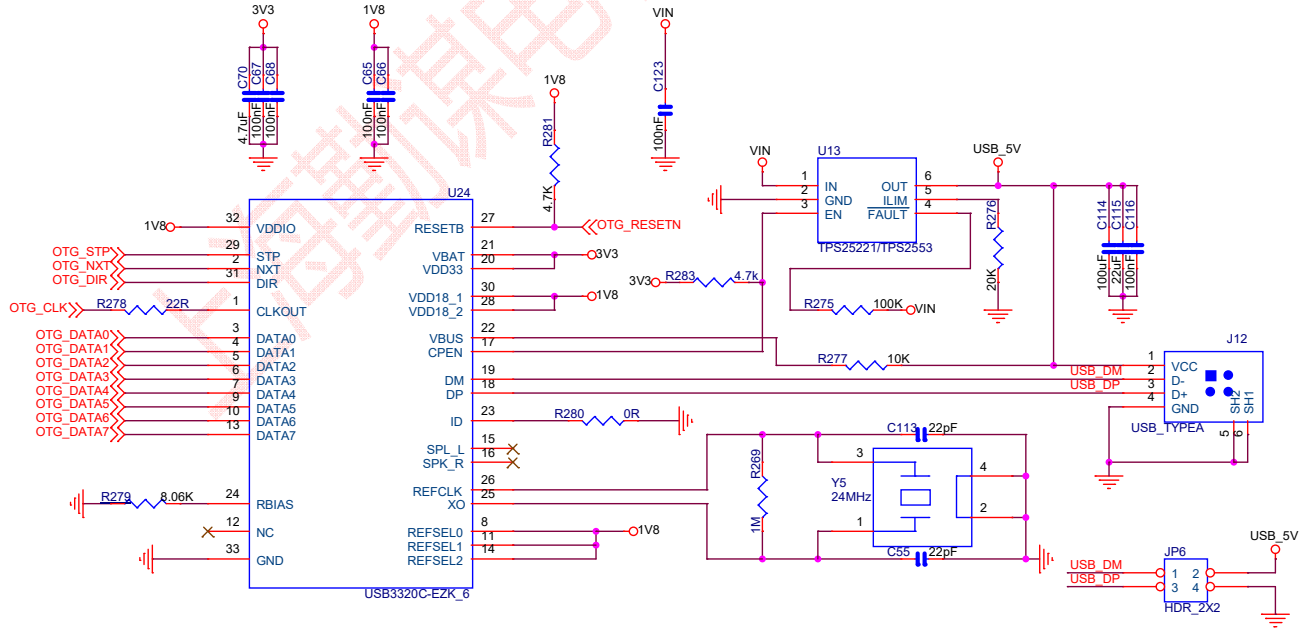

Figure 2-23. USB Host Port

3. Reference

[1] ug585-Zynq-7000-TRM.pdf
[2] ds187-XC7Z010-XC7Z020-Data-Sheet.pdf
[3] ug865-Zynq-7000-Pkg-Pinout.pdf
[4] MT41K256M16TW-107:P.pdf
[5] tps563201.pdf
[6] Rtl8211.PDF
[7] USB3320C.pdf

4. Revision

Doc. Rev.	Date	Comments
0.1	18/06/2023	Initial Version.
1.0	30/06/2023	V1.0 Formal Release.